

HM62A168, HM62A188 Series

Direct Mapped 8,192-Word x 16(18)-Bit/ 2-Way 4,096-Word x 16(18)-Bit Static Cache Memory

■ DESCRIPTION

The Hitachi HM62A168/188 is a high speed 128(144)-k Cache memory organized as 2-way set associative 4k x 16(18) or direct mapped 8k x 16(18).

By using two HM62A168/188 can be achieved high performance 32-bit microprocessor system. The HM62A168/188, packaged in a 52-pin PLCC is available for high density mounting.

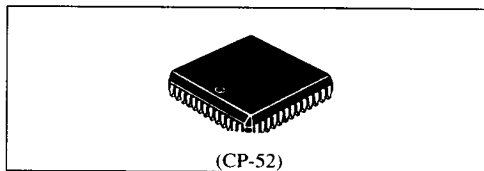
■ FEATURES

- Single 5V supply and high density 52-pin PLCC package
- High speed
Access time: 25/30/35 ns (maximum)
- Directly TTL compatible
All inputs and outputs
- Address latch
- Pin programmable for 8k x 16(18) or 2-way 4k x 16(18)

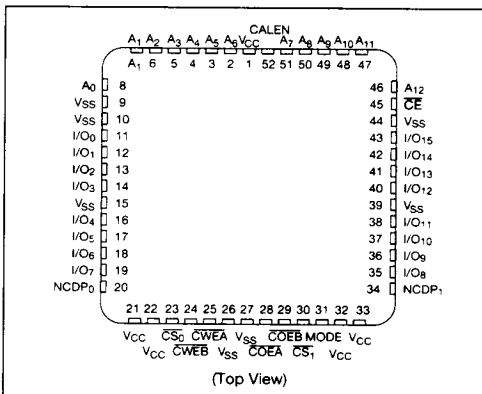
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62A168CP-25	25 ns	52-pin PLCC (CP-52)
HM62A168CP-25R	25 ns	
HM62A168CP-30	30 ns	
HM62A168CP-35	35 ns	
HM62A188CP-25	25 ns	
HM62A188CP-25R	25 ns	
HM62A188CP-30	30 ns	
HM62A188CP-35	35 ns	
HM62A168BCP-25*	25 ns	
HM62A168BCP-35*	35 ns	
HM62A188BCP-25*	25 ns	
HM62A188BCP-35*	35 ns	

*Please see note 6



■ PIN ARRANGEMENT



■ PIN DESCRIPTION

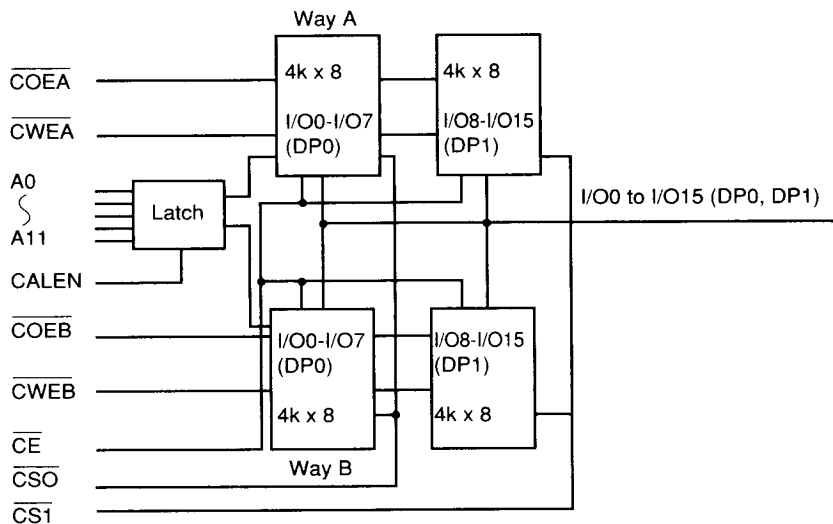
Pin Name	Function
CALEN	Cache Address Latch Enable
MODE	Mode Select
A0-A12	Address
CS0, CS1	Cache Chip Select
COEA, COEB	Cache Output Enable
CWEA, CWEB	Cache Write Enable
I/O0-I/O15	Data Input/Output
CE	Cache Chip Enable
NC	No Connection
DP0, DP1	Parity Input/Output



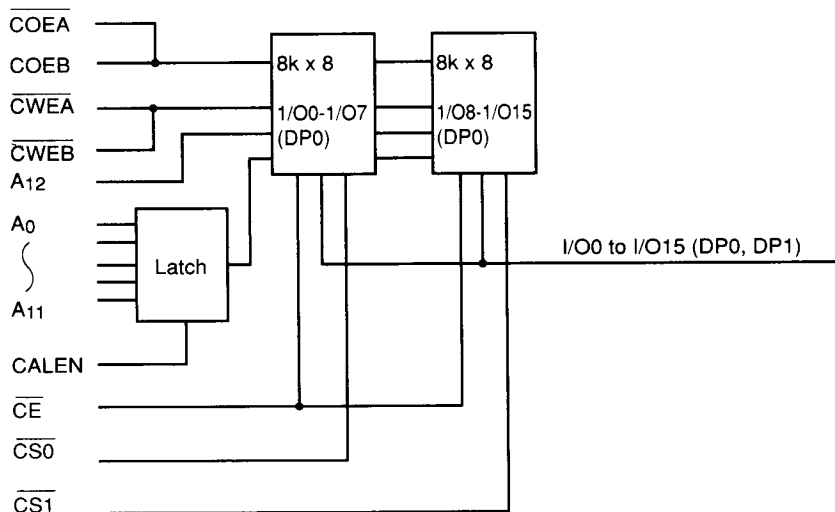
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■ BLOCK DIAGRAM

- **Topology Two-Way Set Associative** (MODE = Logic high)



- **Topology Direct Mapped** (MODE = Logic low)



Signal Description

Signal Name	Pin Number	Signal Description
A0-A6	8-2	Address inputs to the memory array. A0-A11 are latched on the falling edge of CALEN.
A7-A11	51-47	
A12	46	
		A12 address input. In the two-way mode, address input A12 will be a "don't care" and should be externally wired to ground.
		In the direct-mapped mode. When MODE is connected to VSS, A12 selects which of the two 4K x 16(18) banks is read from or written to. A12 is not latched by CALEN, as are the other address inputs.
CALEN	52	Cache Address Latch Enable input. This signal controls the internal address latches for inputs A0-A11. When CALEN is high, the latch is transparent. The falling edge of CALEN latches the current address input levels. A12 is static and is not controlled by CALEN.
I/O0-I/O15	11-14, 16-19, 35-38, 40-43	Data inputs and outputs. These are the three-state lines that provide data access to the memory array.
MODE	31	MODE input. This signal controls whether the memory device is to be used in a direct-mapped configuration (8K x 16(18)). When the MODE signal is high, the device is placed in the two-way mode. When the mode input is low, the cache is in the direct-mapped mode. This is a hard wired strap option and must not be changed dynamically.
$\overline{CS}_0, \overline{CS}_1$	23, 30	Cache Chip Select inputs. These active low signals selectively enable the two bytes of memory. $\overline{CS}_0$ low enables bits I/O0-I/O7 and DP0. $\overline{CS}_1$ low enables bits I/O8-I/O15 and DP1. This applies to both the direct-mapped and two-way modes.
$\overline{CE}$	45	Cache Chip Enable input (active low). This signal functions as a global chip enable. It gates the $\overline{COEA}$, $\overline{COEB}$, $\overline{CWEA}$, and $\overline{CWEB}$ inputs. A chip enable controlled write can be done by taking $\overline{CE}$ inactive high while one of the $\overline{CWEX}$ signals is active (assuming all other timings for a write cycle are met).
$\overline{COEA}, \overline{COEB}$	28, 29	Cache Output Enable inputs. These active low input enable cache bank A or bank B to drive the data bus when in the two-way mode. In the two-way mode, bank A is enabled when $\overline{COEA}$ is low and bank B is enabled when $\overline{COEB}$ is low. If both banks are activated at the same time, then both banks become deselected. In the direct-mapped mode, $\overline{COEA}$ and $\overline{COEB}$ must be tied together externally. A low on $\overline{COEA}$ and $\overline{COEB}$ then enables the outputs of the 8K x 16(18) memory. A12 is used to determine which 4K x 16(18) bank is accessed.
$\overline{CWEA}, \overline{CWEB}$	25, 24	Cache Write Enable inputs (active low). In the two-way mode when $\overline{CWEA}$ ($\overline{CWEB}$) is active, data is written into memory bank A (B). In the direct-mapped mode, $\overline{CWEA}$ and $\overline{CWEB}$ must be tied together externally. A low on $\overline{CWEA}$ and $\overline{CWEB}$ enables data to be written into the 8K x 16(18) memory. A12 is used to determine which 4K x 16(18) bank is accessed.
DP0 or NC	20	Parity data inputs and outputs (HM62A188). These are three-state lines that provide parity data access to the memory array. For the HM62A168, these two pins are not used (NC) and must not be physically tied to VCC, VSS, or any other device inputs.
DP1 or NC	34	
VCC	1, 21, 22, 32, 33	System Power +5V. (21, 22, 32, 33 are for outputs)
VSS	9, 10, 15, 26, 27 39, 44	System Ground. (10, 15, 39, 44 are for outputs)



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■ FUNCTION TABLE

Two-Way Mode (Mode = High) 2-4K x 16(18)

CE	CS ₀	CS ₁	COEA	COEB	CWEA	CWEB	I/O ₀ -I/O ₇ (DP ₀)	I/O ₈ -I/O ₁₅ (DP ₁)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output High-Z
X	X	X	L	L	X	X	High-Z	High-Z	Output High-Z
L	L	H	L	H	H	H	Output	High-Z	Read Way A
L	L	H	H	L	H	H	Output	High-Z	Read Way B
L	H	L	L	H	H	H	High-Z	Output	Read Way A
L	H	L	H	L	H	H	High-Z	Output	Read Way B
L	L	L	L	H	H	H	Output	Output	Read Way A
L	L	L	H	L	H	H	Output	Output	Read Way B
L	L	H	X	X	L	H	Input	High-Z	Write Way A
L	L	H	X	X	H	L	Input	High-Z	Write Way B
L	H	L	X	X	L	H	High-Z	Input	Write Way A
L	H	L	X	X	H	L	High-Z	Input	Write Way B
L	L	L	X	X	L	H	Input	Input	Write Way A
L	L	L	X	X	H	L	Input	Input	Write Way B
L	L	H	X	X	L	L	Input	High-Z	Write Way A & B
L	H	L	X	X	L	L	High-Z	Input	Write Way A & B
L	L	L	X	X	L	L	Input	Input	Write Way A & B

Direct Mode (Mode = Low) 8K x 16(18)

CE	CS ₀	CS ₁	COEA	COEB	CWEA	CWEB	I/O ₀ -I/O ₇ (DP ₀)	I/O ₈ -I/O ₁₅ (DP ₁)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output High-Z
L	L	H	L	L	H	H	Output	High-Z	Read
L	H	L	L	L	H	H	High-Z	Output	Read
L	L	L	L	L	H	H	Output	Output	Read
L	L	H	X	X	L	L	Input	High-Z	Write
L	H	L	X	X	L	L	High-Z	Input	Write
L	L	L	X	X	L	L	Input	Input	Write



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to VSS	V _{in}	-0.5* ¹ to +7.0	V
Power Dissipation	P _T	1.4	W
Operating Temperature Range	T _{opr}	0 to +70	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T _{bias}	-10 to +85	°C

Note: 1. V_{in} min = -2.5 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATION CONDITIONS (T_a = 0 to +70°C, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V _{CC}	4.5* ¹	5.0	5.5* ¹	V
	V _{SS}	0	0	0	V
Input High (Logic 1) Voltage	V _{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V _{IL}	-0.5* ²	—	0.8	V

Note: 1. V_{CC} min = 4.75V and V_{CC} max. = 5.25V for HM62A168/188-25/25R/30.
 2. V_{IL} min = -2.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%*¹, V_{SS} = 0V, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit	Test Conditions
Input Leakage Current	I _{LI}	—	—	2.0	μA	V _{CC} = Max., V _{in} = V _{SS} to V _{CC}
Output Leakage Current	I _{LO}	—	—	10.0	μA	Output Disable V _{I/O} = V _{SS} to V _{CC}
Active Operating Power Supply Current	I _{CC}	—	—	220	mA	V _{in} = V _{SS} /V _{CC} , I _{I/O} = 0 mA. 2X Min. Cycle, CE, CS = V _{IL} Max., CALEN = V _{IH} Min.
Output Low Voltage	V _{OL}	—	—	0.4	V	I _{OL} = 4 mA
Output High Voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

Notes: 1. V_{CC} = 5V ± 5% for HM62A168/188-25/25R/30, HM62A168B/188B-25.
 2. Typical limits are at V_{CC} = 5.0, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1 MHz.)*¹

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C _{in}	—	6	pF	V _{in} = 0V
Input/Output Capacitance	C _{I/O}	—	12	pF	V _{I/O} = 0V

Note: 1. This parameter is sampled and not 100% tested.

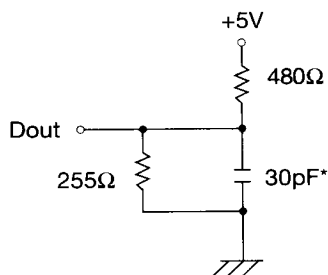


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AC CHARACTERISTICS ($T_a = 0$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted.)

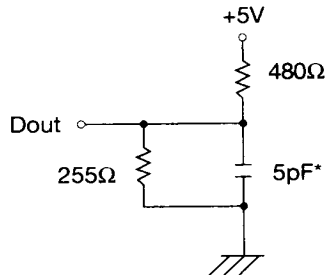
Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 3ns
- Input and Output timing reference levels: 1.5V
- Output load: See figures
- Exceeding minimum air flow equipment: See air flow requirements



Output Load (A)

*Including scope & jig.



Output Load (B)

(for t_{CHZ} , t_{CLZ} , t_{WHZ} & t_{OW})

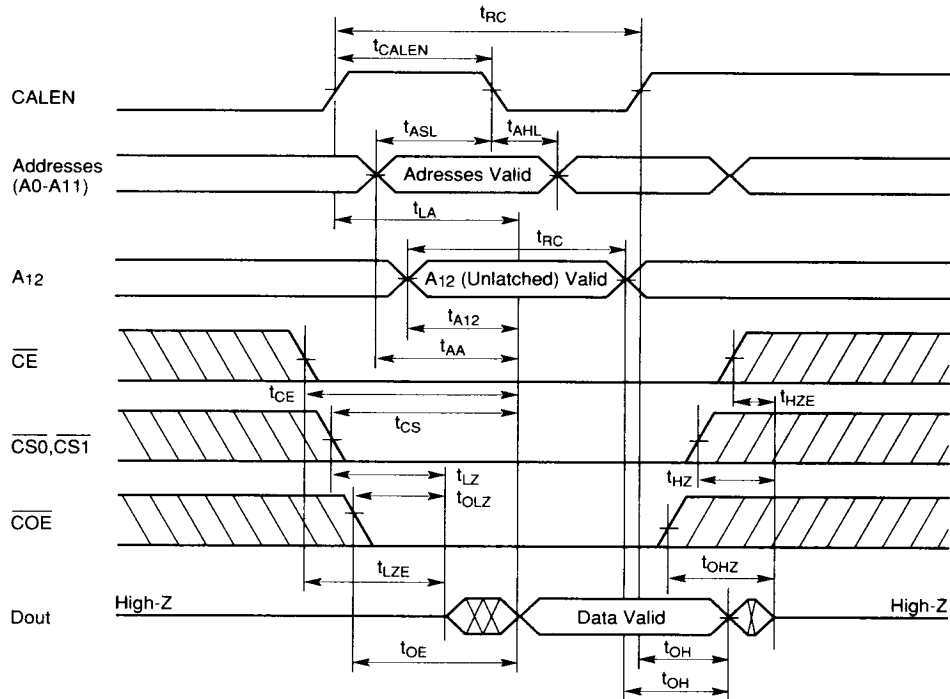
Note: 1. $V_{CC} = 5\text{V} \pm 5\%$ for HM62A168/188-25/25R/30, HM62A168B/188B-25.

READ CYCLE

Parameter	Symbol	HM62A168/B-25 HM62A188/B-25		HM62A168-25R HM62A188-25R		HM62A168-30 HM62A188-30		HM62A168/B-35 HM62A188/B-35		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	25	—	25	—	30	—	35	—	ns	
Address Access Time	t_{AA}	—	25	—	25	—	30	—	35	ns	
A12 Address Access Time	t_{A12}	—	17	—	17	—	20	—	25	ns	
Chip Select Access Time	t_{CS}	—	20	—	20	—	20	—	25	ns	
Chip Enable Access Time	t_{CE}	—	20	—	22	—	22	—	25	ns	
CALEN High to Output Valid	t_{LA}	—	25	—	25	—	30	—	35	ns	1
Output Enable to Output Valid	t_{OE}	—	10	—	10	—	12	—	13	ns	
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	3	—	ns	2
Chip Select to Output Low-Z	t_{LZ}	3	—	3	—	3	—	3	—	ns	3
Chip Enable Low to Output Low-Z	t_{LZE}	5	—	5	—	5	—	5	—	ns	3
Output Enable to Output Low-Z	t_{OLZ}	2	—	2	—	2	—	2	—	ns	3
Chip Deselect to Output High-Z	t_{HZ}	—	15	—	15	—	15	—	25	ns	3
Chip Enable High to Output High-Z	t_{HZE}	—	15	—	15	—	15	—	25	ns	3
Output Disable to Output High-Z	t_{OHZ}	—	10	—	10	—	10	—	14	ns	3
Address Latch Enable Pulse Width	t_{CALEN}	8	—	8	—	8	—	10	—	ns	
Address Setup to Latch Low	t_{ASL}	4	—	4	—	4	—	6	—	ns	
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	5	—	ns	



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■ READ TIMING WAVEFORM (1) ($\overline{CWE} = \text{High}$)


- Notes:
1. t_{LA} is applied to the case that address is valid before CALEN goes high.
 2. t_{OH} is determined by the earliest of CALEN going high, valid addresses A0-A11 transition with CALEN high, or A12 transition.
 3. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.



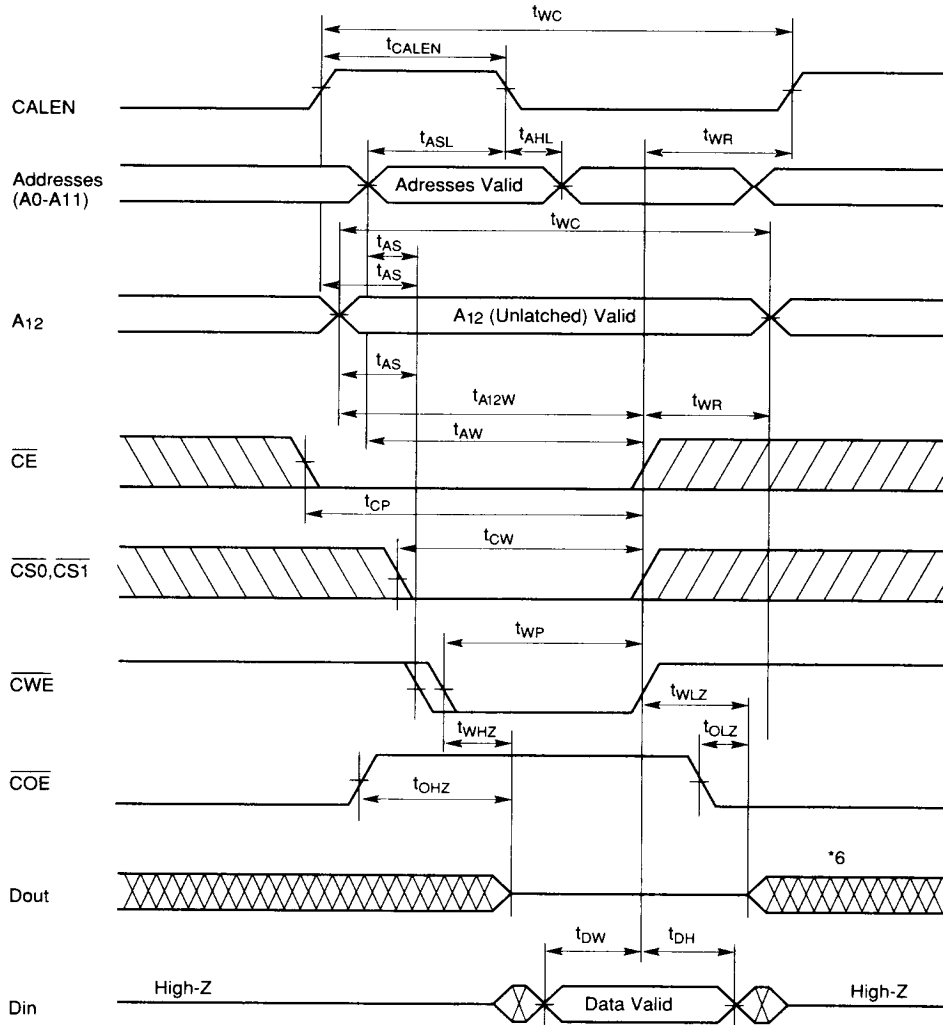
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■ WRITE CYCLE

Parameter	Symbol	HM62A168/B-25 HM62A188/B-25		HM62A168-25R HM62A188-25R		HM62A168-30 HM62A188-30		HM62A168/B-35 HM62A188/B-35		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	tWC	25	—	25	—	30	—	35	—	ns	
Address Valid to End of Write	tAW	18	—	18	—	18	—	25	—	ns	1
A12 Valid to End of Write	tA12W	18	—	18	—	18	—	25	—	ns	
Chip Select to End of Write	tCW	18	—	18	—	18	—	25	—	ns	
Data Valid to End of Write	tDW	10	—	10	—	10	—	10	—	ns	
Data Hold from End of Write	tDH	0	—	0	—	0	—	0	—	ns	
Write Enable Active to High-Z	tWHZ	—	15	—	15	—	15	—	15	ns	5
Write Enable Inactive to Low-Z	tWLZ	3	—	3	—	3	—	3	—	ns	5
Write Pulse Width	tWP	15	—	15	—	18	—	25	—	ns	
CE Pulse Width During Chip Enable Controlled Write	tCP	15	—	15	—	18	—	25	—	ns	
Address Setup Time	tAS	0	—	0	—	0	—	0	—	ns	2
Write Recovery Time	tWR	0	—	0	—	0	—	0	—	ns	3
Address Latch Enable Pulse Width	tCALEN	8	—	8	—	8	—	10	—	ns	
Address Setup to Latch Low	tASL	4	—	4	—	4	—	6	—	ns	
Address Hold to Latch Low	tAHL	5	—	5	—	5	—	5	—	ns	
Chip Enable Low to Output Low-Z	tOLZ	2	—	2	—	2	—	2	—	ns	
Output Disable to Output High-Z	tOHZ	—	10	—	10	—	10	—	10	ns	

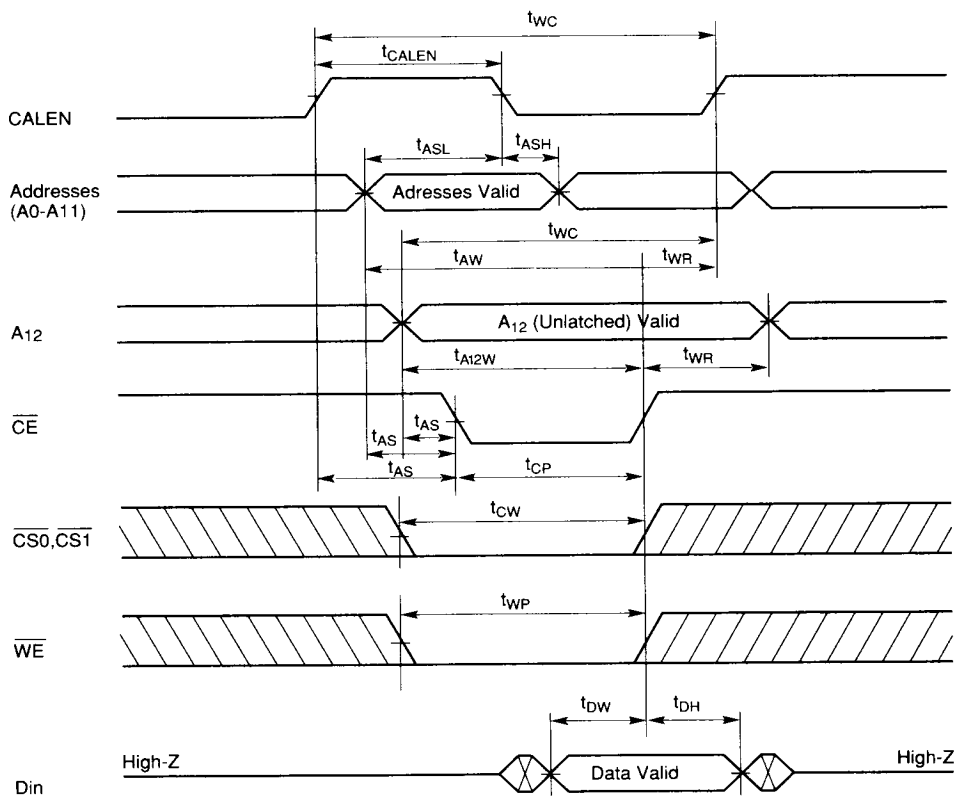


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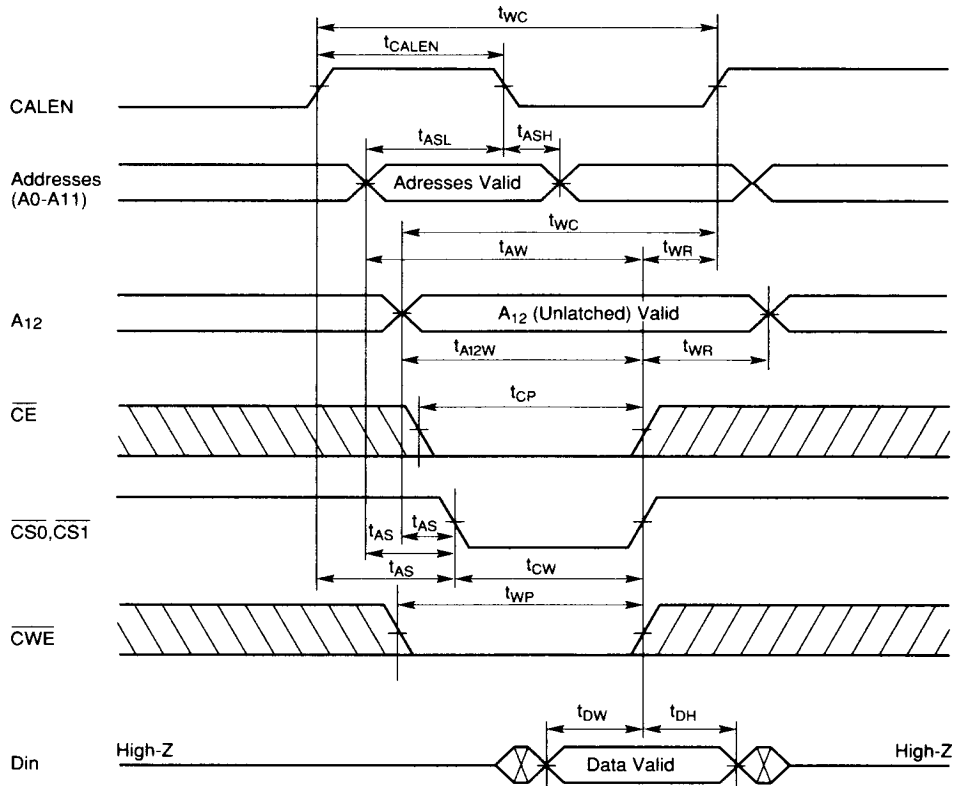
■ WRITE TIMING WAVEFORM (1) ($\overline{WE}$ Controlled)


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■ **WRITE TIMING WAVEFORM (2)** ($\overline{\text{COE}} = \text{High}$, $\overline{\text{CE}}$ Controlled)



■ WRITE TIMING WAVEFORM (3) ($\overline{\text{COE}}$ = High, $\overline{\text{CS}}$ Controlled)



- Notes:
1. t_{AW} is measured from the later of CALEN going high, or addresses A0-A11 transition with CALEN high to the end of write cycle.
 2. t_{AS} is measured from the latest of CALEN going high, addresses A0-A11 transition with CALEN high, or address A12 transition to the beginning of write cycle.
 3. t_{WR} is measured from the earliest of $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ going high to the earlier of CALEN going high, or address A12 transition.
 4. A write occurs during the overlap of a low $\overline{\text{CS0}}$ or $\overline{\text{CS1}}$, a low $\overline{\text{CE}}$, and a low $\overline{\text{WE}}$.
 5. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
 6. Dout is not the same phase of write data of this write cycle. Normal read cycle shall be used for write verify. This does not apply to the HM62A168B and HM62A188B.



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■ AIR FLOW REQUIREMENTS

