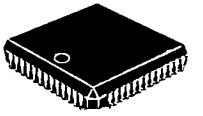
Dual 8,192-Word x 20-Bit Static Cache Memory

■ DESCRIPTION

The HM62A2016 is a high speed 327,680-bit cache memory organized as two banks of 8,192 words by 20-bits. The device includes dual address latches, dual chip select latches, data multiplexer with multiple chip enables and output enables. It can be used in a cache memory system adopting Harvard architecture which requires separate instruction and data storages.



(CP-52)

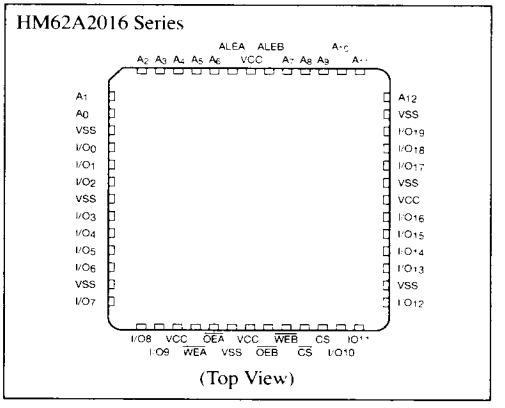
■ FEATURES

- High speed: up to 33 MHz operation
  Address access time: 17/20/25/30 ns
  Output enable access time: 7/7/8/8 ns
- Dual 8k x 20 memory arrays with data multiplexer
- Dual latches for address and chip select inputs
- Expandable both in width and depth
  Two separate chip selects
- 52-pin PLCC

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62A2016CP-17	17 ns	52-pin PLCC (CP-52)
HM62A2016CP-20	20 ns	
HM62A2016CP-25	25 ns	
HM62A2016CP-30	30 ns	

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0-A12	Address Inputs
ALEA, ALEB	Latch Enables
$\overline{OEA}$, $\overline{OEB}$	Output Enables
$\overline{WEA}$, $\overline{WEB}$	Write Enable
I/O0-I/O19	Data Inputs Outputs
CS, $\overline{CS}$	Chip Selects

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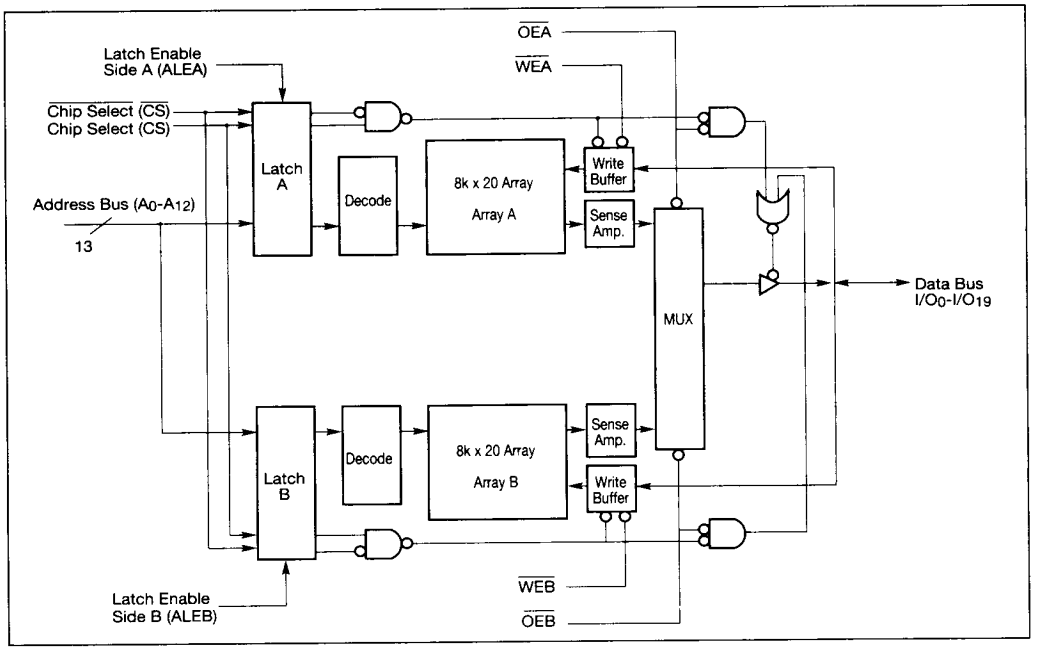
■ BLOCK DIAGRAM



Signal Description

Signal Name	Pin Number	Signal Description
A0-A12	3–9 46–51	Shared address inputs to both Memory Array A and Memory Array B. Current A_0–A_{12} values are latched into Latch A or Latch B by the falling edge of ALEA or ALEB.
ALEA, ALEB	2, 52	Latch enable inputs. When ALEA or ALEB is high, Latch A or Latch B is transparent to address and chip select input values. The falling edge of ALEA and ALEB latches current inputs at A_0–A_{12} and current states of CS and $\overline{CS}$. These latched values remain applied to the respective memory arrays until ALEA or ALEB transition to a high state.
$\overline{CS}$, CS	30, 31	Active low and active high chip select inputs. The current states of CS and $\overline{CS}$ are latched by the falling edge of ALEA and ALEB. When $\overline{CS}$ is low and CS is high read and write access to both arrays is possible. $\overline{CS}$ should be grounded and CS should be tied to V_{CC} in applications where no device depth expansion takes place. See the Depth Expansion Section for a detailed description of the chip select function.
$\overline{WEA}$, $\overline{WEB}$	24, 29	Active low write enable inputs. $\overline{WEA}$ controls writing into Array A and $\overline{WEB}$ controls writing into Array B. Both $\overline{WEA}$ and $\overline{WEB}$ must not be both low simultaneously.
$\overline{OEA}$, $\overline{OEB}$	25, 28	Active low output enable inputs. $\overline{OEA}$ and $\overline{OEB}$ are used to control driving of stored data from Array A or Array B onto the I/O lines during read operations. $\overline{OEA}$ and $\overline{OEB}$ must not be both low simultaneously.
I/O_0, I/O_{19}	11–13, 15–18 20–22, 32–34, 36–39, 42–44	Data inputs and outputs. These are three-state lines that provide data access to both memory arrays.

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■ FUNCTION TABLE

CS	$\overline{CS}$	ALEA	ALEB	$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	Operation	I/O Status
L	X	*1	*1	X	X	X	X	Not Selected	Outputs High-Z
X	H	*1	*1	X	X	X	X	Not Selected	Outputs High-Z
H	L	X	X	H	H	H	H	Data I/O's Disabled	Outputs High-Z
H	L	H	X	H	H	L	H	Read from Array A (Current Addresses)	Data Out
H	L	L	X	H	H	L	H	Read from Array A (Latched Addresses)	Data Out
H	L	X	H	H	H	H	L	Read from Array B (Current Addresses)	Data Out
H	L	X	L	H	H	H	L	Read from Array B (Latched Addresses)	Data Out
H	L	X	X	X	X	L*2	L*2	Not Allowed in Same Phase	—
H	L	H	X	L	H	H	H	Write to Array A (Current Addresses)	Data In
H	L	L	X	L	H	H	H	Write to Array A (Latched Addresses)	Data In
H	L	X	X	L*3	H	L*3	H	Not Allowed in Same Phase	—
H	L	X	X	L*4	H	H	L*4	Not Allowed in Same Phase	—
H	L	X	H	H	L	H	H	Write to Array B (Current Addresses)	Data In
H	L	X	L	H	L	H	H	Write to Array B (Latched Addresses)	Data In
H	L	X	X	H	L*4	L*4	H	Not Allowed in Same Phase	—
H	L	X	X	H	L*3	H	L*3	Not Allowed in Same Phase	—
H	L	X	X	L*5	L*5	X	X	Not Allowed in Same Phase	—

X = Don't care, H = High, L = Low, High-Z = High Impedance

Notes: 1. CS and CS values shown in the table must have propagated through transparent latches and meet specified chip select setup times before a deselect operation can occur.
2. If data are read simultaneously from both arrays, an undefined data outputs. Specified AC and DC parameters are not guaranteed in this state.
3. Simultaneous reading and writing of a single array or of both arrays is not permitted.
4. Simultaneous reading from one array while writing to the other array is not possible.
5. Simultaneous writing to both arrays is not permitted during normal R3000 based cache operation.

■ FUNCTIONAL DESCRIPTION

The HM62A2016 is a highly-integrated memory device with several performance-enhancing features which allow direct interfacing to a MIPS R3000 or R3000A RISC processor. Two independent address latches, with fast setup times, are provided on-chip to allow faster addressing of two 8k x 20 memory arrays, Array A and Array B. Address inputs and data I/O lines are shared between the two arrays.

Two sets of $\overline{OE}$ and $\overline{WE}$ inputs, coupled with an on-board multiplexer control read and write access to each of the arrays. Integrating a 2:1 output data multiplexer on-chip reduces the problem of data bus contention that may occur when using discrete SRAMs and multiplexers, and allows easier synchronization of output enable signals.

$\overline{OEA}$ and $\overline{OEB}$ inputs directly control the driving of stored data at the outputs of the HM62A2016 during read operations. Fast (7 ns) output enable and disable times are matched and permit data to be quickly taken off the data bus as well as driven on. This high level of device feature integration demonstrated by the HM62A2016 allows construction of a dual 32-kbyte cache memory subsystem by combining only three devices together to reach the full 60-bit tag plus data width requirements of the MIPS R3000(a) processor.

The HM62A2016 is designed to permit storage and retrieval of tag address and cache data information to and from the two memory arrays in a direct-mapped, split data/instruction cache format. It is functionally compatible to and meets all MIPS R3000(A) cache memory timing requirements. The HM62A2016 fully supports "pipelined" reads and writes, as described below.

Valid addresses that appear at A_0—A_{12} inputs are recognized by on-chip Latches A or B when they are transparent (i.e. when ALEA or ALEB inputs are high). Current address input values are latched by the falling edge of ALEA and ALEB.

For an R3000(A) to HM62A2016 cache interface, addresses are latched during the first phase of a 2-phase read operation cycle, and valid data appears at outputs (I/O_0–I/O_{19}) during the second phase. These addresses will remain latched and applied to Array A or Array B as long as ALEA or ALEB remains low. Similarly, for a write operation, valid addresses are also latched during the first phase, while data is actually written into the addressed location during the second phase.

These sequential reads occur in a pipe-lined manner, where data or instructions are read from one array during the same phase when addresses for a subsequent read from the other array are latched. Similarly, alternating consecutive writes to the two memory arrays are possible as long as the minimum 2-phase write operation cycle is met with correct timings.

A write operation to a memory array can occur in the phase that immediately precedes or follows a read operation from the other array.

It is not possible to write to or read from both arrays at the same time. Nor is it possible to do more than one read or write per phase. It is not possible to read from or write to the same array in consecutive phases because of the minimum 2-phase read/write operation cycle requirements. See the Function Table for a detailed listing of prohibited operations, as well as legitimate read and write modes.

Array A and B are interchangeable and can arbitrarily be designated as for data or instruction storage.

Depth Expansion

Overview

Each HM62A2016 has a latched active high chip select input (CS) as well as an active low input ($\overline{CS}$). Depth expansion is achieved by connecting address line (A_{13}) into CS and $\overline{CS}$ inputs of two HM62A2016's and grounding or tying to V_{CC} the other remaining chip select of each device, as shown in figure 1. Corresponding (A or B) control inputs ($\overline{OE}$, $\overline{WE}$, and ALE) of depth-expanded HM62A2016's should be tied together.

The latched chip select function of the HM62A2016 is designed to permit one array to be latched "on" (active for read or write access) while the other corresponding array of a different davice is turned "off".

Detailed Description

The current states of CS and $\overline{CS}$ are latched on-chip by the falling edge of ALEA or ALEB. An "array select" state (both $\overline{CS}$ = 1 and $\overline{CS}$ = 0), that passes through a single transparent Latch (A or B) and meets t_{CSL} timing, will permit that particular array (A or B) to be active for read and write access. An array in a selected state will remain active as long as its ALE input remains low. If an array select state is recognized by both transparent latches (A and B), then both arrays for that HM62A2016 device will be active.

A "deselect" state (either $\overline{CS}$ = 0 or CS = 1) that propagates through a single transparent latch (A or B) and meets the minimum specified chip select setup time will disable both read and write access to that respective array (Array A or Array B). If a deselecting input state passes through both transparent latches A and B, then read and write access to both arrays is disabled.

Example

An example of consecutive reads from two depth-expanded HM62A2016's is shown in Read Cycle No. 2. In the first phase, an instruction is read from the I-cache of the "low RAM". At the beginning of this phase, A_{13} transitions from low to high and causes the selection of the D-cache array of the "high RAM" for a read operation in the following phase. This high A_{13} state also deselects the D-cache array of the "low RAM" for the following phase.

Consecutive operations are possible because the latching of A_{13} to select or deselect an array can occur in the same phase as a read or write operation from another array of a different HM62A2016.

As a further example, the timings for a depth-expanded store-load sequence are shown in Write Cycle No. 2.

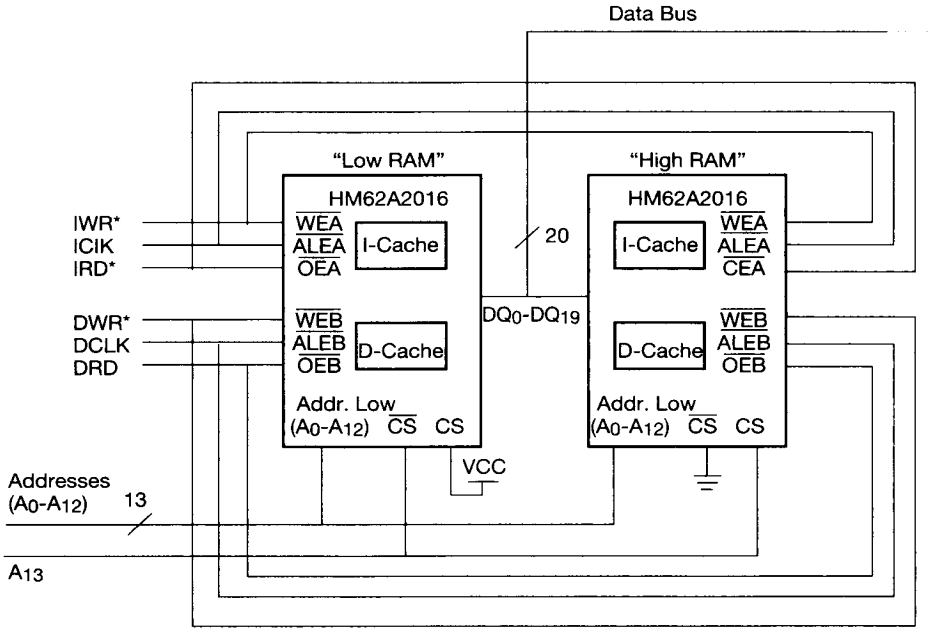

Figure 1. 16k x 20 x 2 Cache SRAM from two 8K x 20 x 2 Cache SRAMs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage relative to V_{SS}	V_{CC}	−0.5*1 to +7.0	V
Voltage on any pin relative to V_{SS}	V_{in}	−0.5*1 to V_{CC} +0.3	V
Power Dissipation	P_T	2.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_{in} min = −2.5 V for pulse width 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

Note: 1. V_{IL} min = −2.0V for pulse width 10 ns.
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, exceeding minimum air flow requirement)

Parameter	Symbol	Min.	Typ	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	µA	Output Disable $V_{I/O}$ = V_{SS} to V_{CC}
Active Operating Power Supply Current	I_{CC}	—	—	220	mA	V_{in} = V_{SS} to V_{CC}, Outputs Open Load, I_{out} = 0 mA, t_{cycle} = Min. Cycle, $\overline{CS}$ = V_{IL} Max., CS = V_{IH} Min.
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} =8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA

Note: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading

■ CAPACITANCE (T_a = 25°C, f= 1 MHz.)*1

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is sampled and not 100% tested.

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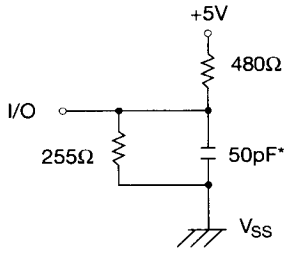
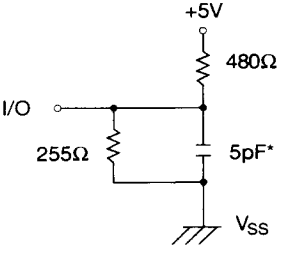
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = to 70°C, exceeding minimum air flow requirement)

Test Conditions

- Input and Output timing reference levels: 1.5V
- Input pulse levels: V_{SS} to 3V
- Output load: See figures



Output Load (A)
*Including scope & jig.



Output Load (B)
(for t_{OLZ} & t_{OHZ})

■ READ CYCLE

Parameter	Frequency / Symbol	33 MHz HM62A2016-17		25 MHz HM62A2016-20		20 MHz HM62A2016-25		16.67 MHz HM62A2016-30		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	17	—	20	—	25	—	30	—	ns
Address Valid to Output Valid	tAA	—	17	—	20	—	25	—	30	ns
Chip Select Access Time	tACS*1	—	17	—	20	—	25	—	30	ns
Output Enable Low to Output Valid	tOE	—	7	—	7	—	8	—	8	ns
Output Enable Low to Output Low-Z	tOLZ	1	—	2	—	2	—	2	—	ns
Output Enable High to Output High-Z	tOHZ	0	7	0	7	0	8	0	8	ns
Output Hold from Latch Enable	tLOH	3	—	3	—	3	—	3	—	ns
Address Setup to Latch Enable Low	tASL	5	—	5	—	5	—	5	—	ns
Address Hold from Latch Enable Low	tAHL	2	—	2	—	2	—	2	—	ns
Chip Select Setup to Latch Enable Low	tCSL*1	5	—	5	—	5	—	5	—	ns
Chip Select Hold from Latch Enable Low	tCSH*1	2	—	2	—	2	—	2	—	ns
Output Enable Separation Time	tOSP	2	—	2	—	2	—	2	—	ns
Latch High to Address Valid	tLAV	3	—	3	—	3	—	3	—	ns

Note: 1. Indicates depth expansion parameter only. These parameters apply for both CS and $\overline{CS}$.

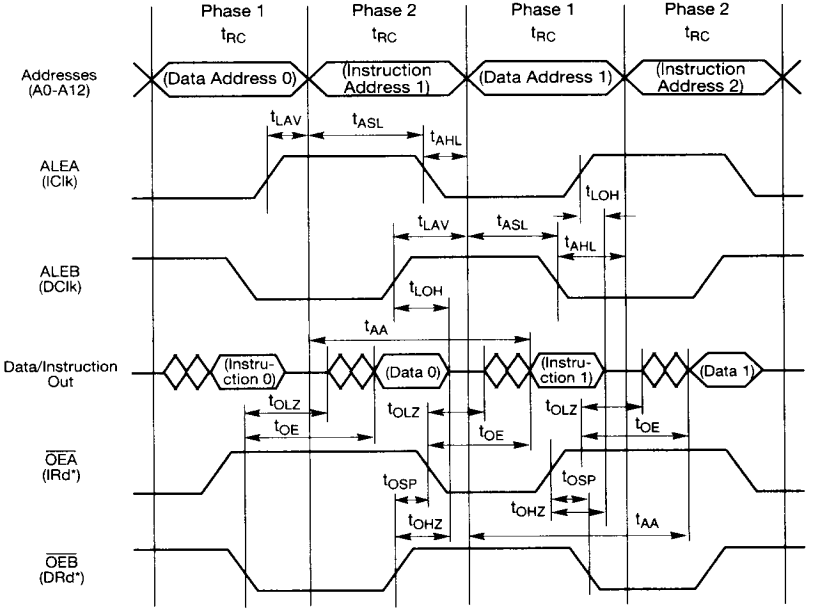
■ WRITE CYCLE

Parameter	Frequency / Symbol	33 MHz HM62A2016-17		25 MHz HM62A2016-20		20 MHz HM62A2016-25		16.67 MHz HM62A2016-30		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	17	—	20	—	25	—	30	—	ns
Address Valid to End of Write	tAW	12	—	15	—	20	—	25	—	ns
Data Valid to End of Write	tDS	6	—	8	—	8	—	10	—	ns
Data Hold from End of Write	tDH	0	—	0	—	0	—	0	—	ns
Write Pulse Width	tWP	10	—	15	—	17	—	22	—	ns
Chip Enable to End of Write	tCW*1	12	—	15	—	20	—	25	—	ns
Address Setup Time Before Write Start	tAS	0	—	0	—	0	—	0	—	ns
Latch Enable Hold from End of Write	tWHL	0	—	0	—	0	—	0	—	ns
Address Setup to Latch Enable Low	tASL	5	—	5	—	5	—	5	—	ns
Address Hold from Latch Enable Low	tAHL	2	—	2	—	2	—	2	—	ns
Chip Select Setup to Latch Enable Low	tCSL*1	5	—	5	—	5	—	5	—	ns
Chip Select Hold from Latch Enable Low	tCSH*1	2	—	2	—	2	—	2	—	ns
Read/Write Separation Time	tRWS	2	—	2	—	2	—	2	—	ns
Latch High to Address Valid	tLAV	3	—	3	—	3	—	3	—	ns

Note: 1. Indicates depth expansion parameter only. These parameters apply for both CS and $\overline{CS}$.

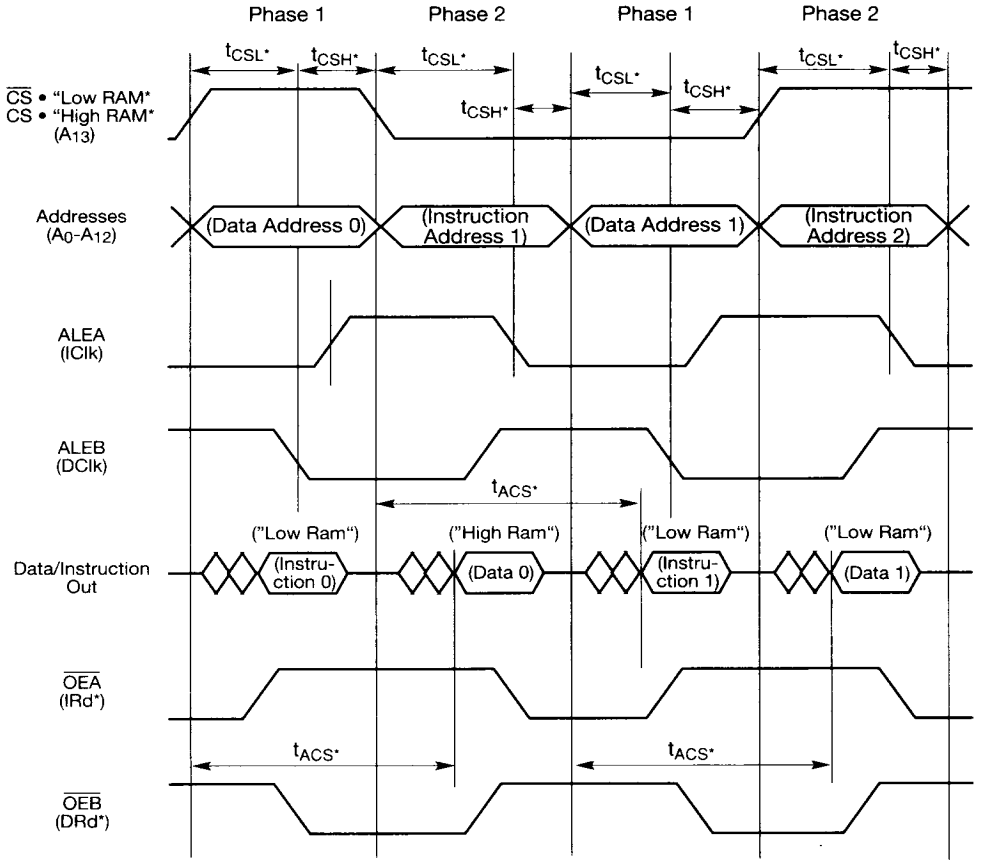
■ TIMING WAVEFORMS

Read Cycle No. 1 ($\overline{CS}$ = Low, CS, $\overline{WEA}$, $\overline{WEB}$ = High)



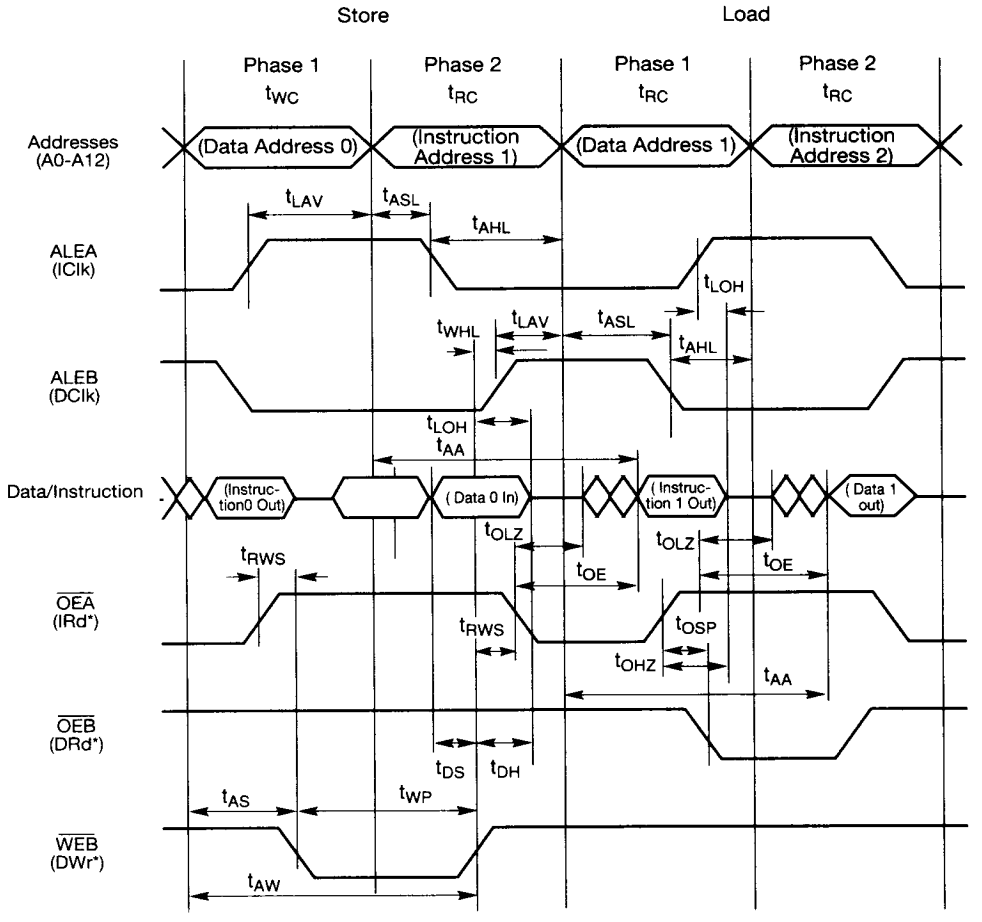
Notes:
1. All timing parameters are measured with output Load A unless otherwise noted.
2. Read cycle time (tRC) refers to read operations with current addresses applied to a transparent (high) latch. Read timing parameters are referenced from the last valid address to the first transition address.
3. Transition is measured ±200 mV from steady state voltage with output Load B for tOLZ and tOHZ. These parameters are sampled and not 100% tested.

Read Cycle No. 2 ($\overline{WEA}$, $\overline{WEB}$ = High) (Consecutive Reads from Two Depth-Expanded HM62A2016's)



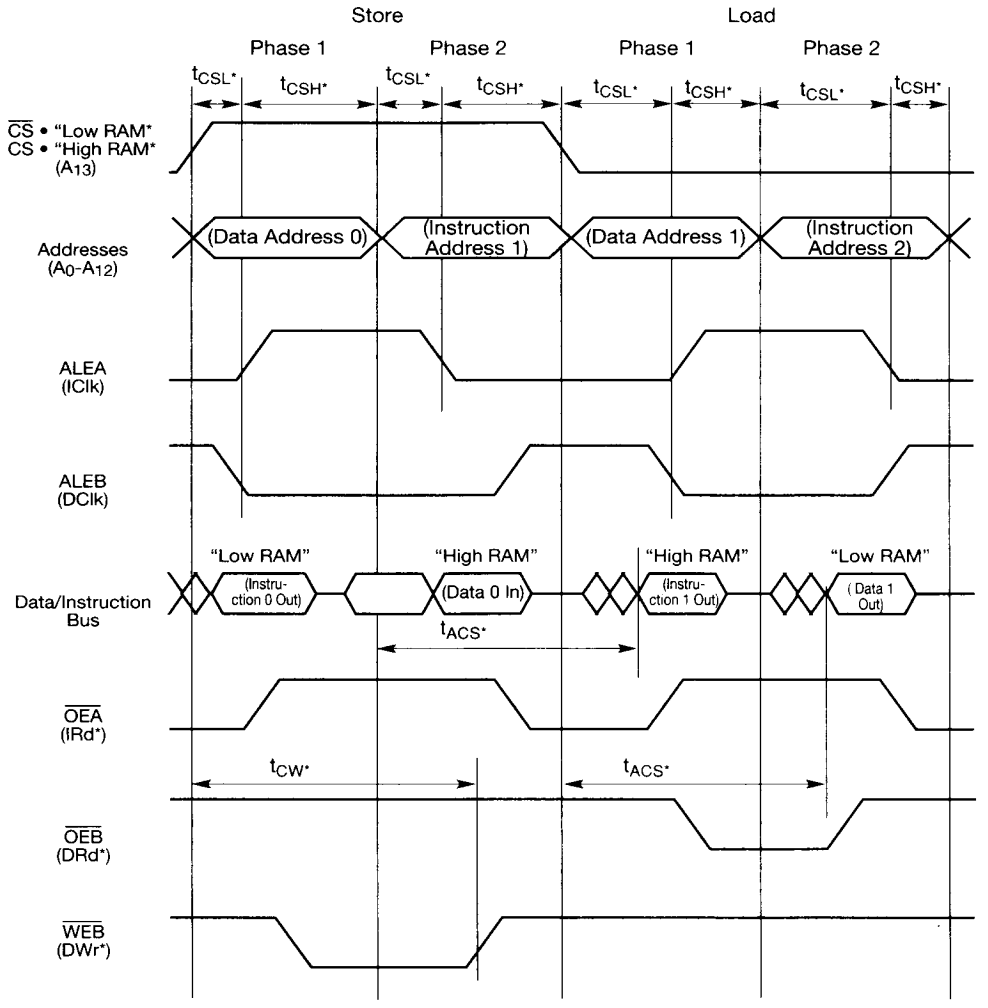
Note: 1. All other non depth-expansion parameters shown in Read Cycle No. 1 still apply, and are not shown for simplicity.

Write Cycle No. 1 ($\overline{CS}$ = Low, CS, $\overline{WEA}$ = High)



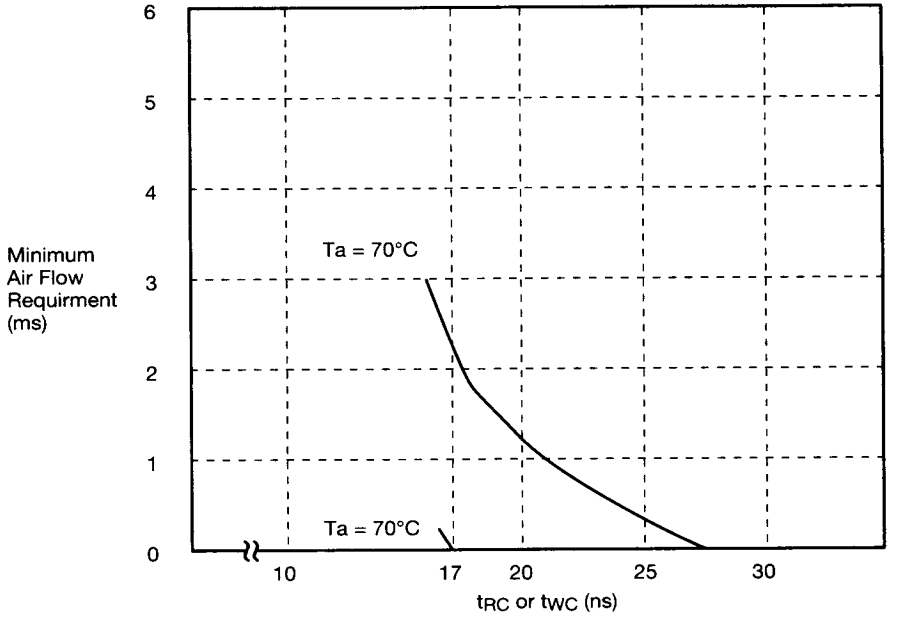
Notes:
1. All timing parameters are measured with output Load A unless otherwise noted.
2. Write cycle time refers to write operations with current addresses applied to a transparent (high) latch.
3. Transition is measured ± 200 mV from steady state voltage with output Load B for t_{OLZ} and t_{OHZ}. These parameters are sampled and not 100% tested.

Write Cycle No. 2 ($\overline{WEA}$ = High) (Store-Load Sequence of Two Depth-Expanded HM62A2016's)



Note: 1. All other non depth-expansion parameters shown in Write Cycle No. 1 still apply, and are not shown for simplicity.

Air Flow Requirements



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