HM62C3232 Series

Preliminary

32K x 32 bits Synchronous Fast Static RAM With Burst Counter and Pipelined Data Output

HITACHI

Rev. 0.2
Feb. 28, 1995

Features

- Single 3.3V power supply (LVTTL)
- Fast clock access times: 8/9/12 ns (max)
- Address data pipeline capability
- Internal input registers (Address, Data, Control)
- Internal data output registers
- Internal self-timed write cycle
- ADSP, ADSC and ADV burst control pins (Supports interleaving)
- Asynchronous output enable controlled Three-state outputs
- Individual byte write control and global write
- Power down state via ZZ
- Common data inputs and data outputs
- High board density 100-lead LQFP package

Ordering Information

Type No.	Access Time	CPU Clock Rate	Package
HM62C3232FP-8	8 ns	66 MHZ	LQFP 100 pin (FP-100H)
HM62C3232FP-9	9 ns	60 MHZ	
HM62C3232FP-12	12 ns	50 MHZ	

Pin Descriptions

(See Detailed Pin Descriptions)

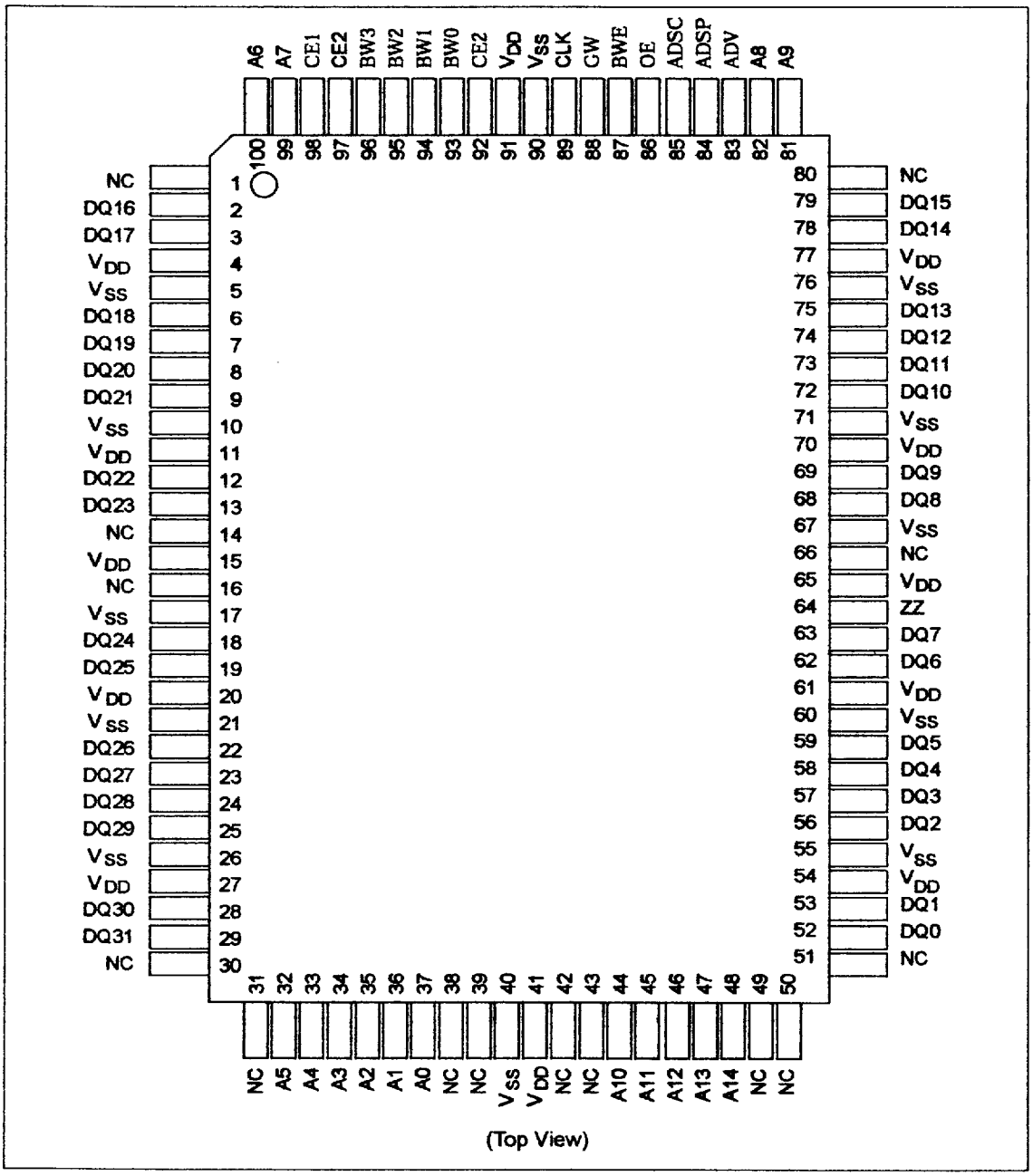
Pin name	Type	Function
A0 to A14	Input	Address inputs
BW0, BW1 BW2, BW3	Input	Byte write enables BW0 controls DQ0 - DQ7 BW1 controls DQ8 - DQ15 BW2 controls DQ16 - DQ23 BW3 controls DQ24 - DQ31
GW	Input	Global write
BWE	Input	Byte write enable
CLK	Input	Clock
CE1	Input	Enable
CE2, CE2	Input	Chip enable
OE	Input	Output enable
ADV	Input	Address advance
ADSP	Input	Address status processor
ADSC	Input	Address status controller
ZZ	Input	Power down
NC	–	No connection
DQ0 to DQ31	Input/Output	
V_{DD}	Supply	Power supply
V_{SS}	Supply	Ground

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

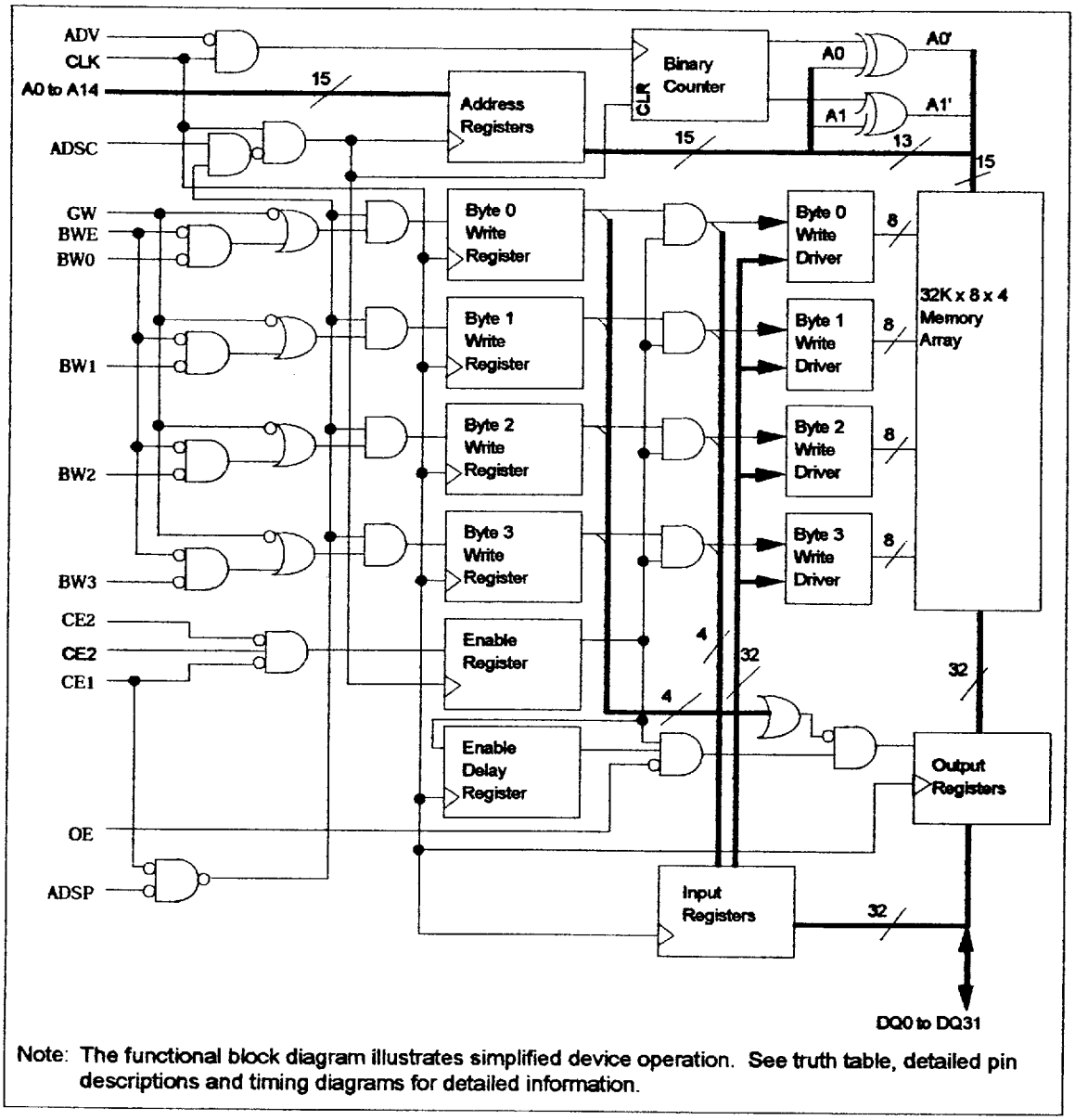
ADE-203-290(B)(Z)

Pin Assignment



(Top View)

Block Diagram



Note: The functional block diagram illustrates simplified device operation. See truth table, detailed pin descriptions and timing diagrams for detailed information.

Synchronous Truth Table

Operation	Address	CE1	CE2	CE2	ADSP	ADSC	ADV	Write	OE	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Notes: 1. H means logic HIGH, L means logic LOW. X means H or L. Write = L means any one or more byte write enable signals (BW0, BW1, BW2 or BW3) and BWE are LOW or GW is LOW. Write = H means all byte write enable signals and GW are HIGH.
2. BW0 enables write to Byte0 (DQ0 to DQ7). BW1 enables write to Byte1 (DQ8 to DQ15). BW2 enables write to Byte2 (DQ16 to DQ23). BW3 enables write to Byte3 (DQ24 to DQ31).
3. All inputs except OE must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, OE must be HIGH before the input data required setup time and hold HIGH throughout the input data hold time.
6. ADSP = LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE LOW or GW LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

Asynchronous Truth Table

Operation	ZZ	OE	I/O Status
Read	L	L	Data out
Read	L	H	High-Z
Write	L	X	High-Z, Data in
Deselect	L	X	High-Z
Power down (Snooze)	H	X	High-Z

Note: H means logic HIGH. L means logic LOW. X means H or L.

Partial Truth Table for Writes

Operation	GW	BWE	BW0	BW1	BW2	BW3
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 0	H	L	L	H	H	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Note: H means logic HIGH. L means logic LOW. X means H or L.

Interleave Sequence Table

Items	A14 to A2	Sequence 1 (A1, A0)	Sequence 2 (A1, A0)	Sequence 3 (A1, A0)	Sequence 4 (A1, A0)
External address	A14 to A2	0 0	0 1	1 0	1 1
1st internal address	A14 to A2	0 1	0 0	1 1	1 0
2nd internal address	A14 to A2	1 0	1 1	0 0	0 1
3rd internal address	A14 to A2	1 1	1 0	0 1	0 0

Note: Each Sequence wraps around to its initial state upon completion.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Voltage on any pins relative to V_{SS} (Except V_{DD})	V_T	–0.5 to V_{DD} +0.5	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage (operating voltage range)	V_{DD}	3.1	3.5	V	
Supply voltage to V_{SS}	V_{SS}	0.0	0.0	V	
Input high voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	0.8	V	1

Note: 1. –2.0 V for undershoot pulse width ≤ tcyc min / 2.

DC and Operating Characteristics (Ta = 0 to +70°C, V_{DD} = 3.3 V ± 5%, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	±2.0	µA	All inputs V_{IN} = V_{SS} to V_{DD}
Output leakage current	I_{LO}	—	±2.0	µA	$\overline{OE}$ = V_{IH}, Vout = V_{SS} to V_{DD}
Supply current	I_{DD}	—	200	mA	Device selected Iout = 0mA, all inputs = V_{IH} or V_{IL}, cycle time = t_{cyc} min.
Standby current	I_{SB}	—	25	mA	Device deselected all inputs = fixed and all inputs ≥ V_{DD} - 0.2 V or ≤ 0.2 V cycle time = t_{cyc} min.
	I_{SBZZ}	—	5	mA	ZZ ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1.0 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	Cin	—	4	5	pF
Input/Output capacitance	$C_{I/O}$	—	7	8	pF

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{DD} = 3.3 ± 5%, V_{SS} = 0 V, unless otherwise noted)

Parameter	Symbol		HM62C3232 -8		-9		-12		Unit	Notes
	standard	Alternate	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	16.7	—	20	—	ns	
Clock Access Time	t_{KHQV}	t_{ACK}	—	8	—	9	—	12	ns	
Output Enable to Output valid	t_{GLQV}	t_{OE}	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	t_{CLZ}	2	—	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{COH}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQZ}	t_{OLZ}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	2	6	ns	1
Clock High to Q High-Z	t_{KHQZ}	t_{CHZ}	—	6	—	6	—	6	ns	1
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	5	—	6	—	ns	
Setup Times :			2.5	—	2.5	—	3	—	ns	2, 3
Address	t_{AVKH}	t_{SA}								
Address Status	t_{ADSVKH}	t_{SADS}								
Input Data	t_{DVKH}	t_{SD}								
Write	t_{WVKH}	t_{SW}								
Address Advance	t_{ADVVK}	t_{SADV}								
Chip Enable	t_{EVKH}	t_{SCE}								
Hold Times :			0.5	—	0.5	—	0.5	—	ns	2, 3
Address	t_{KHAX}	t_{HA}								
Address Status	t_{KHADSX}	t_{HADS}								
Input Data	t_{KHDX}	t_{HD}								
Write	t_{KHWX}	t_{HW}								
Address Advance	t_{KHADVX}	t_{HADV}								
Chip Enable	t_{KHEX}	t_{HCE}								
ZZ Standby		t_{ZZS}	6	—	6	—	6	—	ns	5, 6
ZZ Recovery		t_{ZZREC}	6	—	6	—	6	—	ns	5

Notes: 1. Transition is measured ± 200mV from steady-state voltage with load of FigureB. This parameter is sampled.
2. A READ cycle is defined by byte write enables all HIGH or ADSP LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and ADSP HIGH for the required setup and hold times.
3. This is a synchronous device. All address must meet the specified setup and hold times for all rising edges of CLK when either ADSP or ADSC is LOW and chip enabled. All other Synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either ADSP or ADSC is LOW) to remain enabled .
4. OE is a " H or L " when a byte write enable is sampled LOW.
5. During the cycle when transition of ZZ from high to low or from low to high occurs, ADSP, ADSC, BWE, GW and BWI must be high at its rising edge of CLK.
6. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

Test Conditions

- Input Timing Measurement Reference Level: 1.4 V
- Input Pulse Levels: 0 to 2.8 V
- Input Rise and Fall Time: 2 ns
- Output Timing Reference Level: 1.4 V
- Output Load: See Figure A unless otherwise noted

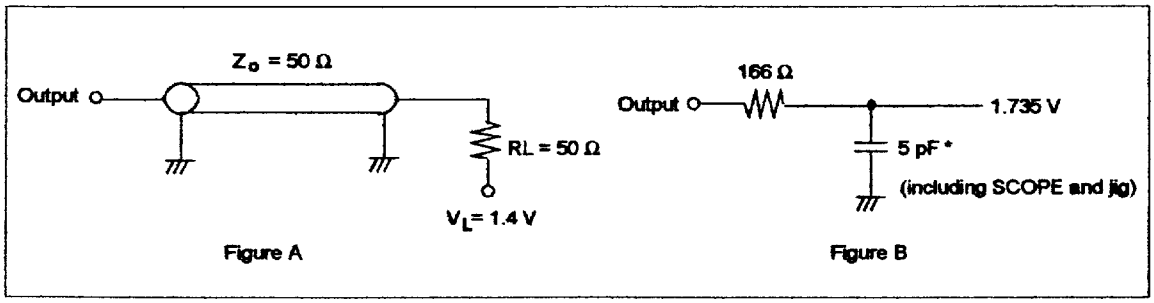
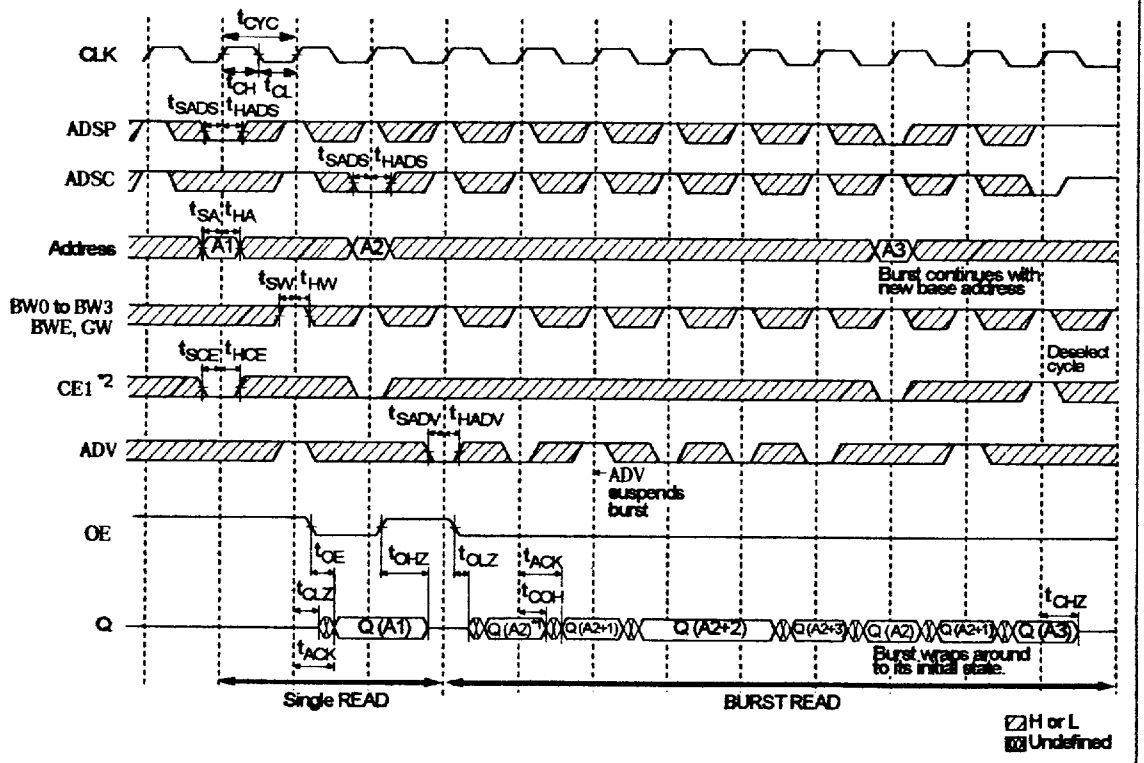


Figure A Figure B

Timing Waveforms

Example of Read Timing

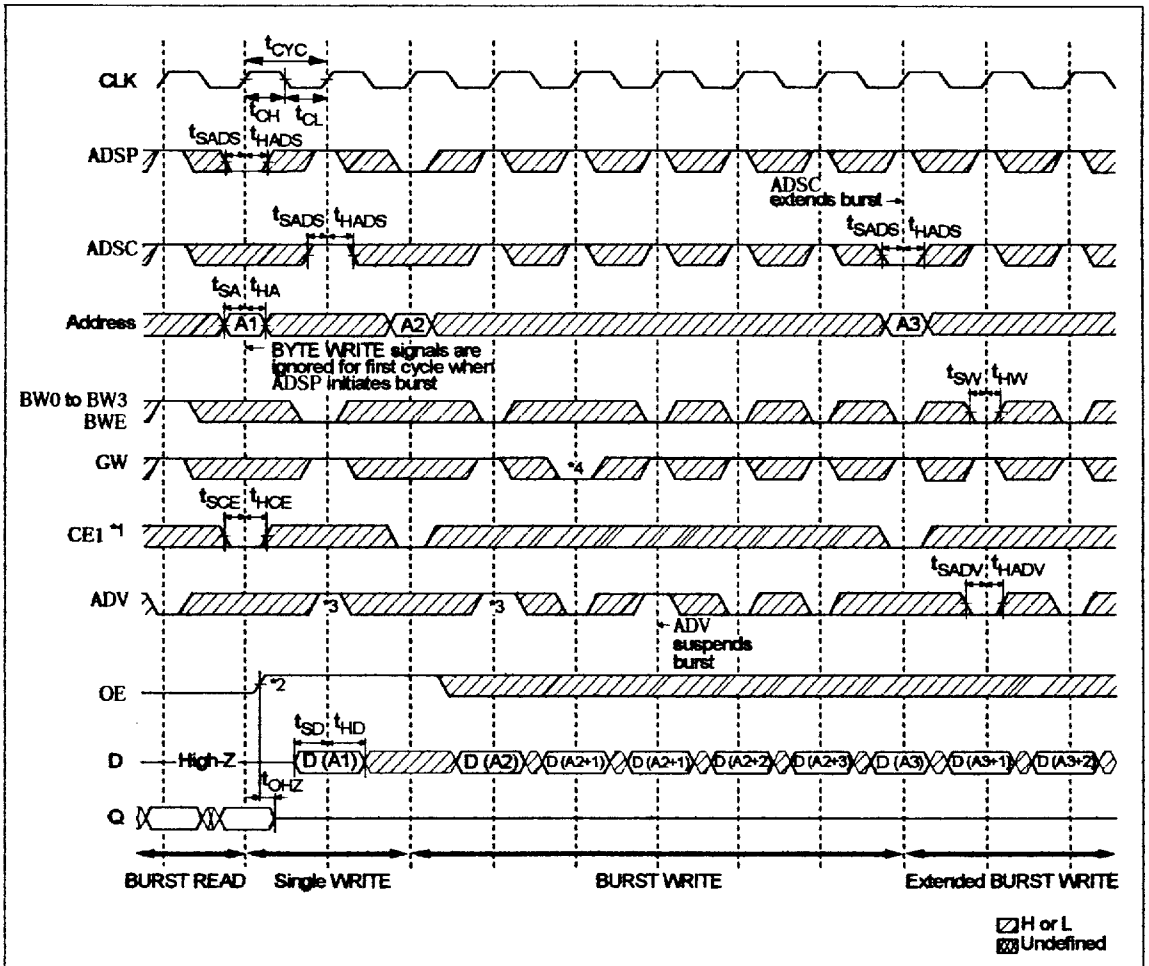


Notes: 1. Q (A2) refers to output from address A2. Q (A2+1) refers to output from next internal burst address following A2.

2. CE2 and CE2 have timing identical to CE1. On this diagram, when CE1 is LOW, CE2 is LOW and CE2 is HIGH. When CE1 is HIGH, CE2 is HIGH and CE2 is LOW.

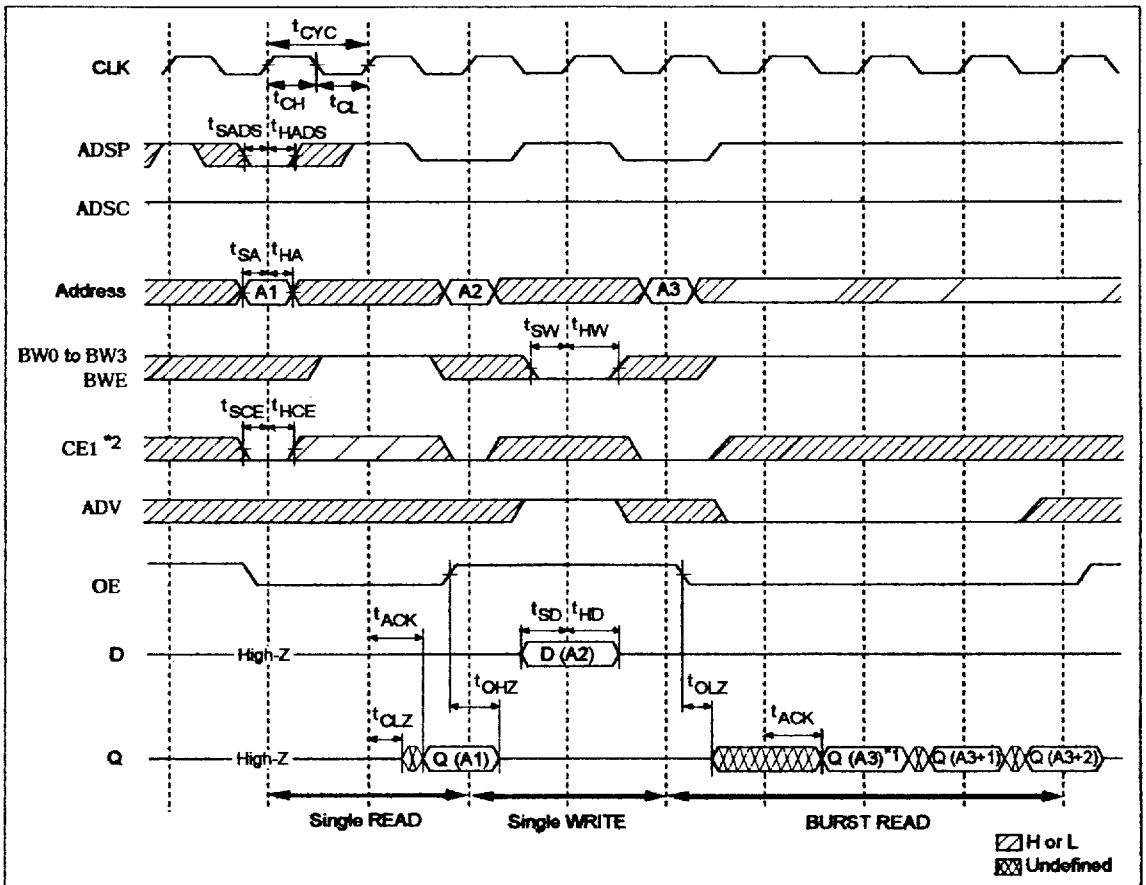
3. ZZ is LOW.

Example of Write Timing



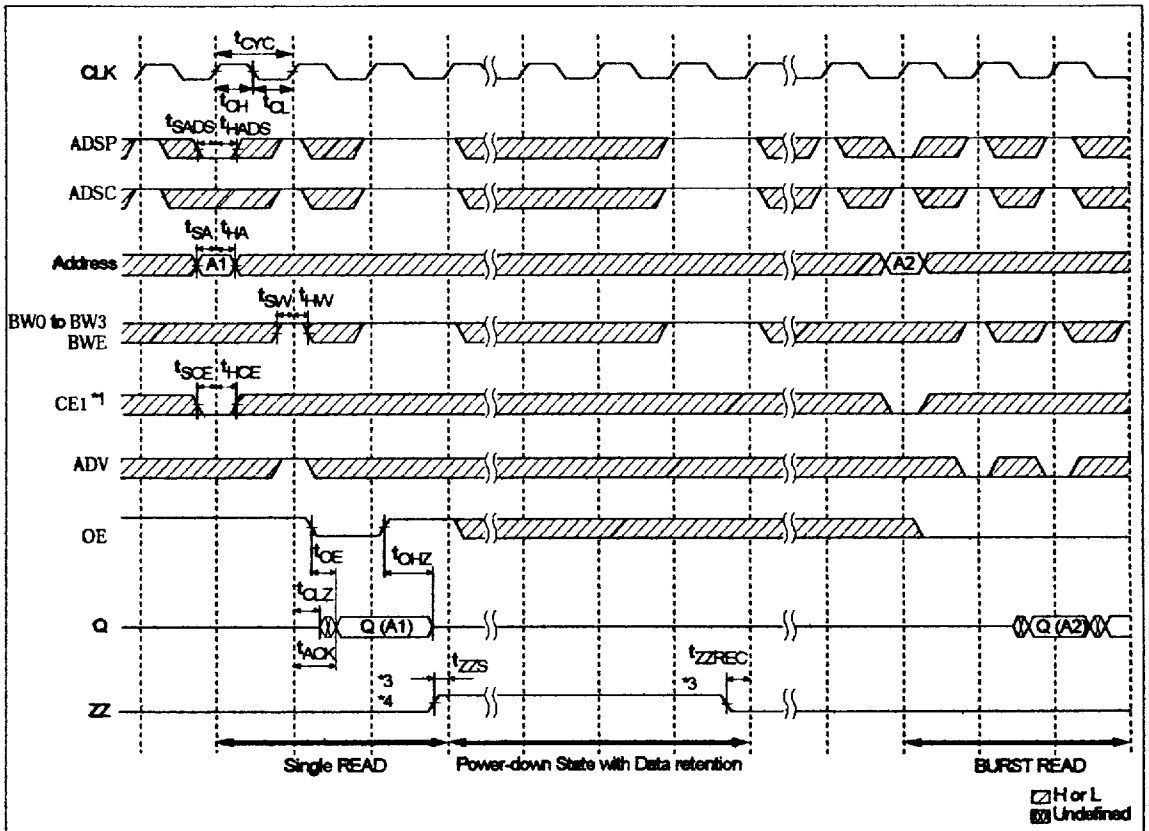
Notes: 1. CE2 and CE2 have timing identical to CE1. On this diagram, when CE1 is LOW, CE2 is LOW and CE2 is HIGH. When CE1 is HIGH, CE2 is HIGH and CE2 is LOW.
2. OE must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. ADV must be HIGH to permit a WRITE to the loaded address.
4. Full width WRITE can be initiated by GW is LOW or GW is HIGH and BWE, BW0 to BW3 are LOW.

Example of Read/Write Timing



Notes: 1. Q (A3) refers to output from address A3. Q (A3+1) refers to output from next internal burst address following A3.
2. CE2 and CE2 have timing identical to CE1. On this diagram, when CE1 is LOW, CE2 is LOW and CE2 is HIGH. When CE1 is HIGH, CE2 is HIGH and CE2 is LOW.
3. GW is HIGH. ZZ is LOW.

Example of Power-down State Timing



Notes: 1. CE2 and CE2 have timing identical to CE1. On this diagram, when CE1 is LOW, CE2 is LOW and CE2 is HIGH. When CE1 is HIGH, CE2 is HIGH and CE2 is LOW.

2. GW is HIGH.

3. During the cycle when transition of ZZ from high to low or from low to high occurs, ADSP, ADSC, BWE, GW and BWi must be high at its rising edge of CLK.

4. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

Detailed Pin Descriptions

LQFP Pin Number(s)	Symbol	Type	Description
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0 - A14	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times around the rising edge of CLK.
93, 94, 95, 96	BW0, BW1 BW2, BW3	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. BW0 controls DQ0 to DQ7. BW1 controls DQ8 to DQ15. BW2 controls DQ16 to DQ23. BW3 controls DQ24 to DQ31. Data I/O are tri-stated if any of these four inputs are LOW.
88	GW	Input	Synchronous Global Write: This active LOW input allows a full 32 bit Write to occur independent of the BWE and BWi lines and must meet the setup and hold times around the rising edge of CLK. System must connect pin to V_{DD} when not used.
87	BWE	Input	Synchronous Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK. System must connect pin to V_{SS} when not used.
89	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	CE1	Input	Synchronous Chip Enables: This active LOW input is used to enable the device and conditions internal use of ADSP. This input is sampled only when a new external address is load.
92	CE2	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input sampled only when a new external address is load. This input can be used for memory depth expansion.
86	OE	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.

Detailed Pin Descriptions (cont.)

LQFP Pin Number(s)	Symbol	Type	Description
83	ADV	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait status to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an ADSP cycle is initiated if a write cycle is desired (to ensure use of correct address).
84	ADSP	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ performed using the new address, independent of the byte write enables and ADSC but dependent upon CE2 and CE2. ADSP is ignored if CE1 is HIGH. Power-down state is entered if CE2 is HIGH or CE2 is LOW.
85	ADSC	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enabled are inactive.
1, 14, 16, 30, 31, 38, 39, 42, 43,49, 50, 51, 66, 80	NC	—	No Connect: These signals are internally not connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ0 to DQ31	Input/ Output	SRAM Data I/O: Byte 0 is DQ0 to DQ7; Byte 1 is DQ8 to DQ15; Byte 2 is DQ16 to DQ23; Byte 3 is DQ24 to DQ31. Input data must meet setup and hold times around the rising edge of CLK.
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{DD}	Supply	Power Supply: +3.3V ± 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND
64	ZZ	Input	Asynchronous Power down (Snooze): This active HIGH input enables SRAM to enter a Power down (Snooze) state with data retention. During Snooze state, data retention is guranteed. At this time, internal state of the SRAM is not preserved. After Snooze state, SRAM must be initiated with ADSP or ADSC using a new external address. Must be connected to V_{SS} in systems that do not use ZZ feature.