

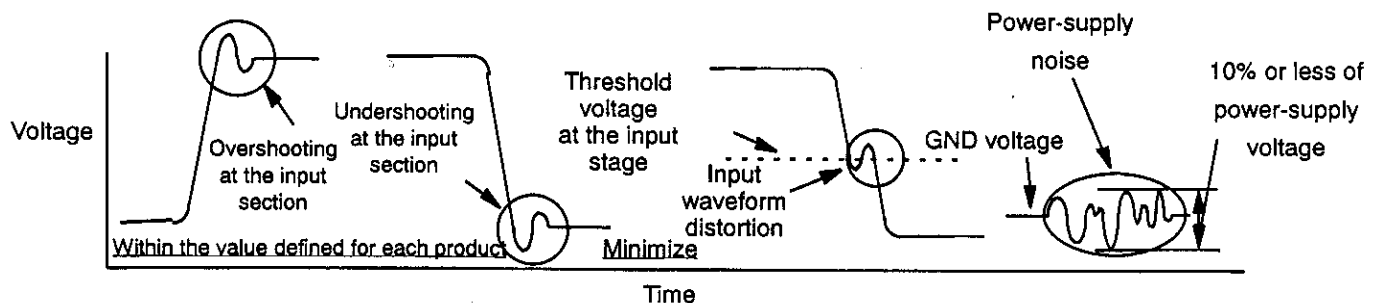
# HITACHI SEMICONDUCTOR TECHNICAL UPDATE

|                     |                                                                                                                                                                                                                                |                |               |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------|
| DATE                | 30 July 2001                                                                                                                                                                                                                   | No.            | TN-M62-090A/E |
| THEME               | Instructions for Using SRAM Devices                                                                                                                                                                                            |                |               |
| CLASSIFICATION      | <input type="checkbox"/> Spec. change <input checked="" type="checkbox"/> Limitation on Use <input type="checkbox"/> Others<br><input type="checkbox"/> Supplement of Documents <input type="checkbox"/> Product line addition |                |               |
| PRODUCT NAME        | All SRAM Products                                                                                                                                                                                                              | Lot            | All lots      |
| REFERENCE DOCUMENTS | Hitachi IC Memory Data Book Mar. 2001<br>ADE-403-001Q                                                                                                                                                                          | Effective Date |               |
|                     |                                                                                                                                                                                                                                | Permanent      |               |

As SRAM products become faster, various design margins are becoming difficult to secure. There is an increased possibility of the disruption of normal operation by noise in the input signal or from the power supply. Before using our SRAM products, please note the following points which you may recognize by reading the notes in the Hitachi IC Memory Data Book on the Instructions for Using Memory Devices. This will help you to prevent abnormal operation of the SRAM.

## 1. Precaution

When operating a semiconductor product, input-signal noise or power-supply noise may prevent the normal operation of the product and cause a malfunction of some kind. Input-signal noise includes overshooting, undershooting, and distortion of the input waveform near the threshold voltage. Make sure that the values of any overshooting or undershooting are within the specified values for the product as described in Hitachi's Data Book. Minimize the input waveform's distortion near the threshold voltage. The level of power-supply noise should be 10% or less than 10% of the peak-to-peak standard power-supply voltage.



## 2. Countermeasures

### (1) Minimize overshooting, undershooting, and distortion of input waveform

- Place resistors (50  $\Omega$  or less) in series on each input
- Place terminal resistors on the ends of input line
- Make good choices in terms of pattern layout and wiring methods
- Suppress instabilities of reference voltages (GND level etc.)

### (2) Reduce power-supply noise

- Place a bypass capacitor (0.1 to 0.01  $\mu$ F) at the shortest possible distance from the device
- Make good choices in terms of pattern layout and wiring methods

(3) When replacing an existing product, please prepare a board that suits the product that is now on the market in terms of the decreased operational margins that go along with the higher speeds of product operation.