HM62V16256B Series

4 M SRAM (256-kword × 16-bit)

HITACHI

ADE-203-933 (Z)
Preliminary, Rev. 0.0
June 26, 1998

Description

The Hitachi HM62V16256B is a CMOS static RAM organized 262,144-word × 16-bit. It realizes higher density, higher performance and low power consumption by employing 0.35 µm Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 48 ball chip size package with 0.75 mm ball pitch or 400-mil 44 pin plastic TSOPII is available for high density mounting.

Features

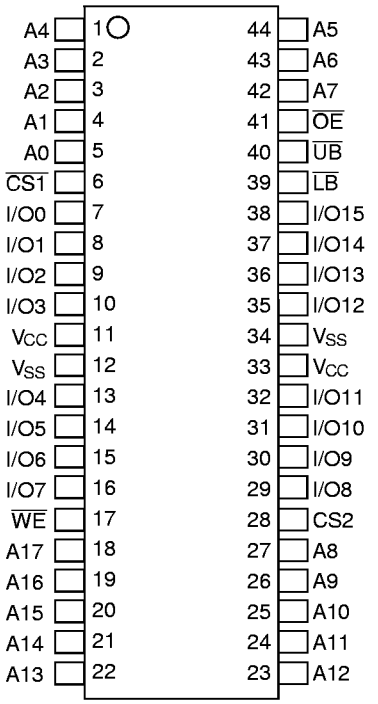
- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 70/85 ns (max)
- Power dissipation:
  - — Active: 15 mW/MHz (typ)
  - — Standby: 1.5 µW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output. Three state output
- Capability of battery backup operation. 2 chip selection for battery backup

Ordering Information

Type No.	Access time	Package
HM62V16256BLTT-7	70 ns	400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB)
HM62V16256BLTT-8	85 ns	
HM62V16256BLTT-7SL	70 ns	
HM62V16256BLTT-8SL	85 ns	
HM62V16256BLBT-7	70 ns	CSP 48-pin (TBT-48)
HM62V16256BLBT-8	85 ns	
HM62V16256BLBT-7SL	70 ns	
HM62V16256BLBT-8SL	85 ns	

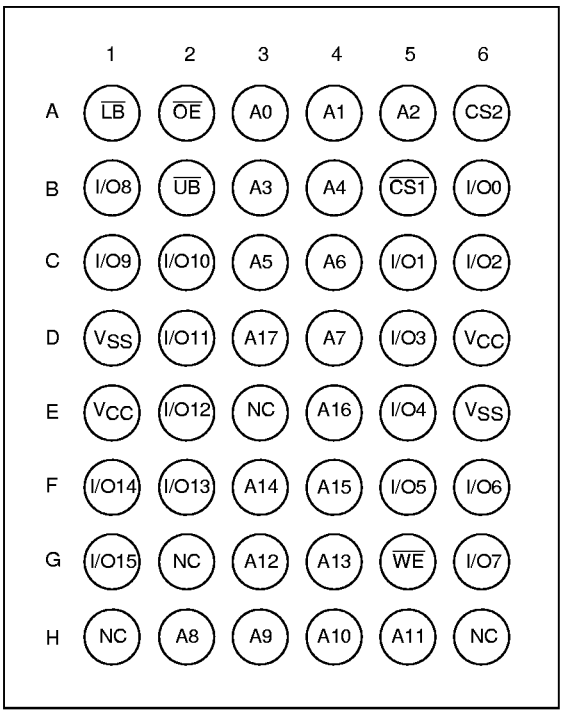
Pin Arrangement

HM62V16256BLTT Series



(Top view)

HM62V16256BLBT Series

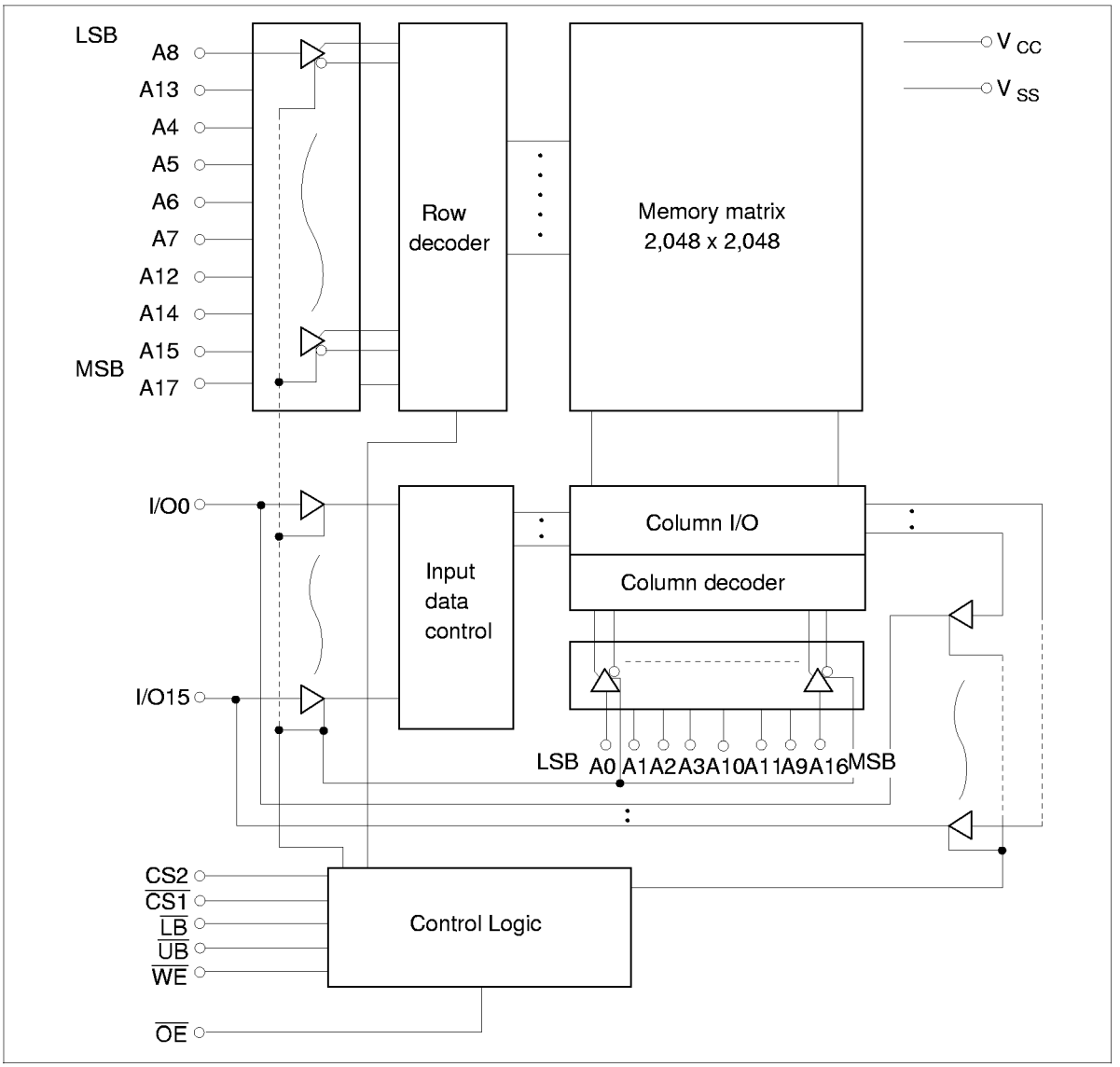


(Top view)

Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{LB}$	Lower byte (I/O0 to 7)
$\overline{UB}$	Upper byte (I/O8 to 15)
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Operation Table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O0 to I/O7	I/O8 to I/O15	Mode	Ref. cycle
H	×	×	×	×	×	High-Z	High-Z	Deselected	Standby
×	L	×	×	×	×	High-Z	High-Z	Deselected	Standby
×	×	×	×	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	×	×	High-Z	High-Z	Output disable	Active
L	H	H	L	H	L	Dout	High-Z	Lower byte read	Active
L	H	H	L	L	H	High-Z	Dout	Upper byte read	Active
L	H	H	L	L	L	Dout	Dout	Word Read	Active
L	H	L	×	H	L	Din	High-Z	Lower byte write	Active
L	H	L	×	L	H	High-Z	Din	Upper byte write	Active
L	H	L	×	L	L	Din	Din	Word write	Active

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	–0.5 to + 4.6	V
Terminal voltage*1	V_T	–0.5*2 to V_{CC} + 0.3*3	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to 85	°C

Notes: 1. Relative to V_{SS}
2. V_T min: –3.0 V for pulse half-width ≤ 30 ns
3. Maximum voltage is 4.6 V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
	V_{IL}	–0.3 *1	—	0.6	V

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V)

Parameter		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, or $\overline{LB}$ = $\overline{UB}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC		I_{CC}	—	—	20	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating power supply current	HM62V16256B-7	I_{CC1}	—	—	70	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	HM62V16256B-8	I_{CC1}	—	—	65		
		I_{CC2}	—	—	15	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC		I_{SB}	—	—	0.3	mA	CS2 = V_{IL}
Standby power supply current (1): DC		I_{SB1}	—	—	20*2	µA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V
		I_{SB1}	—	—	2*3	µA	
Output voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
			—	—	0.2	V	I_{OL} = 100 µA
		V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
			V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L version.
3. This characteristic is guaranteed only for L-SL version.

Capacitance (Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance*1	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.2 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- output timing reference levels: 1.4 V
- Output load (Including scope and jig): 1 TTL + 30 pF (HM62V16256B-7)
  1 TTL + 100 pF (HM62V16256B-8)

Read Cycle

		HM62V16256B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	70	—	85	—	ns	
Address access time	t_{AA}	—	70	—	85	ns	
Chip selection to output valid	t_{CO1}	—	70	—	85	ns	
	t_{CO2}	—	70	—	85	ns	
Output enable to output valid	t_{OE}	—	35	—	45	ns	
$\overline{LB}$, $\overline{UB}$ access time	t_{BA}	—	70	—	85	ns	
Chip selection to output in low-Z	t_{LZ1}	10	—	10	—	ns	2, 3
	t_{LZ2}	10	—	10	—	ns	
$\overline{LB}$, $\overline{UB}$ enable to low-z	t_{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	25	0	25	ns	1, 2, 3
	t_{HZ2}	0	25	0	25	ns	
$\overline{LB}$, $\overline{UB}$ disable to high-Z	t_{BHZ}	0	25	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	25	0	25	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	ns	

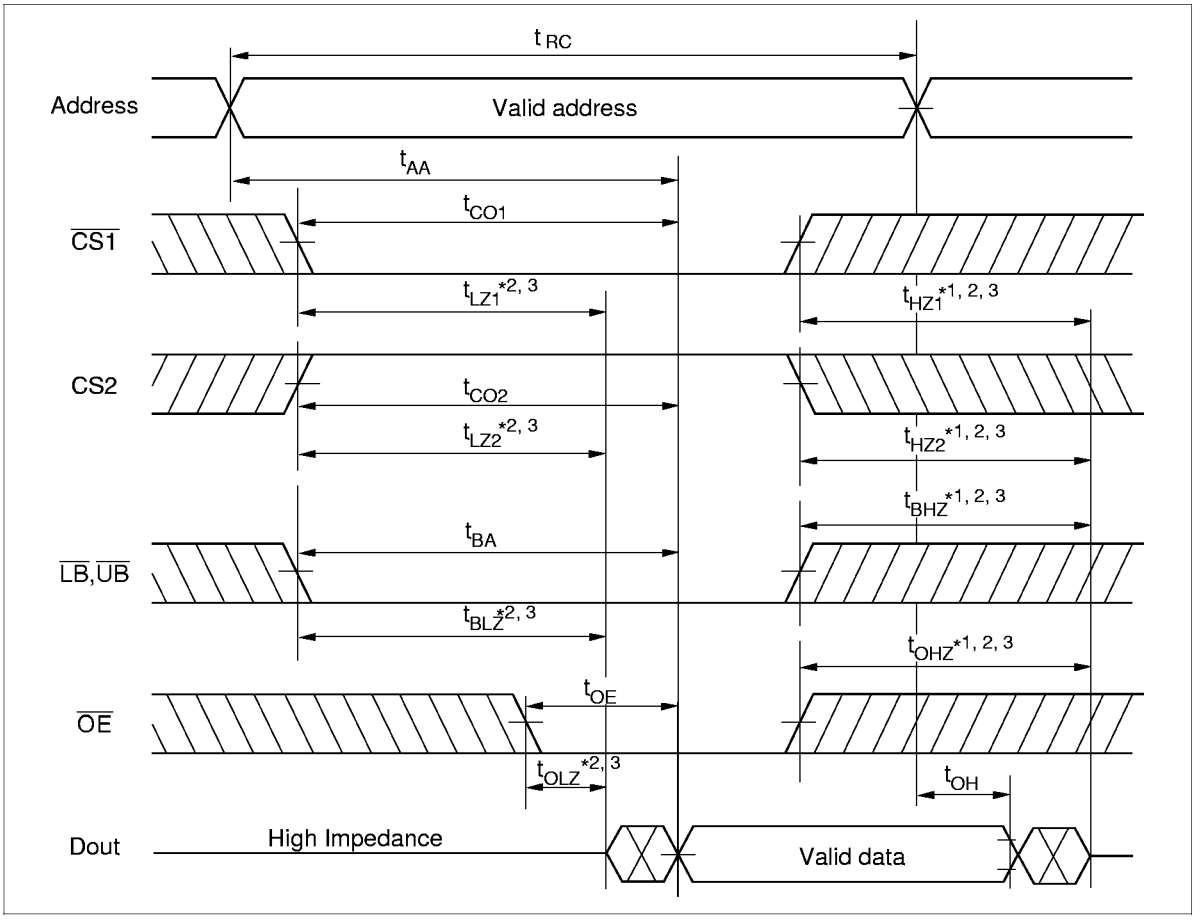
Write Cycle

		HM62V16256B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	70	—	85	—	ns	
Chip selection to end of write	t_{CW}	60	—	70	—	ns	5
Address setup time	t_{AS}	0	—	0	—	ns	6
Address valid to end of write	t_{AW}	60	—	70	—	ns	
$\overline{LB}$, $\overline{UB}$ valid to end of write	t_{BW}	60	—	70	—	ns	
Write pulse width	t_{WP}	55	—	70	—	ns	4
Write recovery time	t_{WR}	0	—	0	—	ns	7
Write to output in high-Z	t_{WHZ}	0	25	0	25	ns	1, 2
Data to write time overlap	t_{DW}	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	25	0	25	ns	1, 2

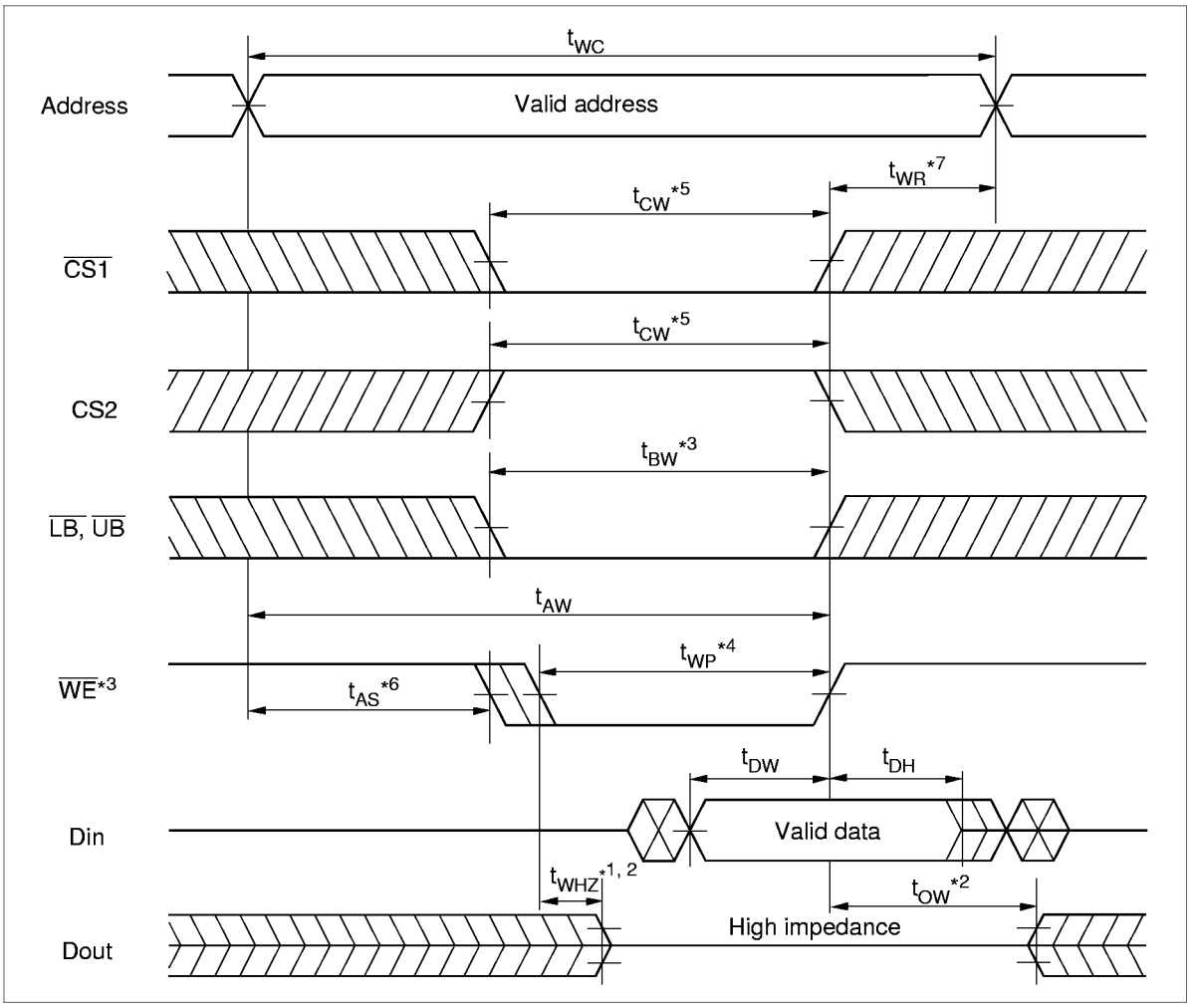
Notes:
1. t_{HZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, a low $\overline{WE}$ and a low $\overline{LB}$ or a low $\overline{UB}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, $\overline{WE}$ going low and $\overline{LB}$ going low or $\overline{UB}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, $\overline{WE}$ going high and $\overline{LB}$ going high or $\overline{UB}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

Timing Waveform

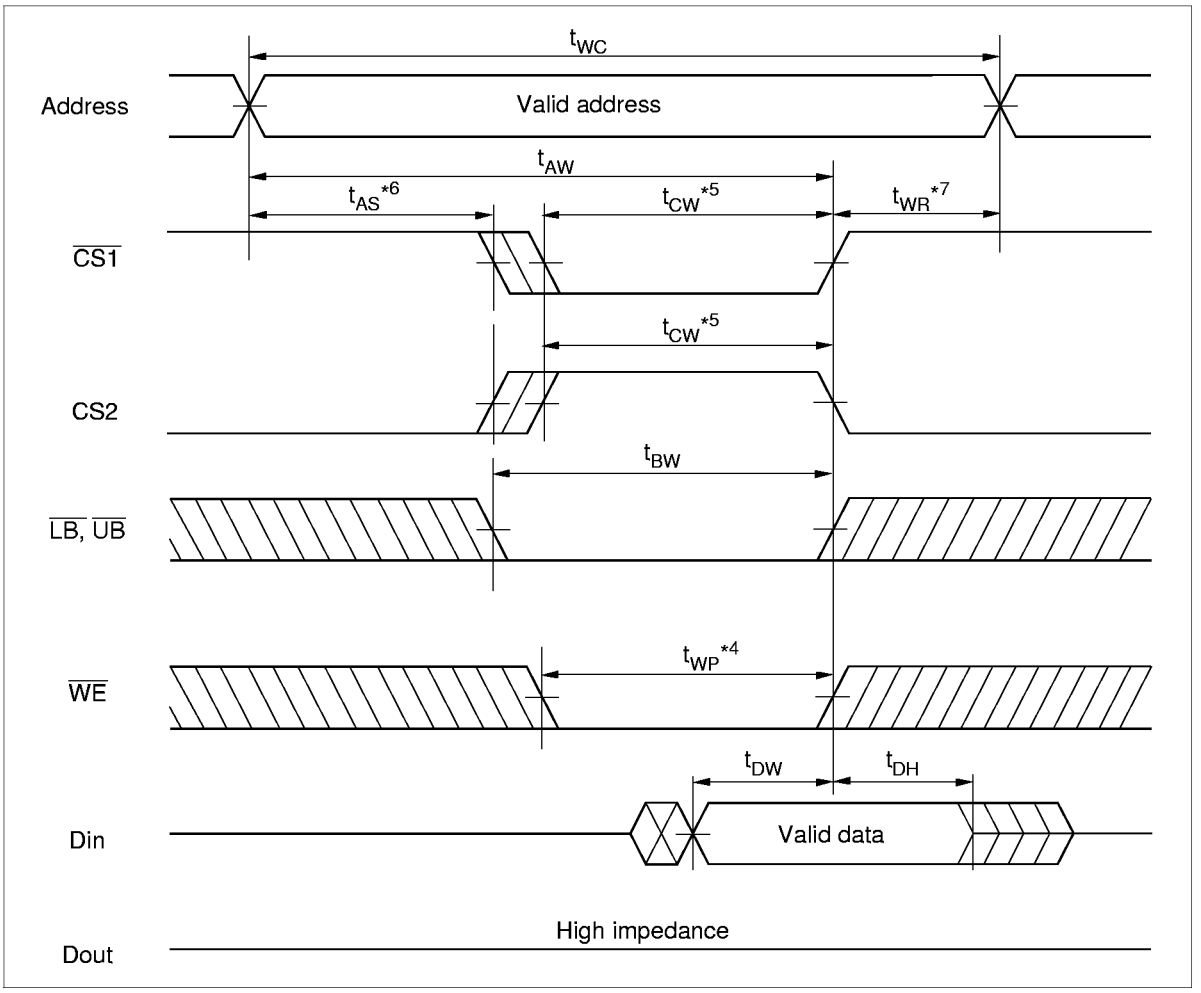
Read Timing Waveform



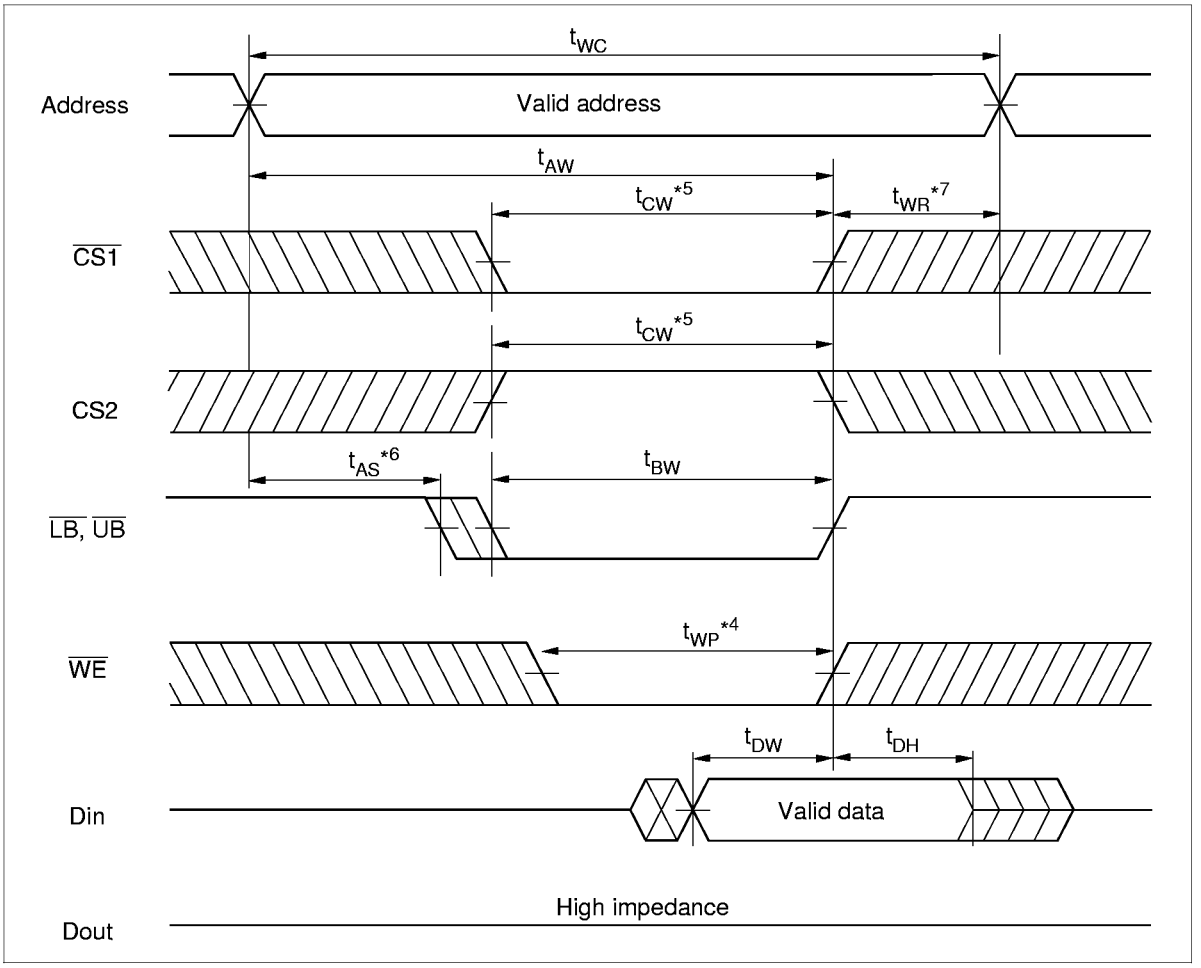
Write Timing Waveform (1) ($\overline{WE}$ Clock)



Write Timing Waveform (2) ($\overline{CS}$ Clock, $\overline{OE}$ = V_{IH})



Write Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Clock, $\overline{OE}$ = V_{IH})



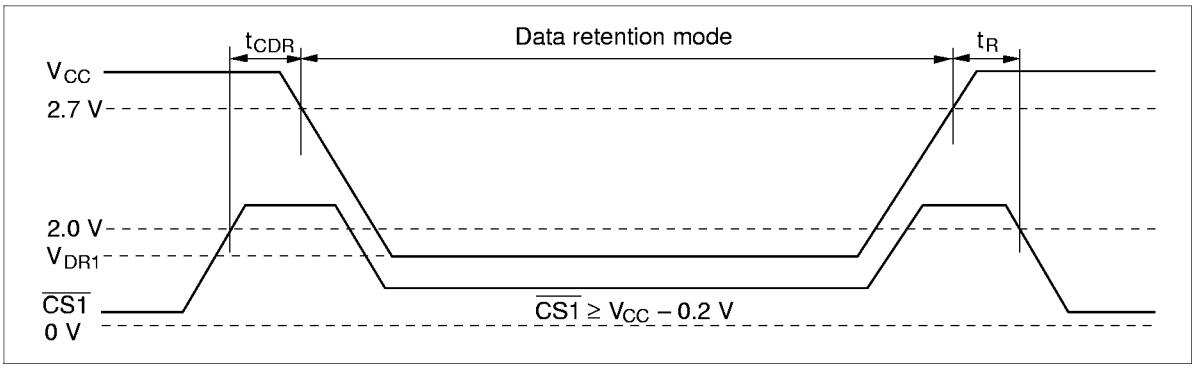
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ*4	Max	Unit	Test conditions*3
V_{CC} for data retention	V_{DR}	2.0	—	—	V	Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≥ V_{CC} – 0.2 V or (3) $\overline{LB}$ = $\overline{UB}$ ≥ V_{CC} – 0.2 V CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≤ 0.2 V
Data retention current	I_{CCDR} (L version)	—	1	10*1	µA	V_{CC} = 3.0 V, Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V or (3) $\overline{LB}$ = $\overline{UB}$ ≥ V_{CC} – 0.2 V CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≤ 0.2 V
	I_{CCDR} (L-SL version)	—	1	1*2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*5	—	—	ms	

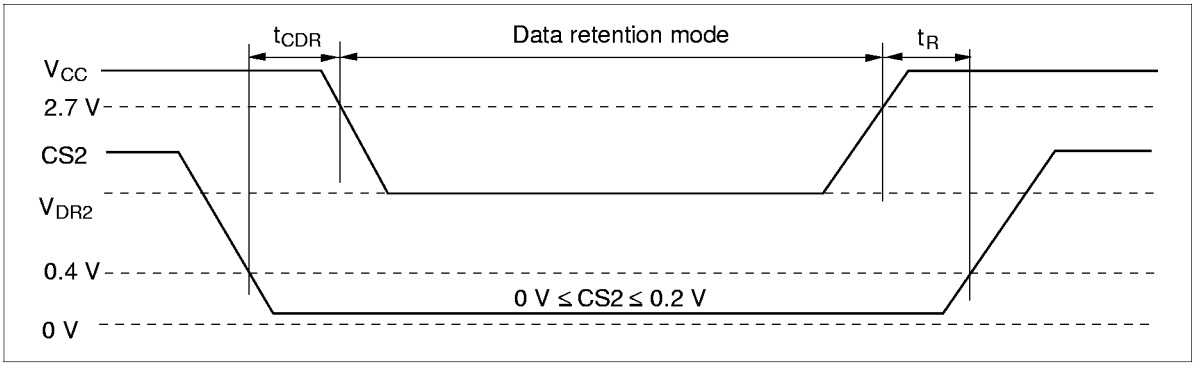
Notes: 1. This characteristic is guaranteed only for L version, TBD µA max. at Ta = 0 to +40°C.

2. This characteristic is guaranteed only for L-SL version, TBD µA max. at Ta = 0 to +40°C.
3. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, $\overline{LB}$, $\overline{UB}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, $\overline{LB}$, $\overline{UB}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$, I/O) can be in the high impedance state.
4. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
5. t_{RC} = read cycle time.

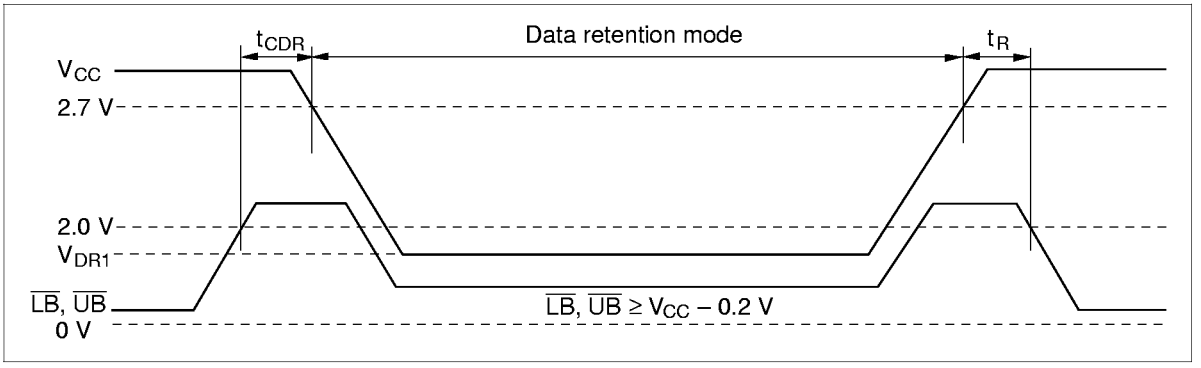
Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)

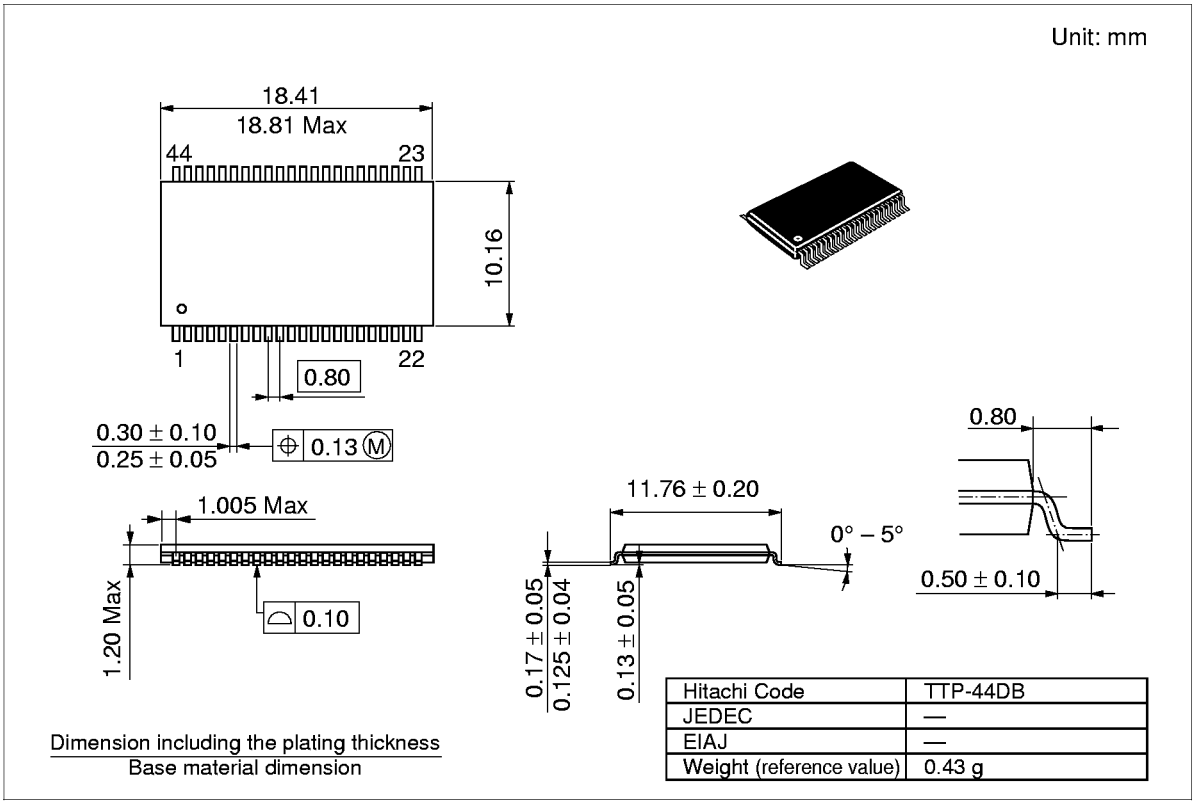


Low V_{CC} Data Retention Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



Package Dimensions

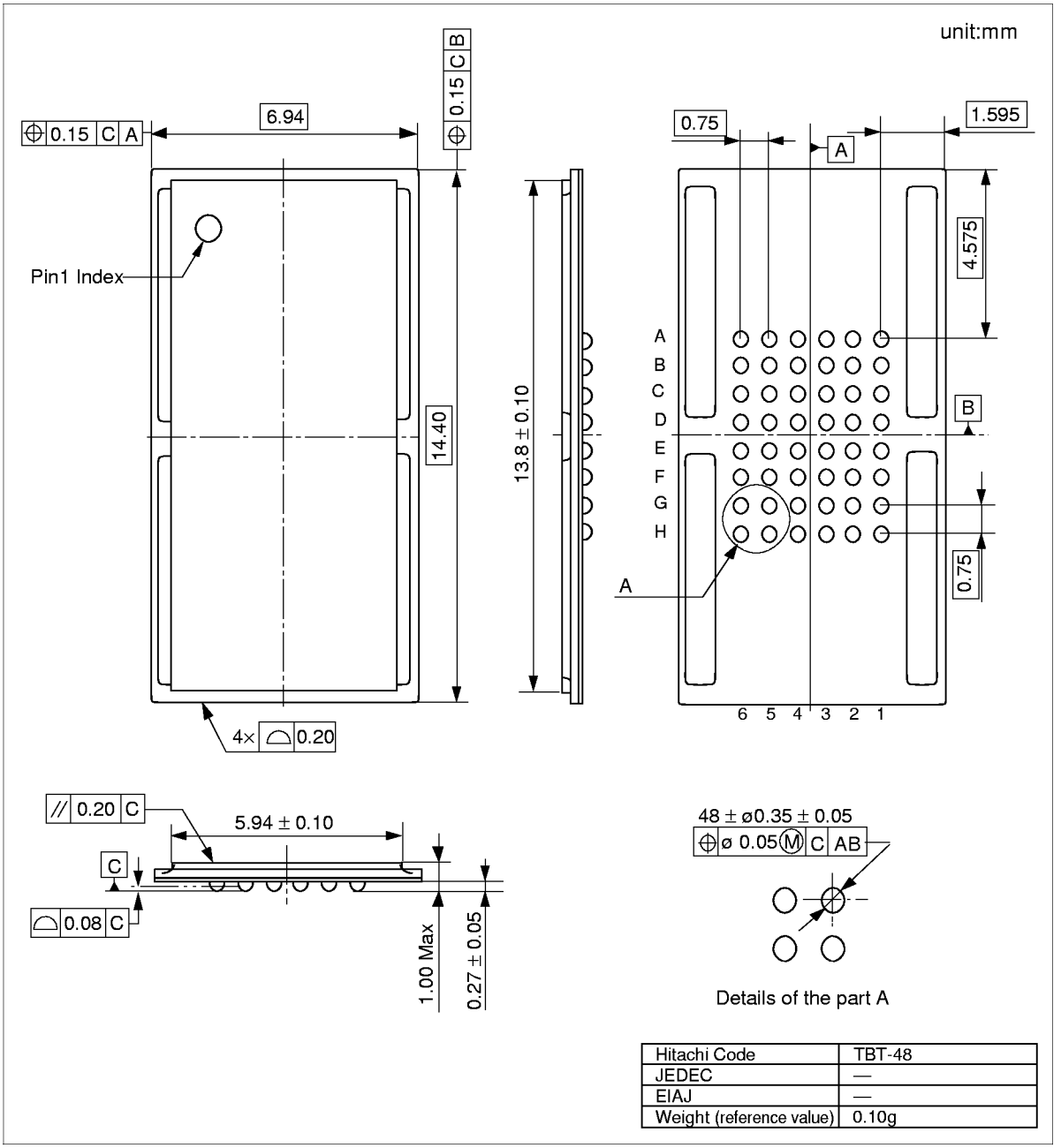
HM62V16256BLTT Series (TTP-44DB) Unit: mm



Hitachi Code	TTP-44DB
JEDEC	—
EIAJ	—
Weight (reference value)	0.43 g

Package Dimensions (cont.)

HM62V16256BLBT Series (TBT-48)



Hitachi Code	TBT-48
JEDEC	—
EIAJ	—
Weight (reference value)	0.10g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA 94005-1897
Tel: <1> (800) 285-1601
Fax: <1> (303) 297-0447

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 26, 1998	Initial issue		