HM62W8127H Series
HM62W9127H Series

Preliminary

131072-word × 8/9-bit High Speed CMOS Static RAM

The HM62W8127H/HM62W9127H is an asyncronous 3.3 V operation high speed static RAM organized as 128 kword × 8/9 bit. It realize high speed access time (25/30/35/45 ns) with employing 0.8 µm CMOS process and high speed circuit designing technology.

It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.

The HM62W8127H/HM62W9127H is packaged in 400-mil 32/36-pin SOJ for high density surface mounting.

Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time 25/30/35/45 ns (max)
- Completely static memory
  — No clock or timing strobe required
- Equal access and cycle times
- Directly CMOS compatible
  — All inputs and outputs
- 400-mil 32/36-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

Ordering Information

Type No.	Access time	Package
HM62W8127HJP-25	25 ns	400-mil 32-pin plastic SOJ (CP-32DB)
HM62W8127HJP-30	30 ns	
HM62W8127HJP-35	35 ns	
HM62W8127HJP-45	45 ns	
HM62W8127HLJP-25	25 ns	
HM62W8127HLJP-30	30 ns	
HM62W8127HLJP-35	35 ns	
HM62W8127HLJP-45	45 ns	
HM62W9127HJP-25	25 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM62W9127HJP-30	30 ns	
HM62W9127HJP-35	35 ns	
HM62W9127HJP-45	45 ns	
HM62W9127HLJP-25	25 ns	
HM62W9127HLJP-30	30 ns	
HM62W9127HLJP-35	35 ns	
HM62W9127HLJP-45	45 ns	

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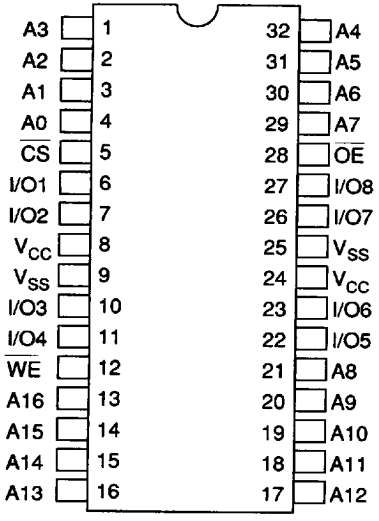
Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

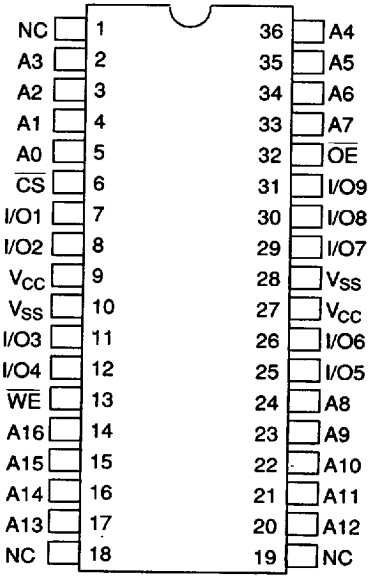
Pin Arrangement

HM62W8127H Series



(Top View)

HM62W9127H Series

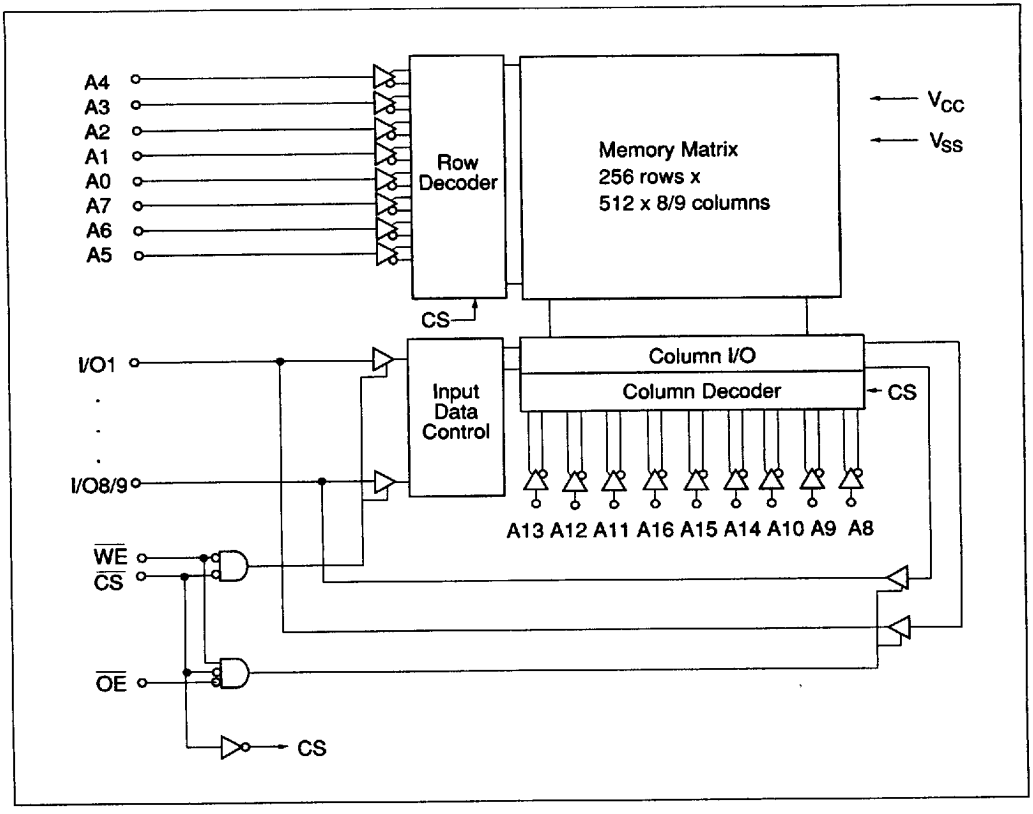


(Top View)

Pin Description

Pin name		
HM62W8127H	**HM62W9127H**	**Function**
A0 – A16	A0 – A16	Address
I/O1 – I/O8	I/O1 – I/O9	Data input/output
$\overline{CS}$	$\overline{CS}$	Chip select
$\overline{WE}$	$\overline{WE}$	Write enable
$\overline{OE}$	$\overline{OE}$	Output enable
V_{CC}	V_{CC}	Power supply
V_{SS}	V_{SS}	Ground
—	NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	–0.5 *1 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: 1. –2.5 V for pulse width (under shoot) ≤ 10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{VE}$	V_{CC} current	I/O	Ref. cycle
H	X	X	I_{SB}, I_{SB1}	High-Z	—
L	H	H	I_{CC}	High-Z	—
L	L	H	I_{CC}	Output	Read cycle
L	X	L	I_{CC}	Input	Write cycle

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*2	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
	V_{IL}	−0.3 *1	—	0.8	V

Note: 1. −2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$V_{I/O}$ = V_{SS} to V_{CC}	1
Operating power supply current	I_{CC}	—	60	100	mA	25 ns cycle, $\overline{CS}$ = V_{IL}, Iout = 0 mA, Other inputs = V_{IH}/V_{IL}	
		—	50	90	mA	30 ns cycle	
		—	45	85	mA	35 ns cycle	
		—	40	80	mA	45 ns cycle	
Standby power supply current	I_{SB}	—	20	40	mA	25 ns cycle, $\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}	
		—	18	35	mA	30 ns cycle	
		—	15	30	mA	35 ns cycle	
		—	13	25	mA	45 ns cycle	
Standby power supply current (1)	I_{SB1}	—	—	1	mA	V_{CC} ≥ $\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or V_{CC} ≥ Vin ≥ V_{CC} – 0.2 V	
		—	—	0.06	mA		L-version
Output voltage	V_{OL1}	—	—	0.2	V	I_{OL1} = 0.1 mA	
	V_{OL2}	—	—	0.4	V	I_{OL2} = 2 mA	
	V_{OH1}	V_{CC} – 0.2	—	—	V	I_{OH1} = –0.1 mA	
	V_{OH2}	2.4	—	—	V	I_{OH2} = –2 mA	

Note: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

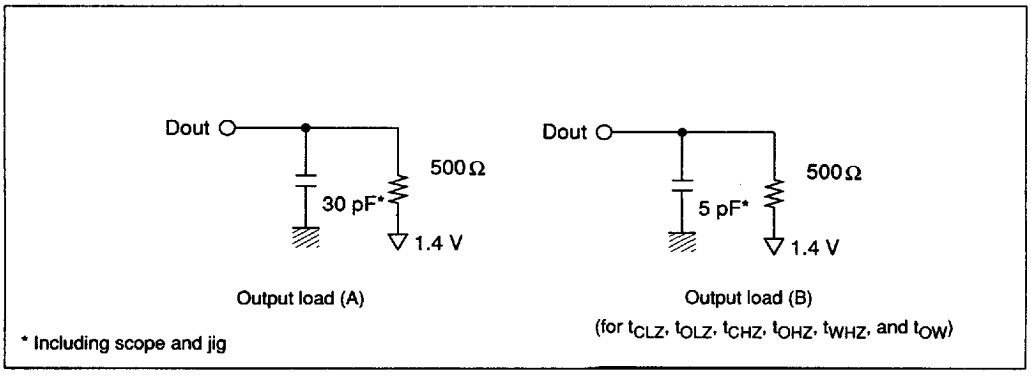
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

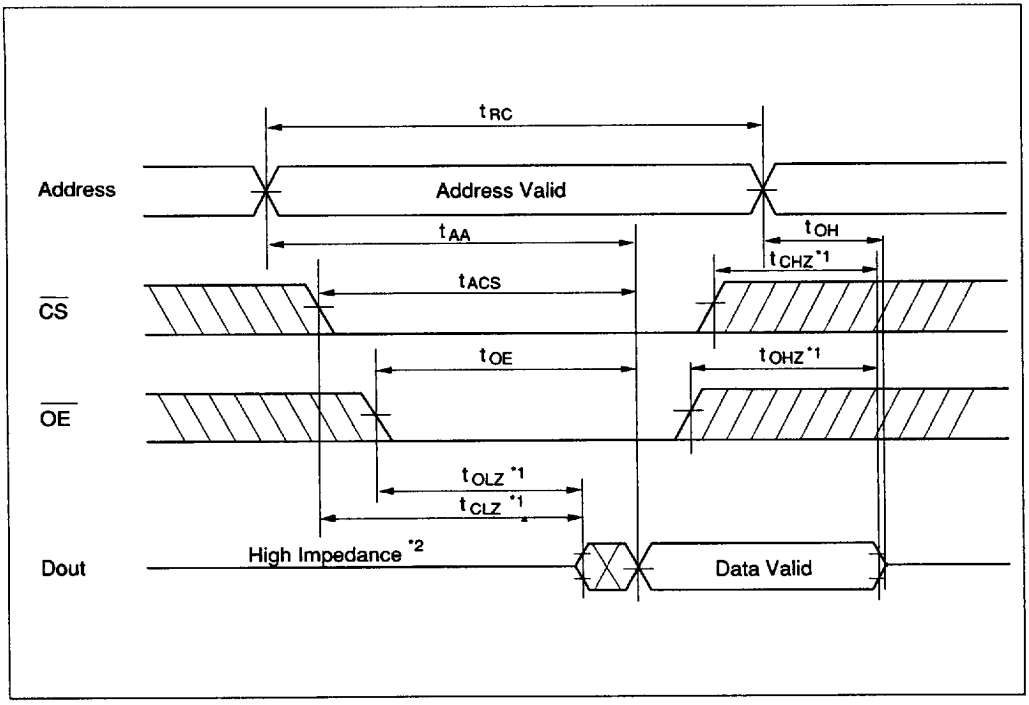
- Input pulse levels: 2.4 V/0.4 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures



Read Cycle

		HM62W8127H/HM62W9127H								
		-25		-30		-35		-45		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Output enable to output valid	t_{OE}	—	15	—	15	—	20	—	25	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip select to output in low-Z	t_{CLZ}	5	—	5	—	5	—	5	—	ns
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	1	—	1	—	ns
Chip deselect to output in high-Z	t_{CHZ}	—	12	—	12	—	12	—	12	ns
Output disable to output in high-Z	t_{OHZ}	—	12	—	12	—	12	—	12	ns

Read Timing Waveform*3



Notes: 1. Transition is measured ±200 mV from steady state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$ and $\overline{OE}$ are low, Dout is low impedance.
3. $\overline{WE}$ is high for read cycle.

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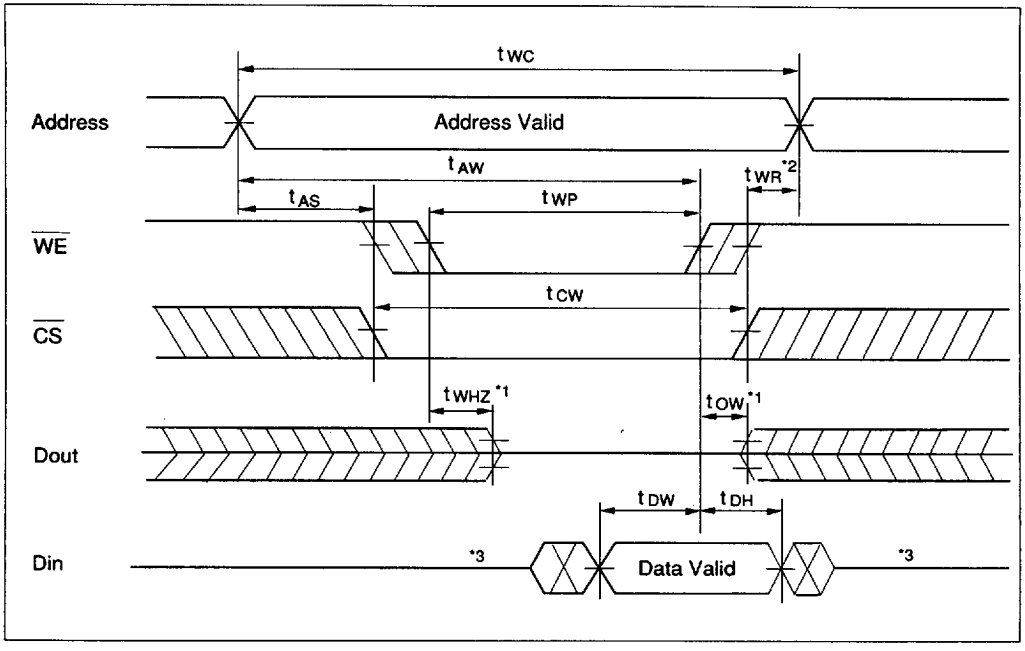
Write Cycle

		HM62W8127H/HM62W9127H								
		-25		-30		-35		-45		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Write cycle time	t_{WC}	25	—	30	—	35	—	45	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	25	—	30	—	ns
Chip select to end of write	t_{CW}	20	—	20	—	25	—	30	—	ns
Write pulse width	t_{WP}	20	—	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns
Data to write time overlap	t_{DW}	15	—	15	—	20	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write disable to output in low-Z	t_{OW}	5	—	5	—	5	—	5	—	ns
Write enable to output in high-Z	t_{WHZ}	—	12	—	12	—	12	—	12	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



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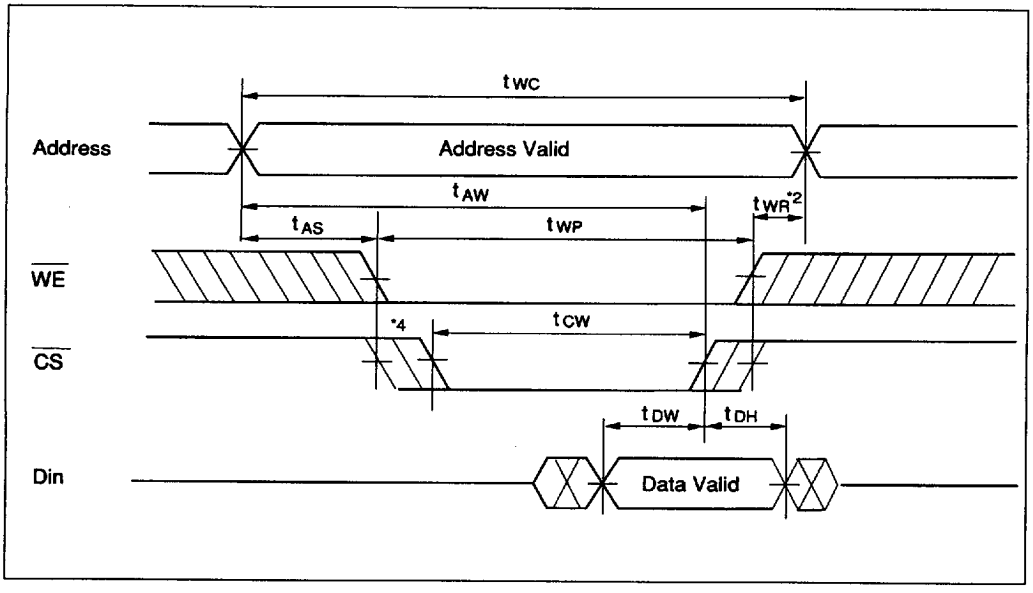
Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes:
1. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampeld and not 100% tested.
2. $\overline{WE}$ must be high during transition except when the device is disabled with $\overline{CS}$.
3. If $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.

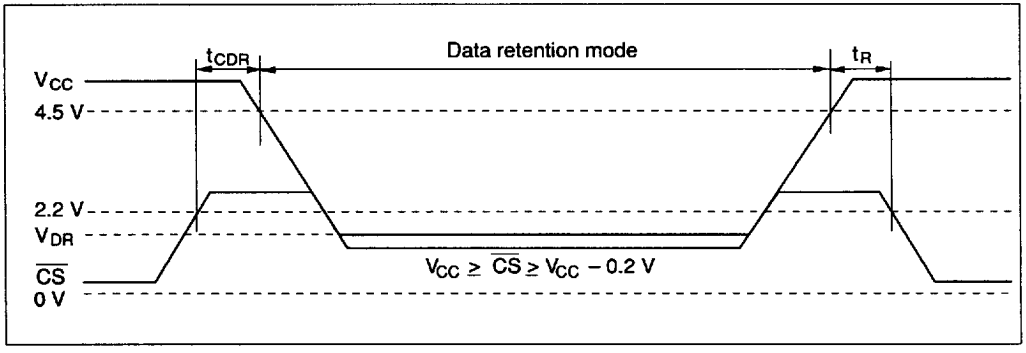
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0 V \leq Vin \leq 0.2$ V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



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