HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	Memory			No	TN-M62-112A/E	Rev	1
THEME	SRAM: Notes on Usage		Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	All 4-Mbit fast SRAM C-mask products	Lot No. All Lots	Reference Documents	Hitachi IC memory datasheets ADE-203-1196B(Z)/1198B(Z)/1199B(Z)/1200C(Z)/1294D(Z)/1202C(Z)/1263A(Z)/1283A(Z)/1304A(Z)/1305A(Z)		Effective Date Permanent	

As the operating speeds of SRAM products rise, securing the various design margins is becoming more difficult. Accordingly, there is an increasing possibility of noise from the input-signal or power-supply lines acting as an obstacle to the normal operation of SRAM products. To prevent malfunctions in 4-Mbit fast SRAM (C-mask) products, please note the following points.

1. Announcement

In executing a write-with-verify operations with a 4-Mbit fast SRAM (C-mask) product, incorrect data may be read because of noise, etc., even when the data has been written correctly (see figure 1 and note 1). This problem does not arise with a further read operation. If you are having problems of the type described or your project may be subject to such problems, refer to the points below for the appropriate countermeasures.

2. Countermeasures

Please apply countermeasures (1) and (2) below according to your situation.

(1) Avoid executing the read for verification in the same cycle as the write operation it follows. Verify the written data after inputting an address or switching the /CS signal.

(2) Please ensure that your design is not subject to adverse effects because of distortion or skewing of the Din input waveform (figure 2). Drive /WE low (write) after determining the data on Din (see figure 3).

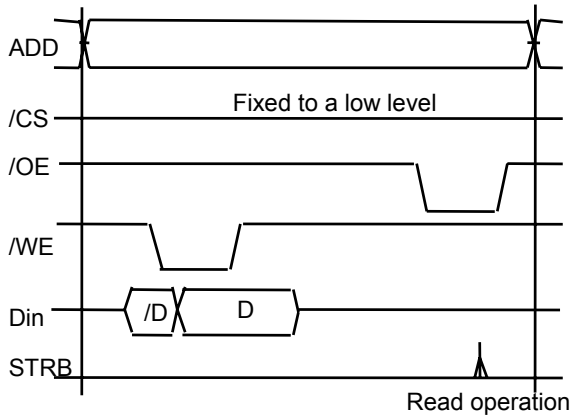

Figure 1. Write Verify Timing

*1: Write verify : After data is written within the same address cycle, perform data-read operation.

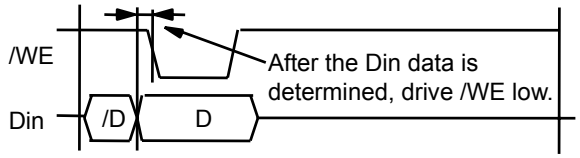

Figure 3 Write Verify Timing (Countermeasure Applied)

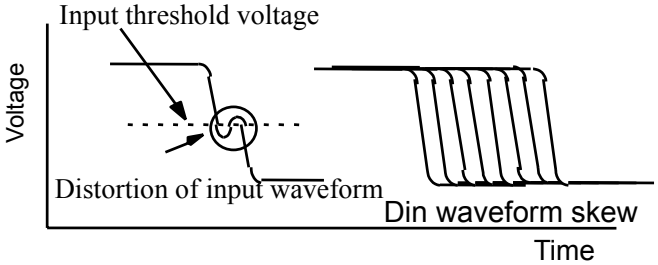

Figure 2 Din Input Waveform