HM62W8511H Series

524288-word × 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-750 (Z)
Preliminary
Rev. 0.0
Feb. 27, 1997

Description

The HM62W8511H is an asynchronous high-speed static RAM organized as 512-kword × 8-bit. It achieves high-speed access time (10/12/15 ns) through 0.35 µm CMOS process and high-speed circuit designing technology. It is most appropriate for applications that require high speed, high-density memory, and wide-bit-width configuration, such as system cache and buffer memory. The HM62W8511H is packaged in a 400-mil 36-pin SOJ for high-density surface mounting.

Features

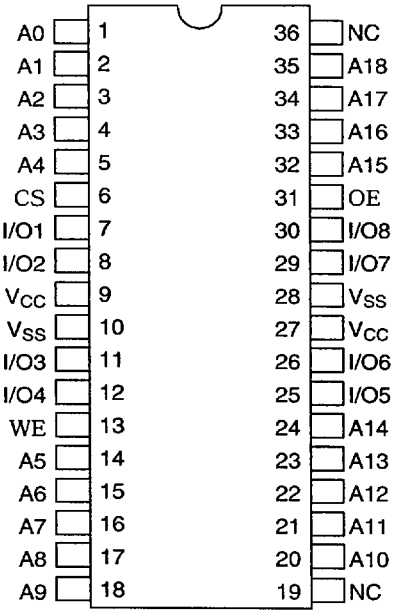
- Single supply : 3.3 V ± 0.3 V
- Access time 10 ns/12 ns/15 ns (max)
- Completely static memory; no clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible (all inputs and outputs)
- 400-mil 36-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

Ordering Information

Type No.	Access Time	Package
HM62W8511HJP-10	10 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM62W8511HJP-12	12 ns	
HM62W8511HJP-15	15 ns	
HM62W8511HLJP-10	10 ns	400-mil 36-pin plastic SOJ (CP-36D)
HM62W8511HLJP-12	12 ns	
HM62W8511HLJP-15	15 ns	

Pin Arrangement

HM62W8511HJP/HLJP Series

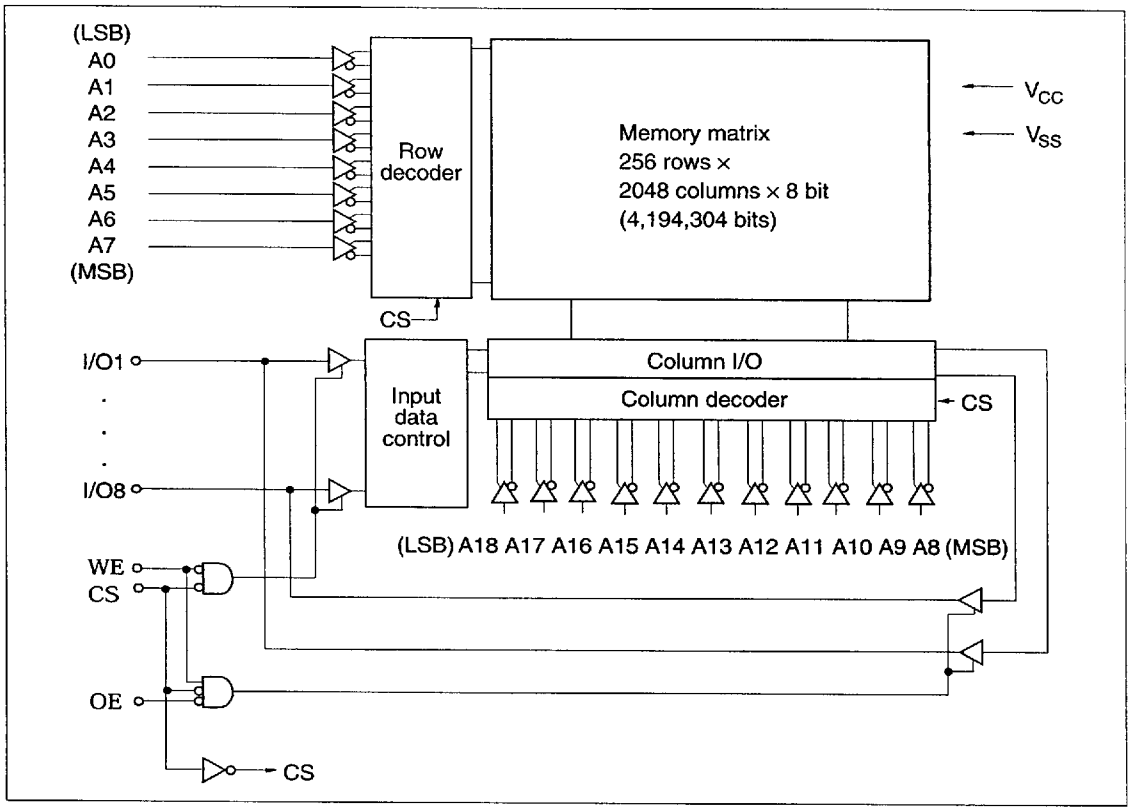


(Top View)

Pin Description

Pin name	Function
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

Block Diagram



Function Table

CS	OE	WE	Mode	V_{cc} current	I/O	Ref. cycle
H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disable	I_{cc}	High-Z	—
L	L	H	Read	I_{cc}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{cc}	Din	Write cycle (1)
L	L	L	Write	I_{cc}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to V_{CC}+0.5	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. V_T min = −2.5 V for pulse width (under shoot) ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}*2	3.0	3.3	3.6	V
Supply voltage	V_{SS}*3	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input voltage	V_{IL}	−0.3*1	—	0.8	V

Notes: 1. V_{IL} min = −2.0 V for pulse width (under shoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0V)

Parameter		Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Operation power supply current	10 ns cycle	I_{CC}	—	—	240	mA	CS = V_{IL}, Iout = 0 mA Other inputs = V_{IH}/V_{IL}
	12 ns cycle	I_{CC}	—	—	200		
	15 ns cycle	I_{CC}	—	—	190		
Standby power supply current	10 ns cycle	I_{SB}	—	—	100	mA	CS = V_{IH}, Other inputs = V_{IH}/V_{IL}
	12 ns cycle	I_{SB}	—	—	100		
	15 ns cycle	I_{SB}	—	—	100		
		I_{SB1}	—	—	10	mA	V_{CC} ≥ CS ≥ V_{CC} - 0.2 V, 1. 0 V ≤ Vin ≤ 0.2 V or 2. V_{CC} ≥ Vin ≥ V_{CC} - 0.2 V
			—*[2]	—*[2]	0.5*[2]		
Output voltage		V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
		V_{OH}	2.4	—	—	V	I_{OH} = –4 mA

Notes: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

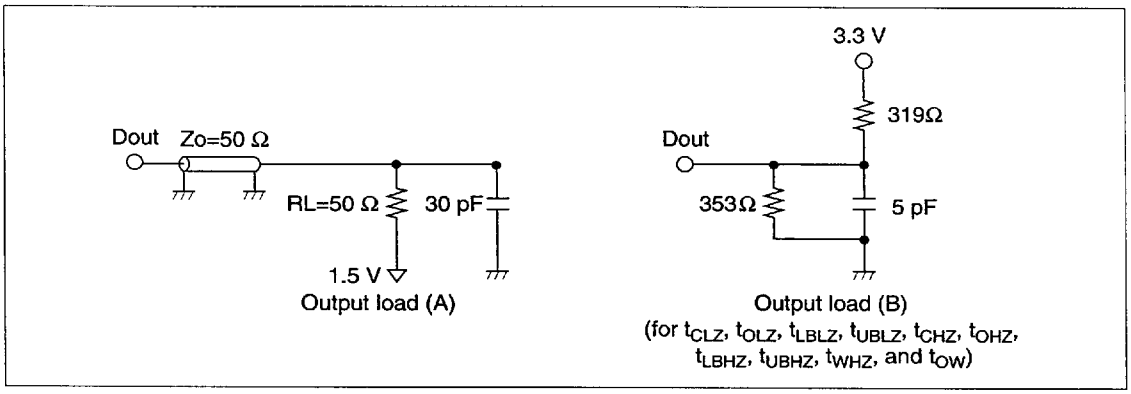
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: These parameters are sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (including scope and jig)



Read Cycle

		HM62W8511H							
		-10		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	10	—	12	—	15	—	ns	
Address access time	t_{AA}	—	10	—	12	—	15	ns	
Chip select access time	t_{ACS}	—	10	—	12	—	15	ns	
Output enable to output valid	t_{OE}	—	5	—	6	—	8	ns	
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	5	—	6	—	8	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	—	8	ns	1

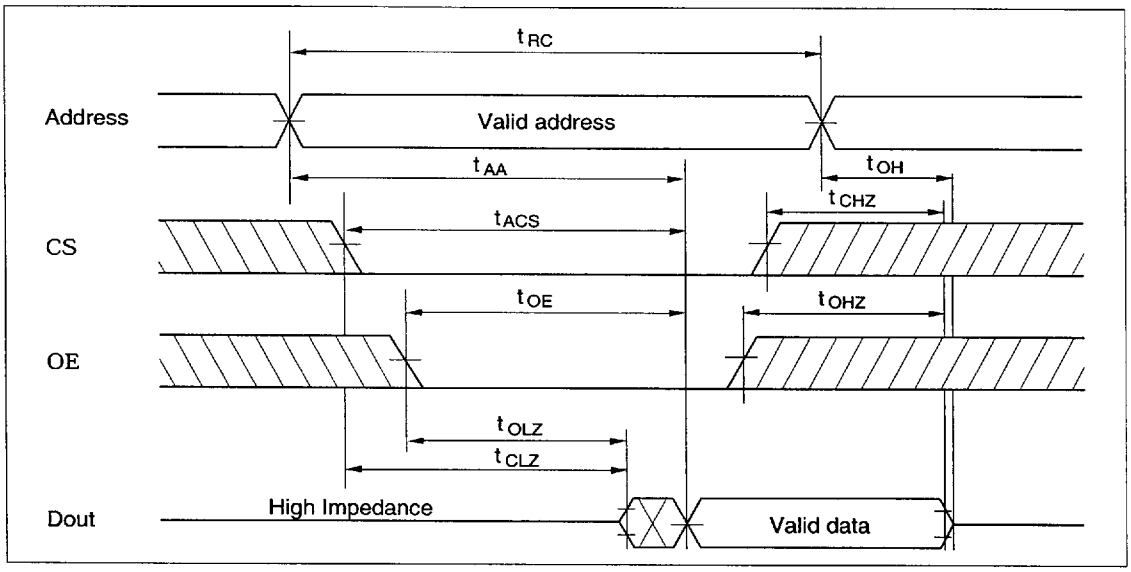
Write Cycle

		HM62W8511H							
		-10		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	10	—	12	—	15	—	ns	
Address valid to end of write	t_{AW}	6	—	8	—	10	—	ns	
Chip select to end of write	t_{CW}	6	—	8	—	10	—	ns	9
Write pulse width	t_{WP}	6	—	8	—	10	—	ns	8
Address setup time	t_{AS}	0	—	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	5	—	6	—	8	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	3	—	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	—	8	ns	1
Write enable to output in high-Z	t_{WHZ}	—	5	—	6	—	8	ns	1

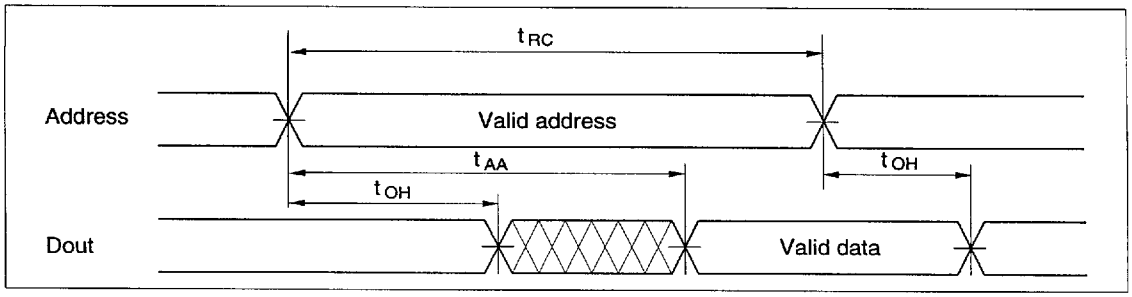
Note:
1. Transition is measured ±200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
2. Address should be valid prior to or coincident with CS transition low.
3. WE and/or CS must be high during address transition time.
4. If CS and OE are low during this period, I/O pins are in the output state, and the data input signals of opposite phase to the outputs must not be applied to them.
5. If the CS low transition occurs simultaneously with the WE low transition or after the WE transition, output remains in a high-impedance state.
6. t_{AS} is measured from the latest address transition to the later of CS or WE going low.
7. t_{WR} is measured from the earlier of CS or WE going high to the first address transition.
8. A write occurs during the overlap of a low CS and a low WE. A write begins at the latest transition among CS going low and WE going low. A write ends at the earliest transition among CS going high and WE going high. t_{WP} is measured from the beginning of the write to the end of the write.
9. t_{CW} is measured from the later of CS going low to the end of the write.

Timing Waveforms

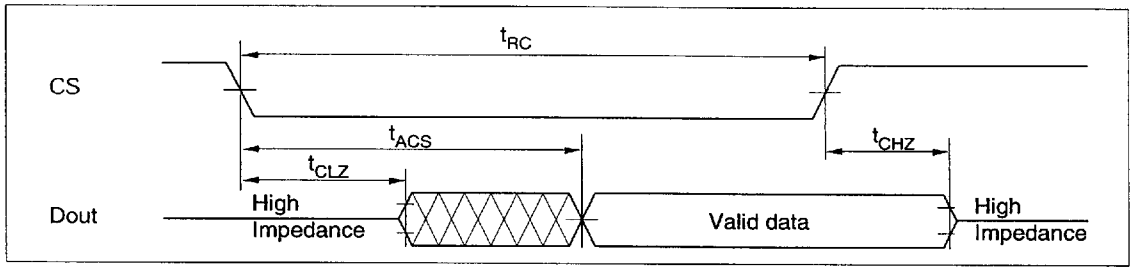
Read Timing Waveform (1) (WE = V_{IH})



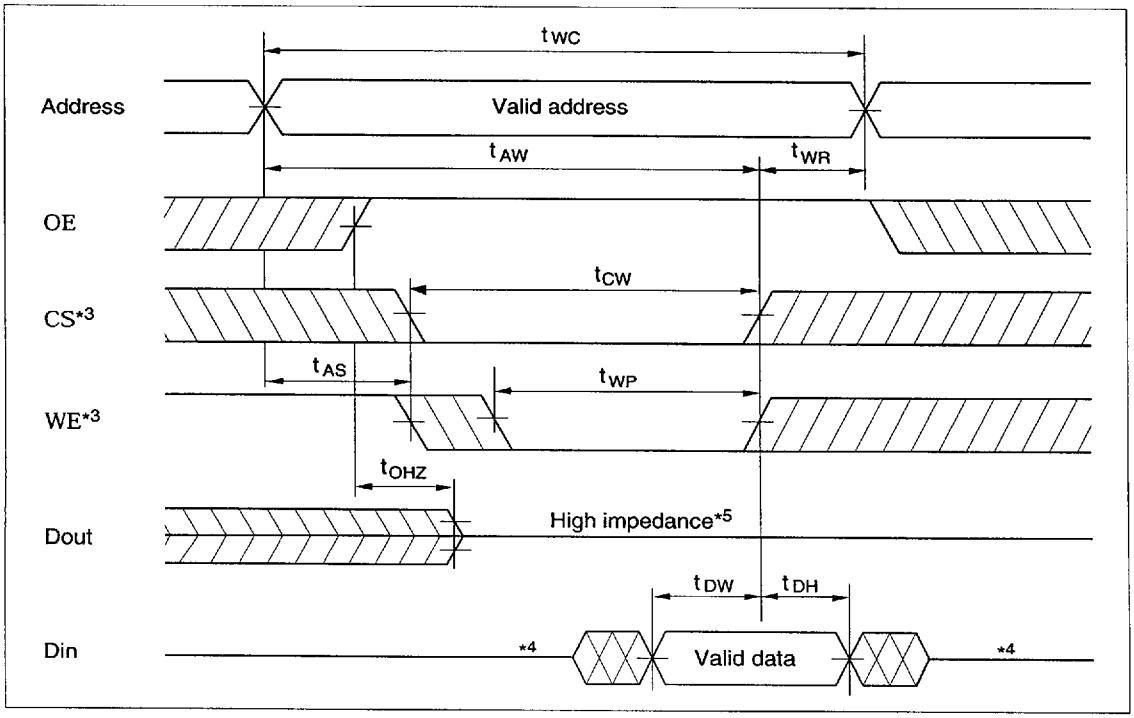
Read Timing Waveform (2) (WE = V_{IH}, CS = V_{IL}, OE = V_{IL})



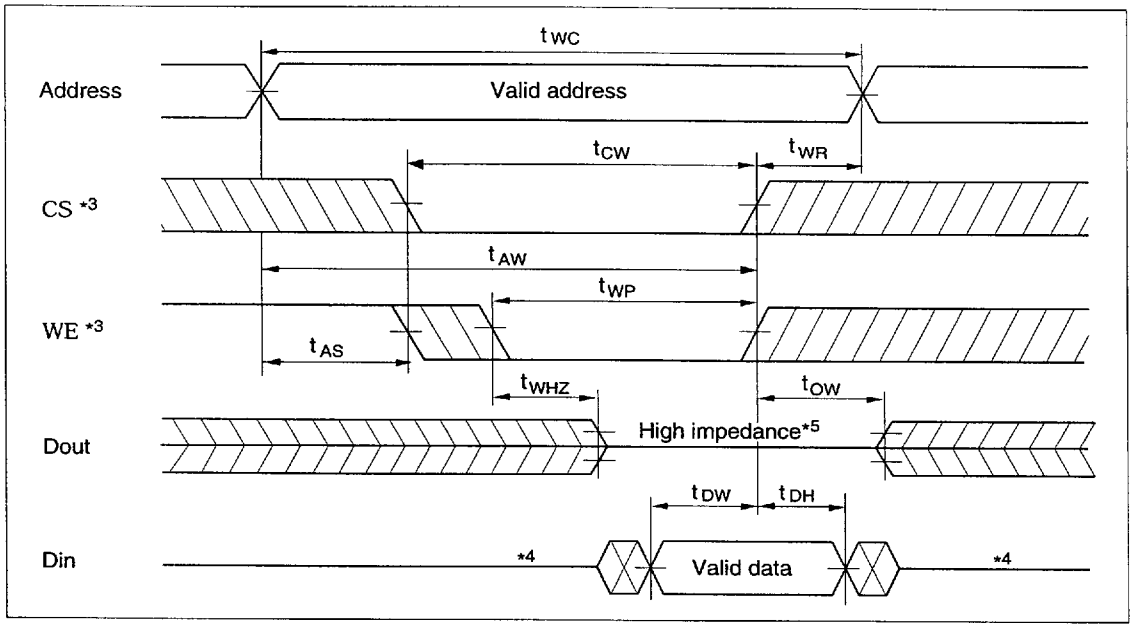
Read Timing Waveform (3) (WE = V_{IH}, CS = V_{IL}, OE = V_{IL})*2



Write Timing Waveform (1) (WE Controlled)



Write Timing Waveform (2) (CS Controlled)



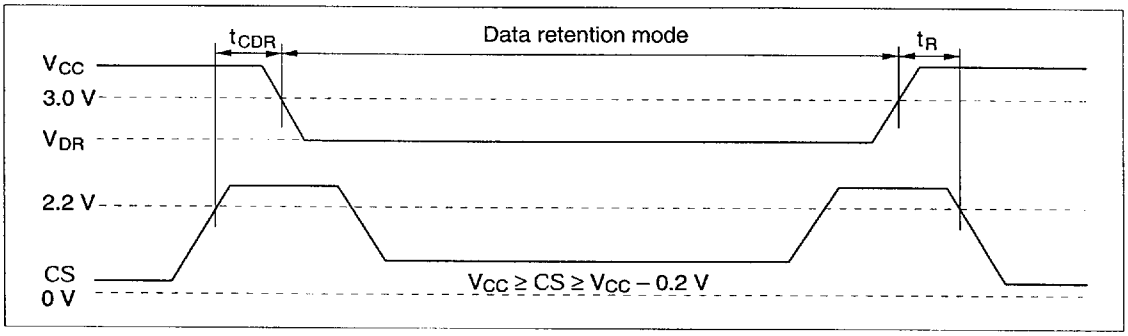
Low V_{CC} Data Retention Characteristics (Ta = 0 to 70°C)

These characteristics are guaranteed only for the L-version.

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq CS \geq V_{CC} - 0.2$ V 1. $0 V \leq Vin \leq 0.2$ V or 2. $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	2	300	µA	V_{CC} = 3 V, $V_{CC} \geq CS \geq V_{CC} - 0.2$ V 1. $0 V \leq Vin \leq 0.2$ V or 2. $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	See retention waveform

Note: Typical values are at V_{CC} = 3.0 V, Ta = 25°C, and not guaranteed.

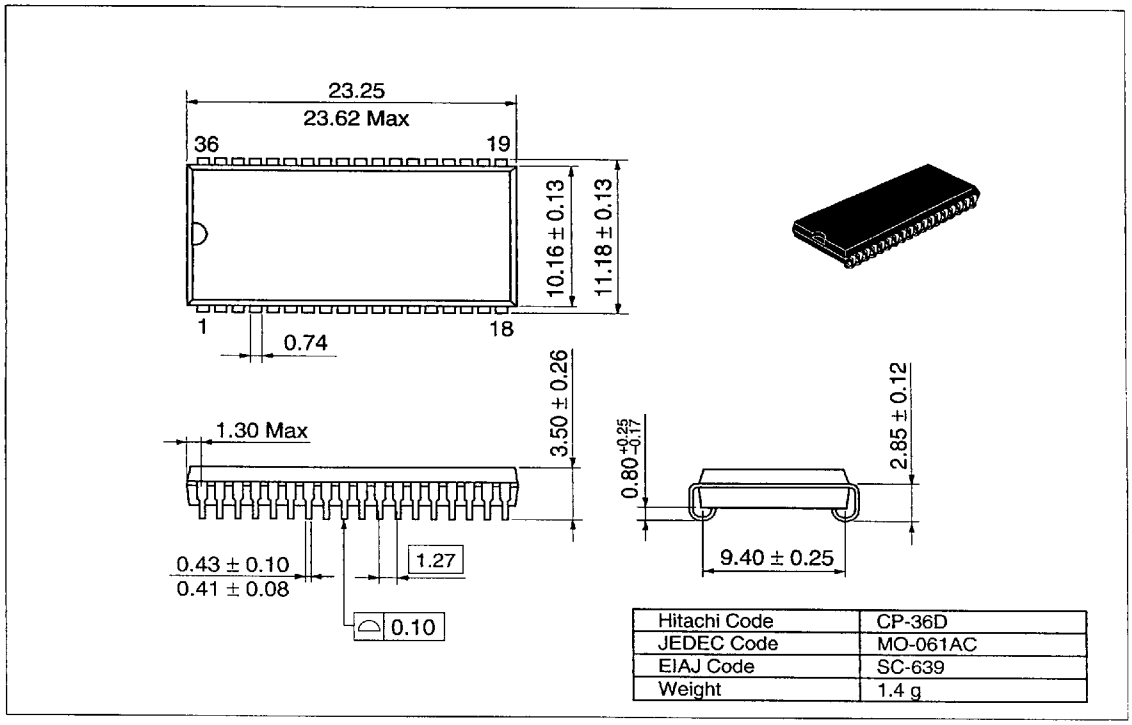
Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM62W8511HJP/HLJP Series (CP-36D)

Unit: mm



Hitachi Code	CP-36D
JEDEC Code	MO-061AC
EIAJ Code	SC-639
Weight	1.4 g