HM658128A Series

131072-word × 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128A is a pseudo-static RAM organized as 131,072-word × 8-bit. HM658128A realizes low power consumption and high speed access time by employing 1.3 µm CMOS process technology.

The HM658128A supports 3 refresh functions: address refresh, auto refresh and self refresh. Low power version dissipates only 0.5 mW (typ) in self refresh mode and retains the data with battery. Self refresh mode is guaranteed only for L-version and LL-version.

The HM658128A is pin-compatible with 1-Mbit static RAM.

Features

- Single 5 V (±10%)
- High speed
  - Access time
    $\overline{CE}$ Access time: 80/100/120 ns
  - Cycle time
    Random read/
    Write cycle time : 130/160/190 ns
- Low power: 300 mW typ (active)
  0.5 mW (standby)
- All inputs and outputs TTL compatible
- Non multiplexed address
- 512 refresh cycles (8 ms)
- Refresh functions
  Address refresh
  Automatic refresh
  Self refresh (Only for L-version and LL-version)

Ordering Information

Type No.	Access time	Package
HM658128ADP-8	80 ns	600-mil 32-pin plastic DIP (DP-32)
HM658128ADP-10	100 ns	
HM658128ADP-12	120 ns	
HM658128ALP-8	80 ns	
HM658128ALP-10	100 ns	
HM658128ALP-12	120 ns	
HM658128ALP-8L	80 ns	
HM658128ALP-10L	100 ns	
HM658128ALP-12L	120 ns	
HM658128ADFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658128ADFP-10	100 ns	
HM658128ADFP-12	120 ns	
HM658128ALFP-8	80 ns	
HM658128ALFP-10	100 ns	
HM658128ALFP-12	120 ns	
HM658128ALFP-8L	80 ns	
HM658128ALFP-10L	100 ns	
HM658128ALFP-12L	120 ns	
HM658128ALT-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP (TFP-32D)
HM658128ALT-10	100 ns	
HM658128ALT-12	120 ns	
HM658128ALT-8L	80 ns	
HM658128ALT-10L	100 ns	
HM658128ALT-12L	120 ns	
HM658128ADT-8	80 ns	
HM658128ADT-10	100 ns	
HM658128ADT-12	120 ns	
HM658128ADR-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TFP-32DR)
HM658128ADR-10	100 ns	
HM658128ADR-12	120 ns	
HM658128ALR-8	80 ns	
HM658128ALR-10	100 ns	
HM658128ALR-12	120 ns	
HM658128ALR-8L	80 ns	
HM658128ALR-10L	100 ns	
HM658128ALR-12L	120 ns	

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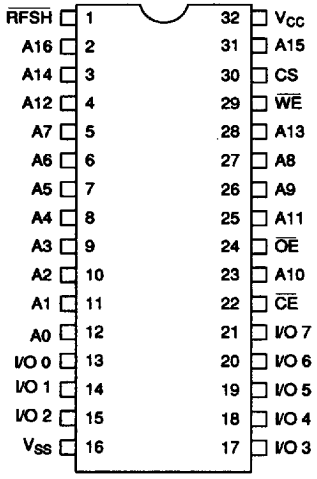
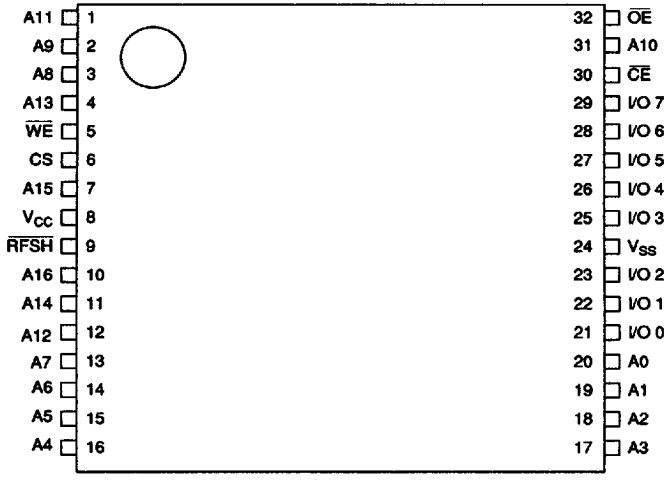
Pin Arrangement

HM658128AP/AFP Series



(Top View)

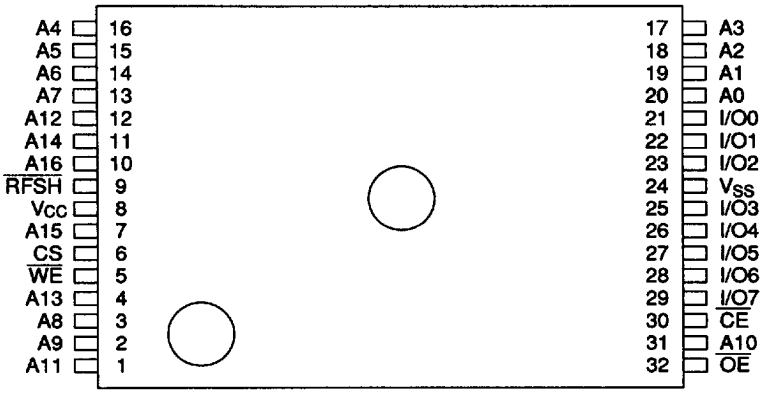
HM658128AT Series



(Top View)

Pin Arrangement (cont)

HM658128AR Series



(Top View)

Pin Description

Symbol	Pin name
A0 – A16	Address inputs
I/O0 – I/O7	Data input/output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
CS	Chip select
V_{CC}	Power supply
V_{SS}	Ground

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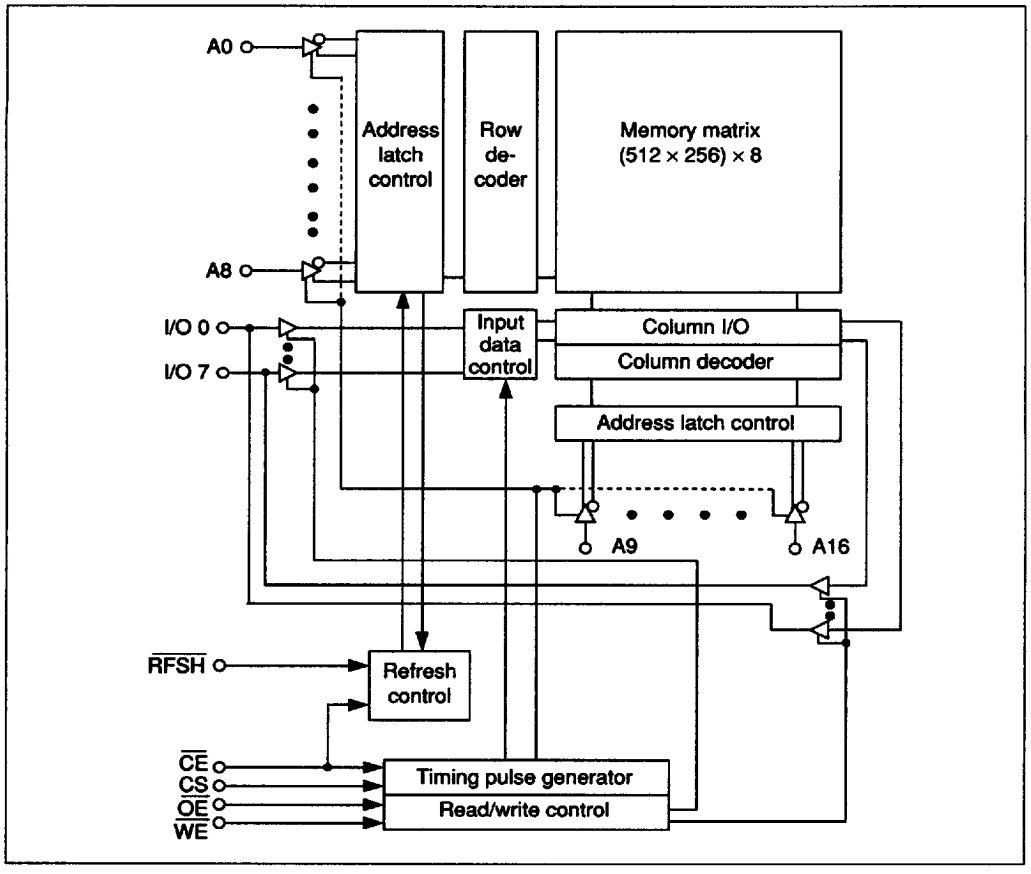
Block Diagram



Truth Table

$\overline{CE}$	CS at $\overline{CE}$ going low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O pin	Mode
L	H	X	L	H	Low-Z	Read
L	H	X	X	L	High-Z	Write
L	H	X	H	H	High-Z	—
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh*1
H	X	H	X	X	High-Z	Standby

Note: 1. Self refresh is guaranteed only for L-version and LL-version.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	–1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5^{*1}	—	0.8	V

Note: 1. V_{IL} min = –3.0 V for pulse width ≤ 10 ns.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Operating power supply current	I_{CC1}	—	60	85	mA	$I_{I/O}$ = 0 mA tcyc = min.
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}, Vin ≥ 0 V
Standby power supply current	I_{SB2}	—	100*1	200*1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V $\overline{RFSH}$ ≥ V_{CC} – 0.2 V, Vin ≥ 0 V
		—	70*2	100*2	µA	
Operating power supply current in self refresh mode	I_{CC2}	—	1*1, *2	2*1, *2	mA	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}, Vin ≥ 0 V
	I_{CC3}	—	100*1	200*1	µA	$\overline{CE}$ ≥ V_{CC} – 0.2 V $\overline{RFSH}$ ≤ 0.2 V, Vin ≥ 0 V
		—	70*2	100*2	µA	
Input leakage current	I_{LI}	–10	—	10	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	–10	—	10	µA	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LL-version.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
- Output load: 1 TTL and 100 pF (including scope and jig)

		HM658128A-8		HM658128A-10		HM658128A-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Random read or write cycle time	t_{RC}	130	—	160	—	190	—	ns
Random read-modify-write cycle time	t_{RWC}	190	—	220	—	260	—	ns
Chip enable access time	t_{CEA}	—	80	—	100	—	120	ns
Output enable access time	t_{OEA}	—	30	—	30	—	40	ns
Chip disable to output in high-Z	t_{CHZ}	0	30	0	30	0	35	ns
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	20	—	ns
Output disable to output in high-Z	t_{OHZ}	—	25	—	25	—	30	ns
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip enable pulse width	t_{CE}	80 ns	10 µs	100 ns	10 µs	120 ns	10 µs	
Chip enable precharge time	t_P	40	—	50	—	60	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Address hold time	t_{AH}	30	—	30	—	35	—	ns
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns
$\overline{RFSH}$ hold time	t_{RHC}	15	—	15	—	15	—	ns
Chip select setup time	t_{CSS}	0	—	0	—	0	—	ns
Chip select hold time	t_{CSH}	30	—	30	—	35	—	ns
Write command pulse width	t_{WP}	30	—	30	—	35	—	ns
Chip enable to end of write	t_{CW}	80	—	100	—	120	—	ns
Data in to end of write	t_{DW}	25	—	25	—	30	—	ns
Data in hold time for write	t_{DH}	0	—	0	—	0	—	ns

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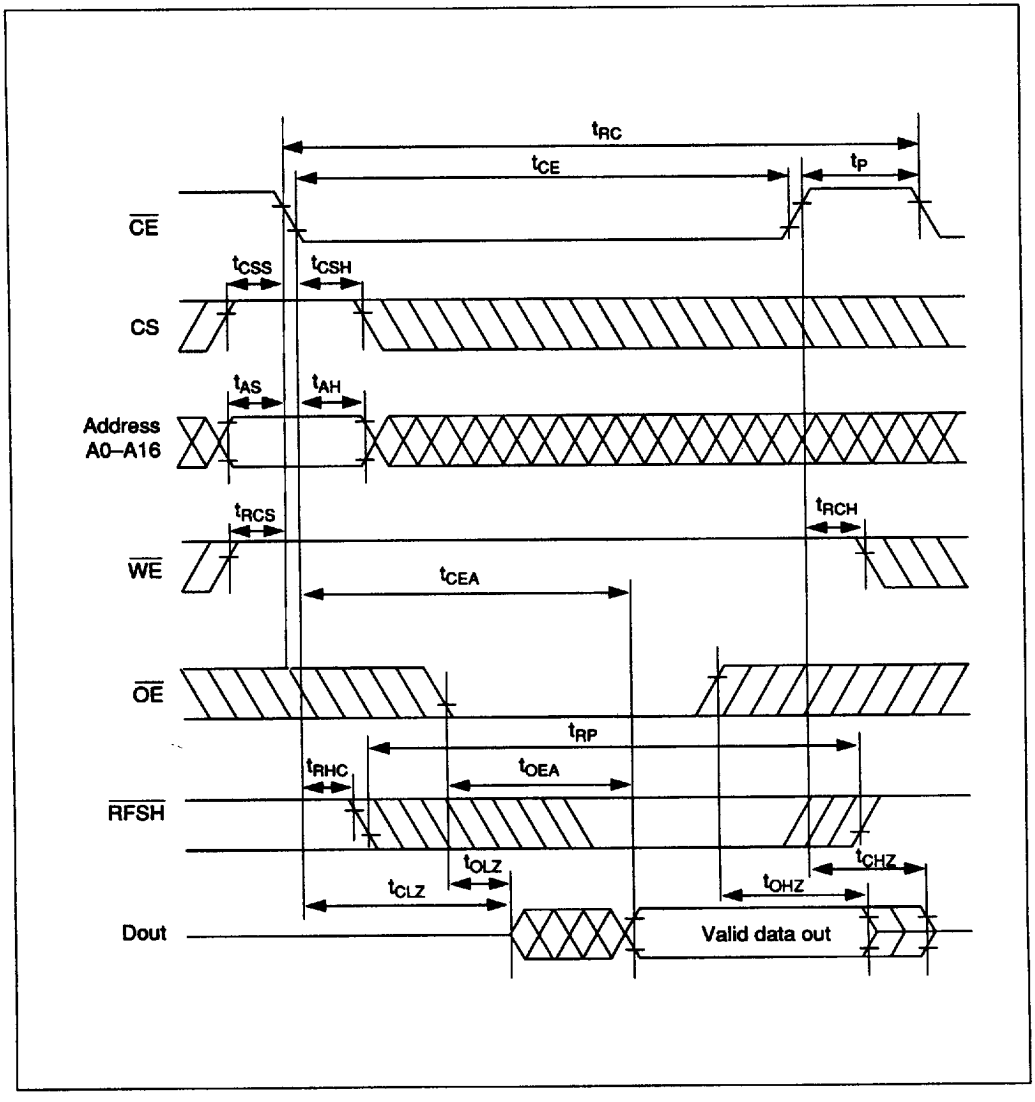
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Parameter	Symbol	HM658128A-8 Min	HM658128A-8 Max	HM658128A-10 Min	HM658128A-10 Max	HM658128A-12 Min	HM658128A-12 Max	Unit
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns
Write to output in high-Z	t_{WHZ}	—	25	—	25	—	30	ns
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns
Refresh command delay time	t_{RFD}	40	—	50	—	60	—	ns
Refresh precharge time	t_{FP}	40	—	40	—	40	—	ns
Refresh command pulse width	t_{RP}	—	8	—	8	—	8	µs
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs	80 ns	8 µs	
Automatic refresh cycle time	t_{FC}	130	—	160	—	190	—	ns
Refresh command pulse width for self refresh	t_{FAS} *9	8	—	8	—	8	—	µs
Refresh reset time for self refresh	t_{RFS} *9	130	—	160	—	190	—	ns
Refresh period (512 cycles)	t_{REF}	—	8	—	8	—	8	ms

Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause more than 100 µs and execute at least 8 initialization cycles.
8. 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15 µs after self refresh, in order to meet the refresh specification of 8 ms and 512 cycles.
9. This characteristics is guaranteed only for L-version and LL-version.
10. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, $\overline{CE}$ and $\overline{RFSH}$ must be kept high. If auto refresh follows self refresh, low transition of $\overline{RFSH}$ at the beginning of auto refresh must not occur during t_{RFS} period.

Timing Waveforms

Read Cycle



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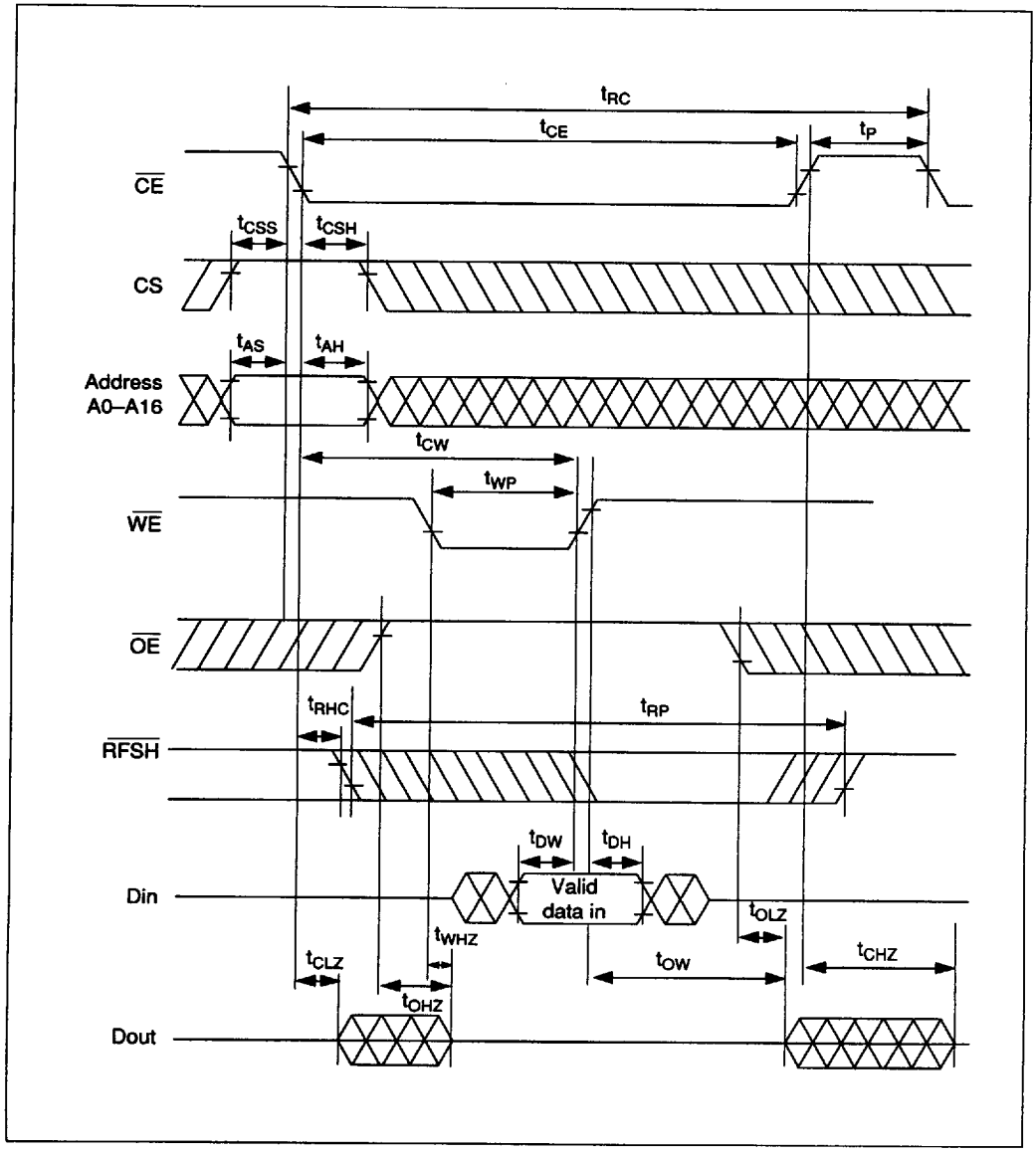
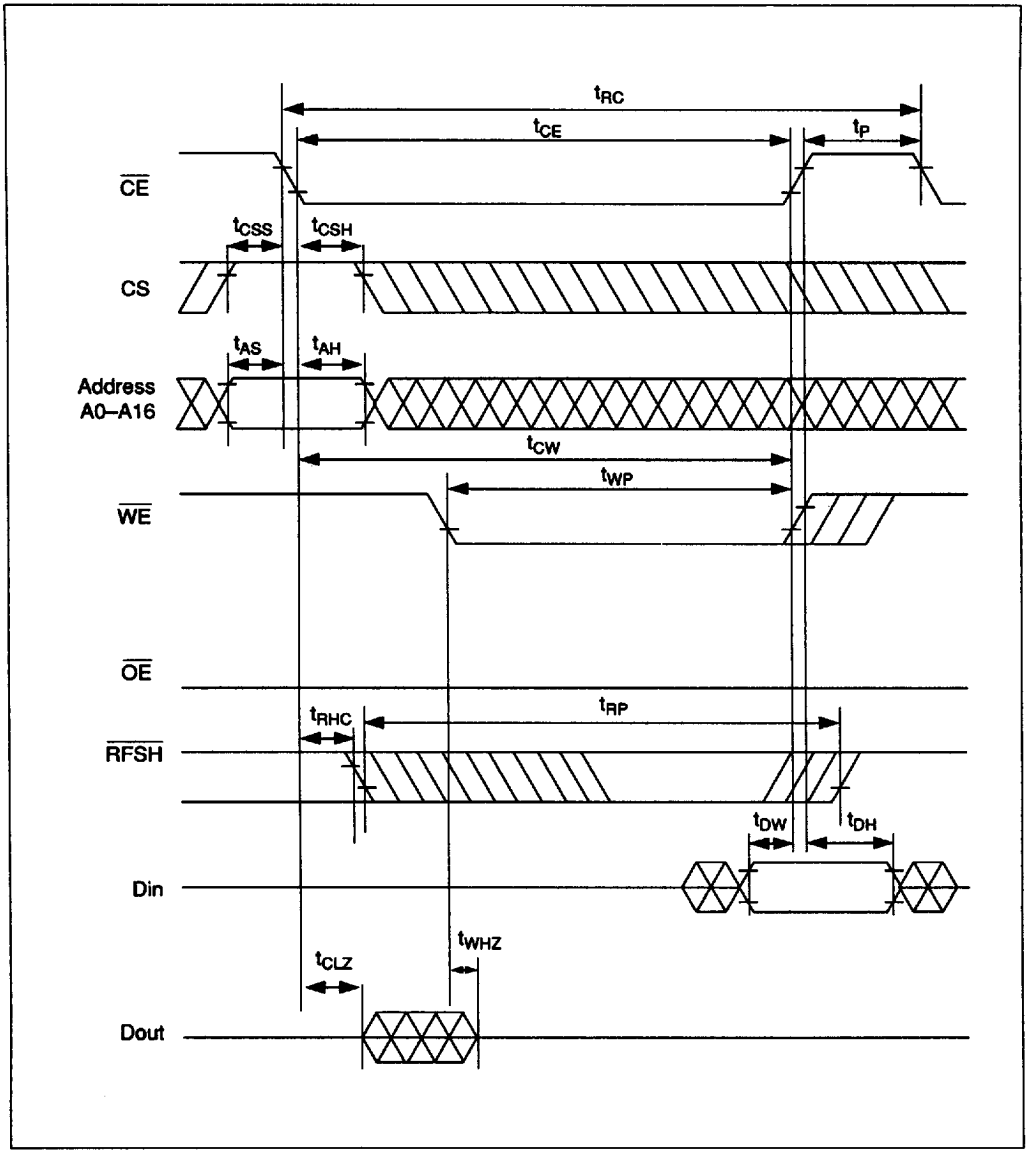
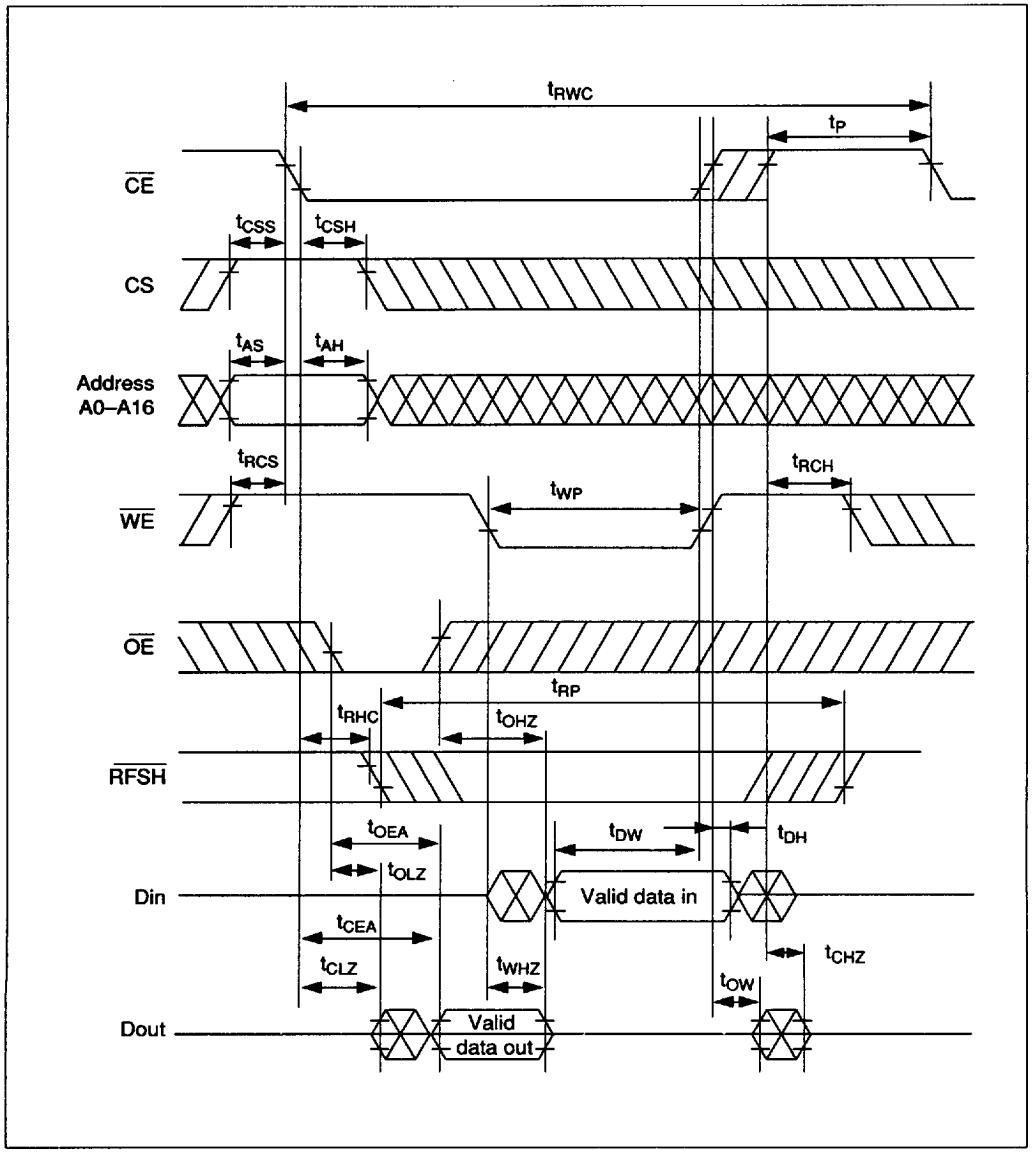
Write Cycle ($\overline{OE}$ clock)



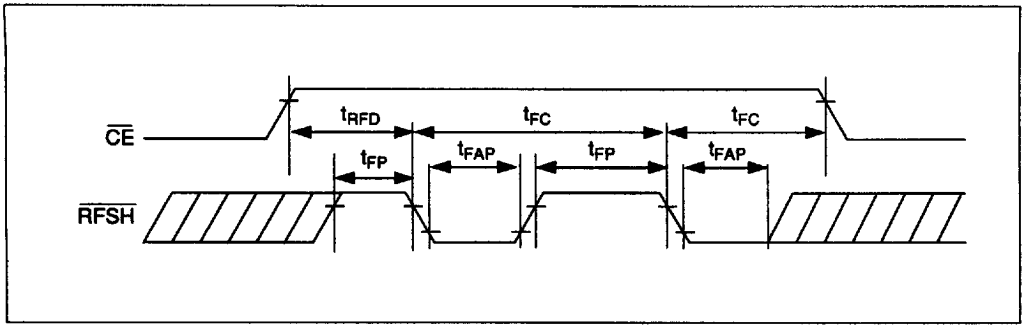
Write Cycle ($\overline{OE}$ Low Fix)



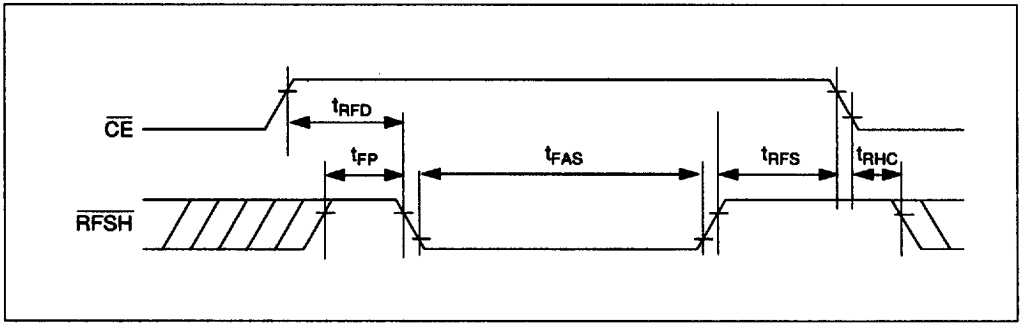
Read-Modify-Write Cycle



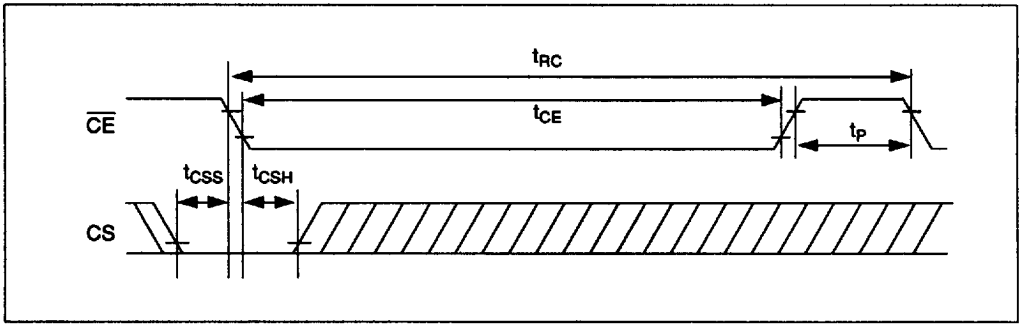
Auto Refresh Cycle



Self Refresh Cycle



CS Standby Mode



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