

# HM6708A Series ——— HITACHI/ LOGIC/ARRAYS/MEM

65536-word × 4-bit High Speed Static Random Access Memory

T-46-23-10

## Features

- 65536-word × 4 bit organization
- Fully TTL compatible input and output
- 1.0  $\mu$ m Hi-BiCMOS process
- +5 V single supply
- Completely static memory  
No clock or timing strobe required
- Low power dissipation  
Operation: 400 mW typ
- Super fast  
Access time: 15/20 ns (max)

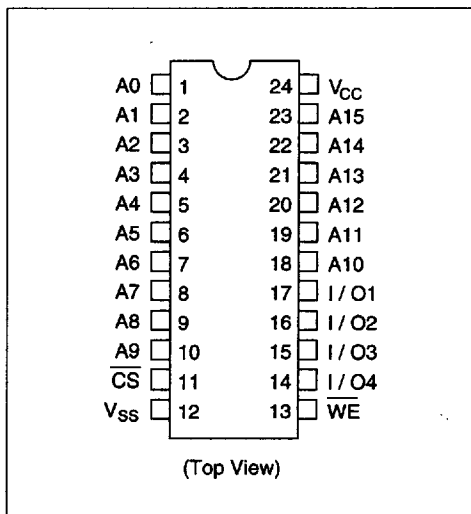
## Ordering Information

| Type No.     | Access time | Package                              |
|--------------|-------------|--------------------------------------|
| HM6708AP-15  | 15 ns       | 300-mil 24-pin plastic DIP (DP-24NC) |
| HM6708AP-20  | 20 ns       |                                      |
| HM6708AJP-15 | 15 ns       | 300-mil 24-pin plastic SOJ (CP-24D)  |
| HM6708AJP-20 | 20 ns       |                                      |

## Pin Description

| Pin name               | Function          |
|------------------------|-------------------|
| A0 – A15               | Address input     |
| I/O1 – I/O4            | Data input/output |
| WE                     | Write enable      |
| $\overline{\text{CS}}$ | Chip select       |
| V <sub>SS</sub>        | Ground            |
| V <sub>CC</sub>        | Power supply      |

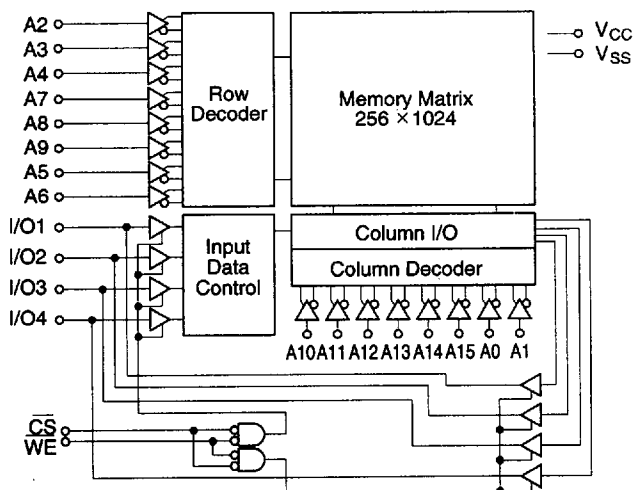
## Pin Arrangement



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## Block Diagram

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## Function Table

| $\overline{CS}$ | $\overline{WE}$ | Mode         | I/O pin  | $V_{CC}$ current  | Ref. cycle           |
|-----------------|-----------------|--------------|----------|-------------------|----------------------|
| H               | X               | Not selected | High-Z   | $I_{SB}, I_{SB1}$ | —                    |
| L               | H               | Read         | Data out | $I_{CC}, I_{CC1}$ | Read cycle (1), (2)  |
| L               | L               | Write        | Data in  | $I_{CC}, I_{CC1}$ | Write cycle (1), (2) |

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**Absolute Maximum Ratings**

| Parameter                             | Symbol           | Rating       | Unit |
|---------------------------------------|------------------|--------------|------|
| Terminal voltage to $V_{SS}$ pin      | $V_T$            | -0.5 to +7.0 | V    |
| Power dissipation                     | $P_T$            | 1.0          | W    |
| Operating temperature range           | $T_{opr}$        | 0 to +70     | °C   |
| Storage temperature range (with bias) | $T_{stg}$ (Bias) | -10 to +85   | °C   |
| Storage temperature range             | $T_{stg}$        | -55 to +125  | °C   |

**Recommended DC Operating Conditions ( $T_a = 0$  to +70°C)**

| Parameter          | Symbol   | Min                | Typ | Max            | Unit |
|--------------------|----------|--------------------|-----|----------------|------|
| Supply voltage     | $V_{CC}$ | 4.5                | 5.0 | 5.5            | V    |
|                    | $V_{SS}$ | 0.0                | 0.0 | 0.0            | V    |
| Input high voltage | $V_{IH}$ | 2.2                | —   | $V_{CC} + 0.5$ | V    |
| Input low voltage  | $V_{IL}$ | -3.0 <sup>*1</sup> | —   | 0.8            | V    |

Note: 1. Pulse width 15 ns, DC : -0.5 V

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DC Characteristics ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_a = 0 \text{ to } +70^\circ\text{C}$ )

| Parameter                      | Symbol     | HM6708A-15 |     |     | HM6708A-20 |     |     | Unit          | Test conditions                                                                                            |
|--------------------------------|------------|------------|-----|-----|------------|-----|-----|---------------|------------------------------------------------------------------------------------------------------------|
|                                |            | Min        | Typ | Max | Min        | Typ | Max |               |                                                                                                            |
| Input leakage current          | $ I_{LI} $ | —          | —   | 2   | —          | —   | 2   | $\mu\text{A}$ | $V_{CC} = 5.5 \text{ V}$ ,<br>$V_{in} = 0 \text{ V to } V_{CC}$                                            |
| Output leakage current         | $ I_{LO} $ | —          | —   | 10  | —          | —   | 10  | $\mu\text{A}$ | $CS = V_{IH}$ ,<br>$V_{I/O} = 0 \text{ V to } V_{CC}$                                                      |
| Operating power supply current | $I_{CC}$   | —          | —   | 100 | —          | —   | 100 | $\text{mA}$   | $CS = V_{IL}$ , $I_{I/O} = 0 \text{ mA}$                                                                   |
| Average operating current      | $I_{CC1}$  | —          | —   | 140 | —          | —   | 120 | $\text{mA}$   | min. cycle,<br>Duty: 100%,<br>$I_{I/O} = 0 \text{ mA}$                                                     |
| Standby power supply current   | $I_{SB}$   | —          | —   | 30  | —          | —   | 30  | $\text{mA}$   | $CS = V_{IH}$ ,<br>$V_{in} = V_{IH} \text{ or } V_{IL}$                                                    |
|                                | $I_{SB1}$  | —          | —   | 10  | —          | —   | 10  | $\text{mA}$   | $CS \geq V_{CC} - 0.2 \text{ V}$<br>$V_{in} \leq 0.2 \text{ V}$ or<br>$V_{in} \geq V_{CC} - 0.2 \text{ V}$ |
| Output low voltage             | $V_{OL}$   | —          | —   | 0.4 | —          | —   | 0.4 | $\text{V}$    | $I_{OL} = 8 \text{ mA}$                                                                                    |
| Output high voltage            | $V_{OH}$   | 2.4        | —   | —   | 2.4        | —   | —   | $\text{V}$    | $I_{OH} = -4 \text{ mA}$                                                                                   |

Capacitance ( $T_a = 25^\circ\text{C}$ ,  $f = 1 \text{ MHz}$ )

| Parameter          | Symbol         | Max | Unit        | Test condition          |
|--------------------|----------------|-----|-------------|-------------------------|
| Input capacitance  | $C_{in}^{*1}$  | 6   | $\text{pF}$ | $V_{in} = 0 \text{ V}$  |
| Output capacitance | $C_{I/O}^{*1}$ | 10  | $\text{pF}$ | $V_{I/O} = 0 \text{ V}$ |

Note: 1. This parameter is sampled and not 100% tested.

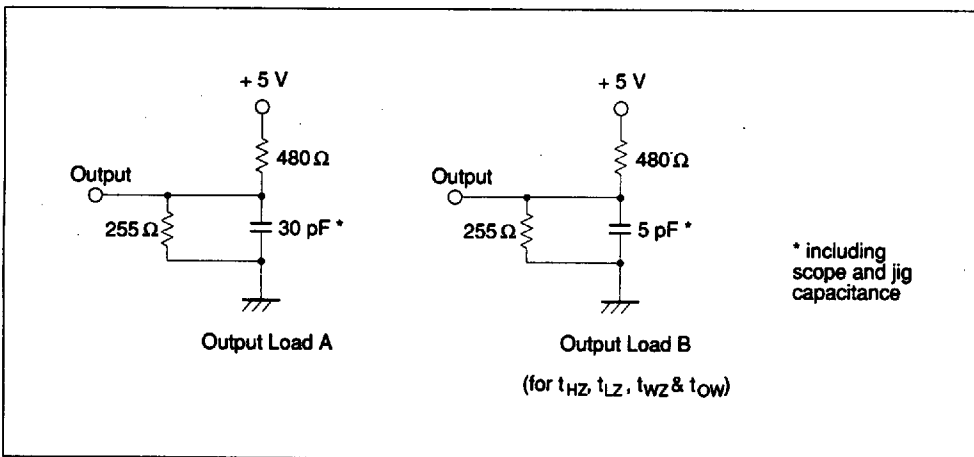
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AC Characteristics ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$  unless otherwise noted)

## Test Conditions

- Input pulse levels:  $V_{SS}$  to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figures
- Input rise and fall times: 4 ns
- Output reference levels: 1.5 V



## Read Cycle

| Parameter                            | Symbol            | HM6708A-15 |     | HM6708A-20 |     | Unit |
|--------------------------------------|-------------------|------------|-----|------------|-----|------|
|                                      |                   | Min        | Max | Min        | Max |      |
| Read cycle time                      | $t_{RC}$          | 15         | —   | 20         | —   | ns   |
| Address access time                  | $t_{AA}$          | —          | 15  | —          | 20  | ns   |
| Chip select access time              | $t_{ACS}$         | —          | 15  | —          | 20  | ns   |
| Output hold from address change      | $t_{OH}$          | 4          | —   | 5          | —   | ns   |
| Chip selection to output in low-Z    | $t_{LZ}^{*1, *2}$ | 4          | —   | 5          | —   | ns   |
| Chip deselection to output in high-Z | $t_{HZ}^{*1, *2}$ | 0          | 6   | 0          | 8   | ns   |

- Notes: 1. This parameter is sampled and not 100% tested.  
2. Transition is measured  $\pm 200\text{ mV}$  from steady state voltage with specified loading in Load (B).

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## Write Cycle

| Parameter                        | Symbol            | HM6708A-15 |     | HM6708A-20 |     | Unit |
|----------------------------------|-------------------|------------|-----|------------|-----|------|
|                                  |                   | Min        | Max | Min        | Max |      |
| Write cycle time                 | $t_{WC}^{*1}$     | 15         | —   | 20         | —   | ns   |
| Chip selection to end of write   | $t_{CW}$          | 10         | —   | 15         | —   | ns   |
| Address valid to end of write    | $t_{AW}$          | 10         | —   | 15         | —   | ns   |
| Address setup time               | $t_{AS}$          | 0          | —   | 0          | —   | ns   |
| Write pulse width                | $t_{WP}$          | 10         | —   | 15         | —   | ns   |
| Write recovery time              | $t_{WR}$          | 0          | —   | 0          | —   | ns   |
| Data valid to end of write       | $t_{DW}$          | 8          | —   | 10         | —   | ns   |
| Data hold time                   | $t_{DH}$          | 0          | —   | 0          | —   | ns   |
| Write enable to output in high-Z | $t_{WZ}^{*2, *3}$ | 0          | 6   | 0          | 8   | ns   |
| Output active from end of write  | $t_{OW}^{*2, *3}$ | 0          | —   | 0          | —   | ns   |

Notes: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

2. This parameter is sampled and not 100% tested.

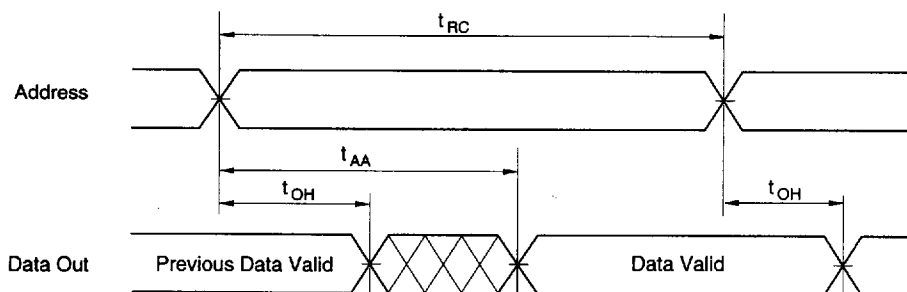
3. Transition is measured  $\pm 200$  mV from steady state voltage with specified loading in Load (B).

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### Timing Waveforms

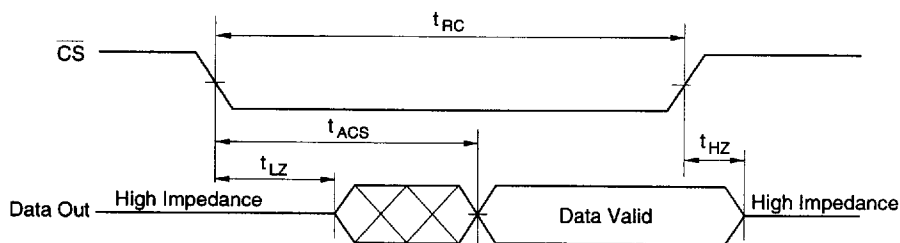
#### Read Cycle (1) \*1, \*2



Notes : 1.  $\overline{WE}$  is high for read cycle.

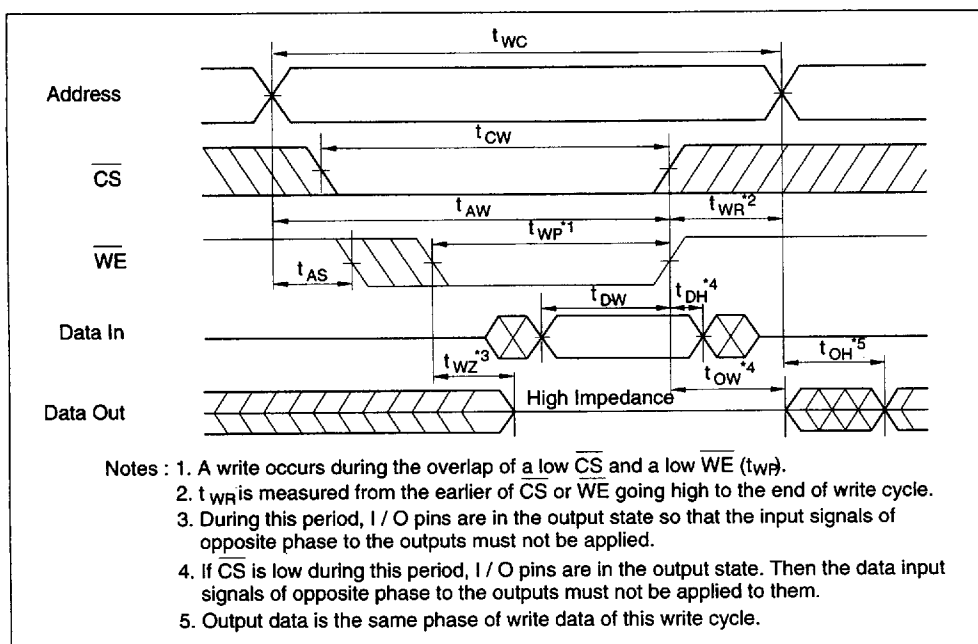
2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .

#### Read Cycle (2) \*1, \*2



Notes : 1.  $\overline{WE}$  is high for read cycle.

2. Address valid prior to or coincident with  $\overline{CS}$  transition low.

**Write Cycle (1) \*1, \*2, \*3, \*4, \*5 ( $\overline{WE}$  Controlled)**

**Write Cycle (2) \*1, \*2, \*3 ( $\overline{CS}$  Controlled)**
