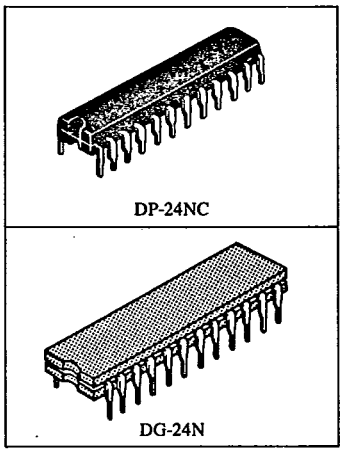
HM6716 Series
HM6719 Series

T-46-23-12

2048-word x 8-bit High Speed Static RAM
2048-word x 9-bit High Speed Static RAM



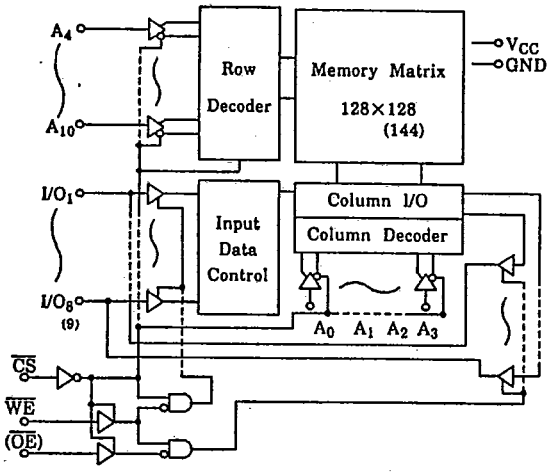
■ Features

- Fast Access Time: 25/30ns (max)
- Low Power Dissipation (DC): 280mW (typ.)
- +5V Single Supply
- Completely Static Memory No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- Skinny 24-pin Cerdip (300mil) and Plastic DIP (300mil)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6716-25	25ns	300 mil 24 Pin Cerdip and Plastic DIP
HM6716-30	30ns	
HM6719-25	25ns	
HM6719-30	30ns	

■ Block Diagram

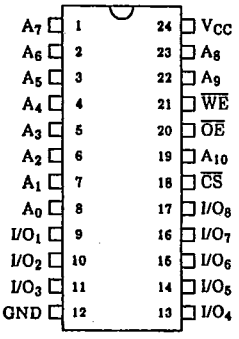


■ Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to GND Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

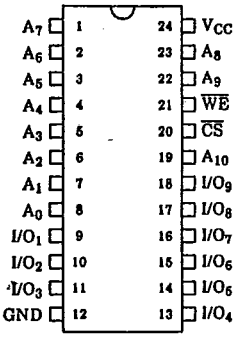
■ PIN ARRANGEMENT

● **HM6716**



(Top View)

● **HM6719**



(Top View)

■ Truth Table

● HM6716

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

● HM6719

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (2) (3)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

■ Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}*)	−3.0	–	0.8	V

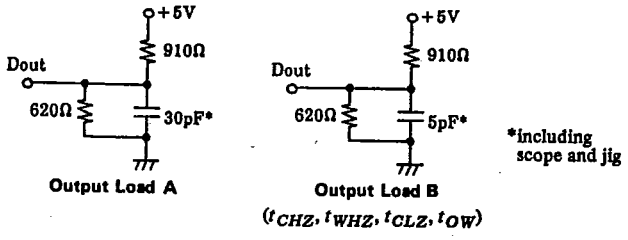
*) Pulse Width: 20ns, DC: −0.5V

■ DC and Operating Characteristics (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=0V to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	–	120	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	–	–	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, $I_{I/O}$=0mA	–	–	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V	–	–	10	mA
Output Low Voltage	V_{OL}	I_{OL}=4mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1mA	2.4	–	–	V

■ AC Test Conditions

Input pulse levels: GND to 3.0V
Input and Output reference levels: 1.5V ±200mV from steady level (Output Load B)
Input rise and fall time: 4ns
Output Load: See Figure



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■ **Capacitance** (T_a = 25°C, f = 1.0 MHz)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	–	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	8	pF

Note) This parameter is sampled and not 100%, tested.

■ **AC Characteristics** (V_{CC} 5V ± 10%, T_a = 0 to +70°C, unless otherwise noted.)

● **READ CYCLE**

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	–
Address Access Time	t_{AA}	–	25	–	30	ns	–
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	–
Chip Selection to Output in Low Z	t_{CLZ}	0	–	0	–	ns	*2
Output Enable to Output Valid	t_{OE}	0	20	0	20	ns	*1
Output Enable to Output in Low Z	t_{OLZ}	0	–	0	–	ns	*1, *2
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns	*2
Chip Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–

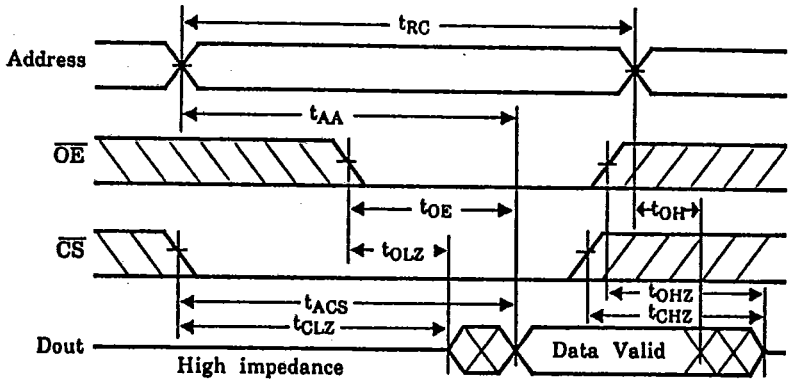
● **Write Cycle**

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	25	–	30	–	ns	–
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	–
Write Pulse Width	t_{WP}	20	–	25	–	ns	–
Write Recovery Time	t_{WR}	0	–	0	–	ns	–
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Write to Output in High Z	t_{WHZ}	0	10	0	12	ns	*2
Data Valid to End of Write	t_{DW}	15	–	15	–	ns	–
Data Hold Time	t_{DH}	5	–	5	–	ns	–
Output Active from End of Write	t_{OW}	0	–	0	–	ns	–

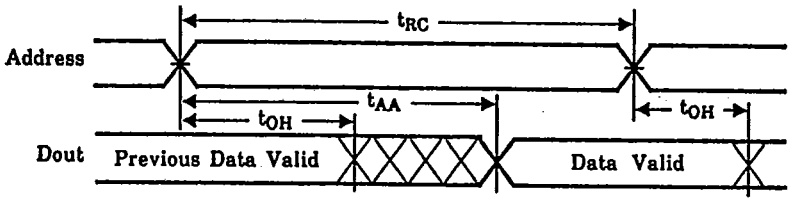
Notes) *1. These parameters are for HM6716.
*2. Transition is measured ±200mV from steady state voltage with Load(B).
This parameter is sampled and not 100% tested.

■ **Timing Waveforms**

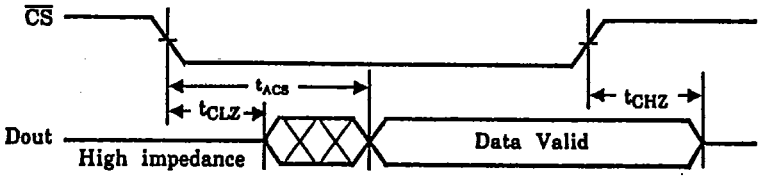
● **Read Cycle (1)**[*1]



● **Read Cycle (2)**[*1,*2,*4]



● **Read Cycle (3)**[*1,*3,*4]



Notes) *1. $\overline{WE}$ is High for Read Cycle.
*2. Device is continuously selected, $\overline{CS}$=V_{IL}.
*3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
*4. $\overline{OE}$=V_{IL}.

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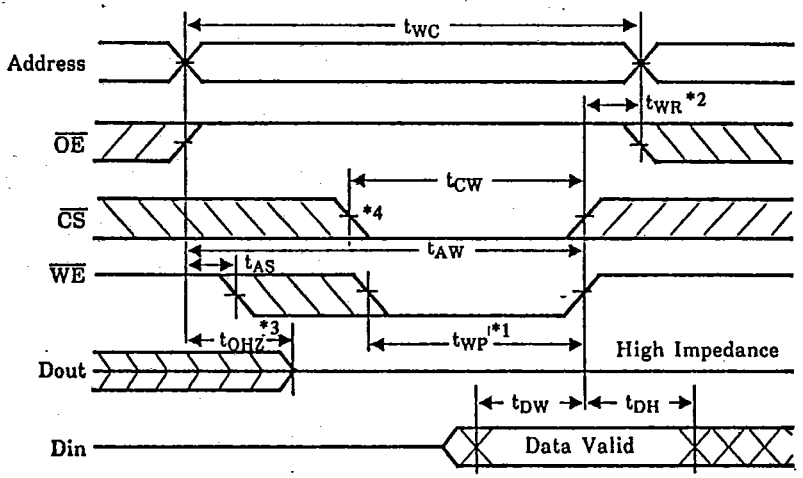
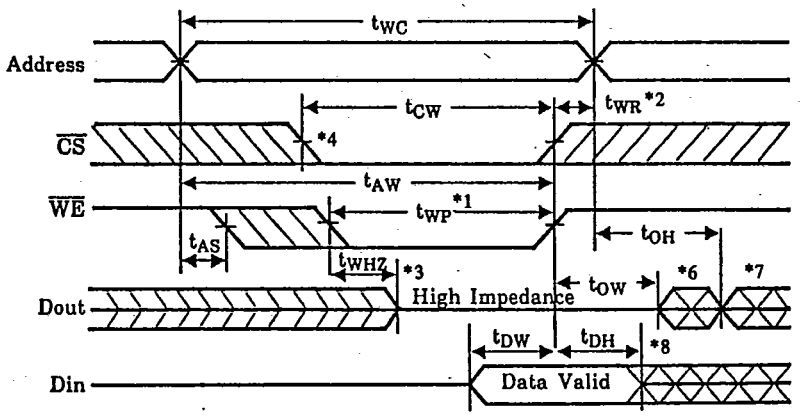
- **Write Cycle (1)**



- **Write Cycle (2)** *5



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL}).
*6. Dout is the same phase of write data of this write cycle.
*7. Dout is the read data of next address.
*8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.