HM6716, HM6719 Series

T-46-23-12

2048-word × 8-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

2048-word × 9-bit High Speed Hi-BiCMOS Static RAM

HITACHI/ LOGIC/ARRAYS/MEM

Features

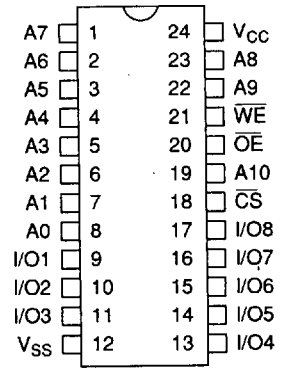
- Fast access time: 25/30 ns (max)
- Low power dissipation (DC): 280 mW (typ)
- +5 V single supply
- Completely static memory
- No clock or timing strobe required
- Fully TTL compatible input and output

Ordering Information

Type No.	Access time	Package
HM6716P-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6716P-30	30 ns	
HM6719P-25	25 ns	
HM6719P-30	30 ns	

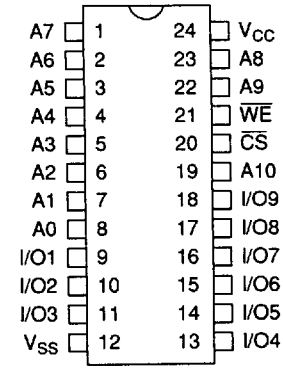
Pin Arrangement

HM6716 Series



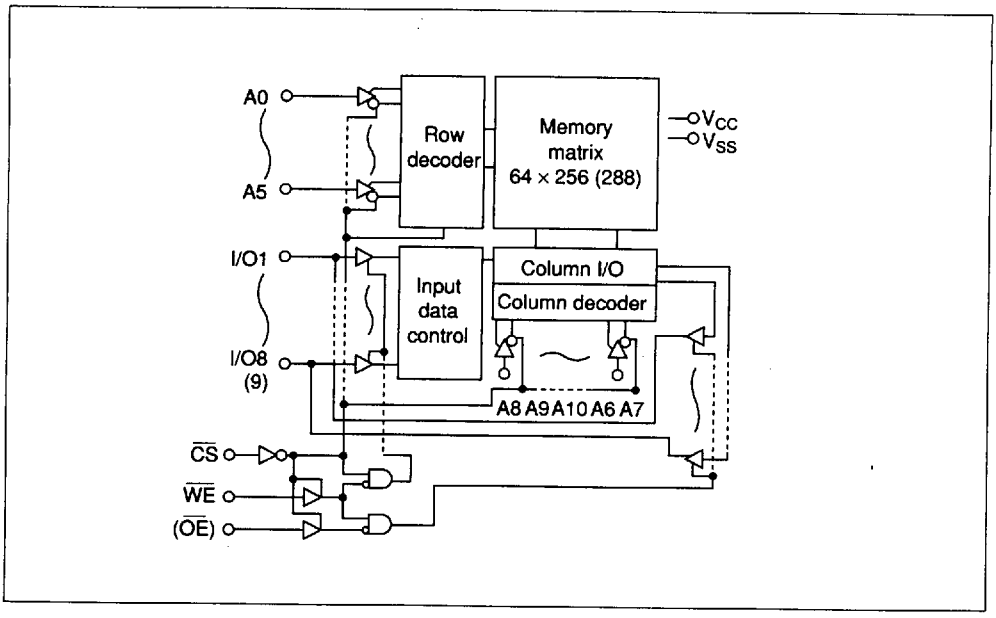
(Top view)

HM6719 Series



(Top view)

Block Diagram



Truth Table (HM6716)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	Pin	Reference cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read cycle 1–3
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write cycle 1
L	L	L	Write	I_{CC}, I_{CC1}	Din	Write cycle 2
L	H	H	Output disabled	I_{CC}, I_{CC1}	High Z	—

Truth Table (HM6719)

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} current	Pin	Reference cycle
H	H or L	Not selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Dout	Read cycle 2, 3
L	L	Write	I_{CC}, I_{CC1}	Din	Write cycle 1

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage to V_{SS} pin	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	6.0	V
Input low voltage	V_{IL}*	–3.0	—	0.8	V

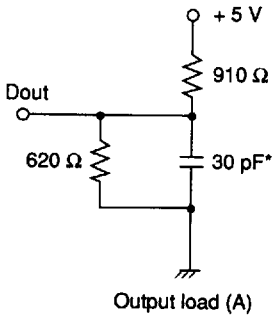
Note: Pulse width: 20 ns, DC: –0.5 V

DC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

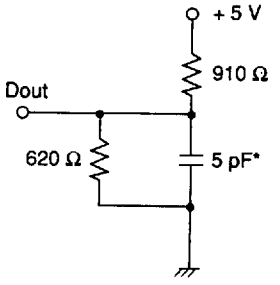
Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input leakage current	$\lvert I_{LI} \rvert$	—	—	2	µA	V_{CC} = 5.5 V, V_{IN} = V_{SS} to V_{CC}
Output leakage current	$\lvert I_{LO} \rvert$	—	—	2	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	130	mA	Min. cycle, duty: 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

AC Test Conditions:

- Input pulse levels: V_{SS} to 3.0 V
- Input and output reference levels: 1.5 V
- Input rise and fall time: 4 ns
- Output load: see figure



Output load (A)



Output load (B)
(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW}, t_{OHZ}, and t_{OLZ})

Note: Including scope and jig

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V	—	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	—	8	pF

AC Characteristics (V_{CC} 5 V ± 10%, Ta = 0 to +70°C, unless otherwise noted.)

Read Cycle

Parameter	Symbol	HM6716-25 HM6719-25 Min	HM6716-25 HM6719-25 Max	HM6716-30 HM6719-30 Min	HM6716-30 HM6719-30 Max	Unit	Notes
Read cycle time	t_{RC}	25	—	30	—	ns	—
Address access time	t_{AA}	—	25	—	30	ns	—
Chip select access time	t_{ACS}	—	25	—	30	ns	—
Chip selection to output in low Z	t_{CLZ}	0	—	0	—	ns	2
Output enable to output valid	t_{OE}	0	20	0	20	ns	1
Output enable to output in low Z	t_{OLZ}	0	—	0	—	ns	1, 2
Chip deselction to output in high Z	t_{CHZ}	0	10	0	12	ns	2
Chip disable to output in high Z	t_{OHZ}	0	10	0	10	ns	1, 2
Output hold from address change	t_{OH}	5	—	5	—	ns	—
Input voltage rise/fall time	t_T	—	150	—	150	ns	3

Write Cycle

Parameter	Symbol	HM6716-25 HM6719-25 Min	HM6716-25 HM6719-25 Max	HM6716-30 HM6719-30 Min	HM6716-30 HM6719-30 Max	Unit	Notes
Write cycle time	t_{WC}	25	—	30	—	ns	—
Chip selection to end of write	t_{CW}	20	—	25	—	ns	—
Address setup time	t_{AS}	0	—	0	—	ns	—
Address valid to end of write	t_{AW}	20	—	25	—	ns	—
Write pulse width	t_{WP}	20	—	25	—	ns	—
Write recovery time	t_{WR}	0	—	0	—	ns	—
Output disable to output in high Z	t_{OHZ}	0	10	0	10	ns	1, 2
Write to output in high Z	t_{WHZ}	0	10	0	12	ns	2

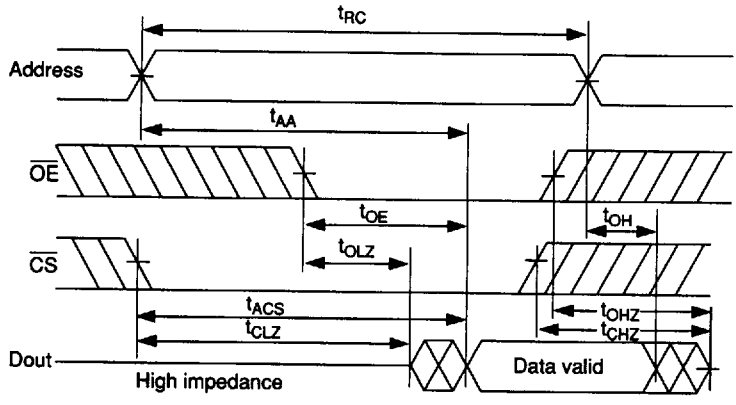
Write Cycle (cont)

Parameter	Symbol	HM6716-25 HM6719-25 Min	Max	HM6716-30 HM6719-30 Min	Max	Unit	Notes
Data valid to end of write	t_{DW}	15	—	15	—	ns	—
Data hold time	t_{DH}	5	—	5	—	ns	—
Output active from end of write	t_{OW}	0	—	0	—	ns	2

Note: 1. These parameters are for HM6716.
2. Transition is measured ±200 mV from steady state voltage with load (B). These parameters are sampled and not 100% tested.
3. Please contact your nearest Hitachi Sales Deptartment regarding specifications.

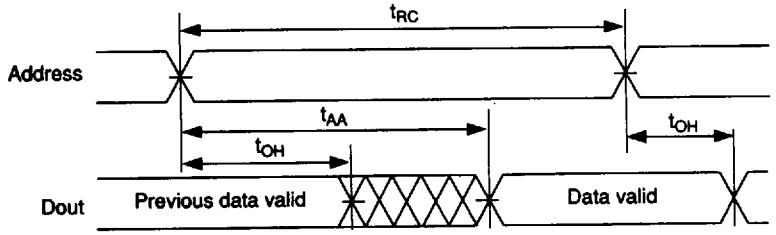
Timing Waveforms

Read Cycle 1



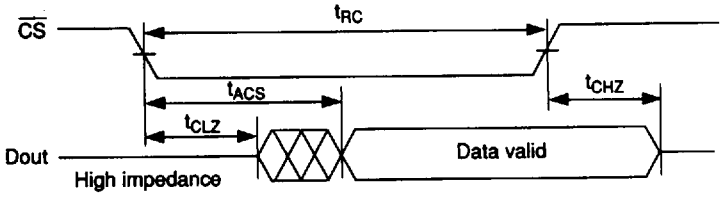
Note: WE is high for read cycle.

Read Cycle 2



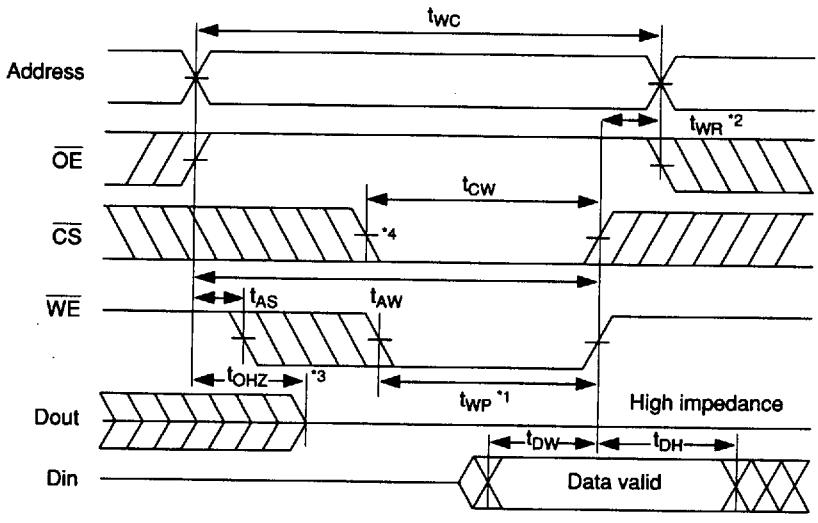
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = V_{IL}.
3. $\overline{OE}$ = V_{IL}.

Read Cycle 3



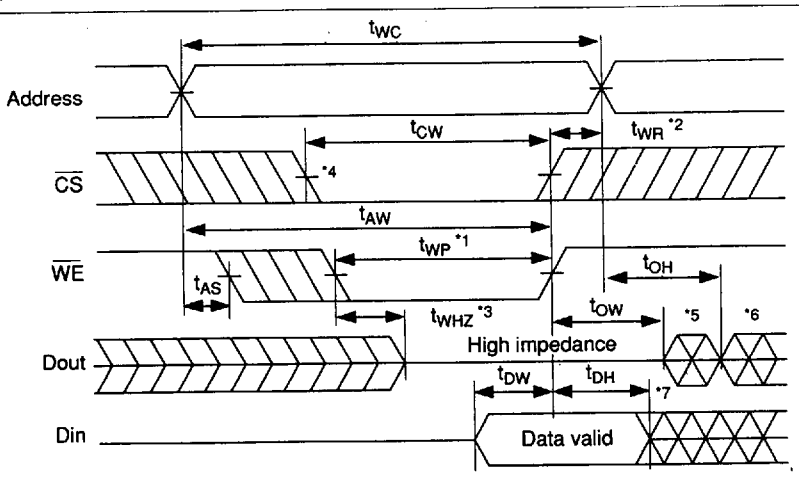
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.

Write Cycle 1



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs dimultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remains in a high impedance state.

Write Cycle 2*8



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. Dout is the same phase of write data of this write cycle.
6. Dout is the read data of next address.
7. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
8. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).