HM67B3632 Series

32k × 36 bit Synchronous Fast Static RAM with Burst Counter and Self-Timed Write

Product Preview
Rev. 8
Nov. 13, 1995

HITACHI

Descriptions

The Hitachi HM67B3632 is a 1,179,648 bits density high performance synchronous static random access memory organized as 32k × 36 bit. This SRAM is designed to support high performance secondary cache for the i486 and Pentium™ based systems

This SRAM integrates input registers and a 2-bit counter to support Pentium™ burst sequence. All synchronous inputs including all addresses, all data inputs, three chip enables ($\overline{CE}$, CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$) and four byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) are registered and controlled by rising edge of external clock input (CLK).

Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) can initiate the burst operation. Burst Address Advance ($\overline{ADV}$) controls continued burst addresses generated internally. Asynchronous Output Enable ($\overline{OE}$) enables all data outputs, which are also asynchronous.

Address, input data and write control are registered to support self-timed write function. Four byte write enables allow individual byte write.

The HM67B3632 operates from +3.3V power supply, and all inputs and outputs are LV-TTL compatible.

Features

- Single 3.3V power supply (LV-TTL)
- Fast access times : 9/10/11/12ns(max)
- Individual byte write control
- Internal input registers
  (Address, Data, Control)
- Internal self-timed write cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ burst control pins
  (i486/Pentium™ burst sequence)
- Asynchronous output enable controlled three-state outputs
- Common data inputs and data outputs
- High board density 100-lead QFP package and 100-lead LQFP package
- 5V -tolerant I/O

i486 and Pentium are trademarks of Intel Corp.
All power supply and ground pins must be connected for proper operation of the device.
This document contains information on a new product.
Specifications and information contained herein are subject to change without notice.

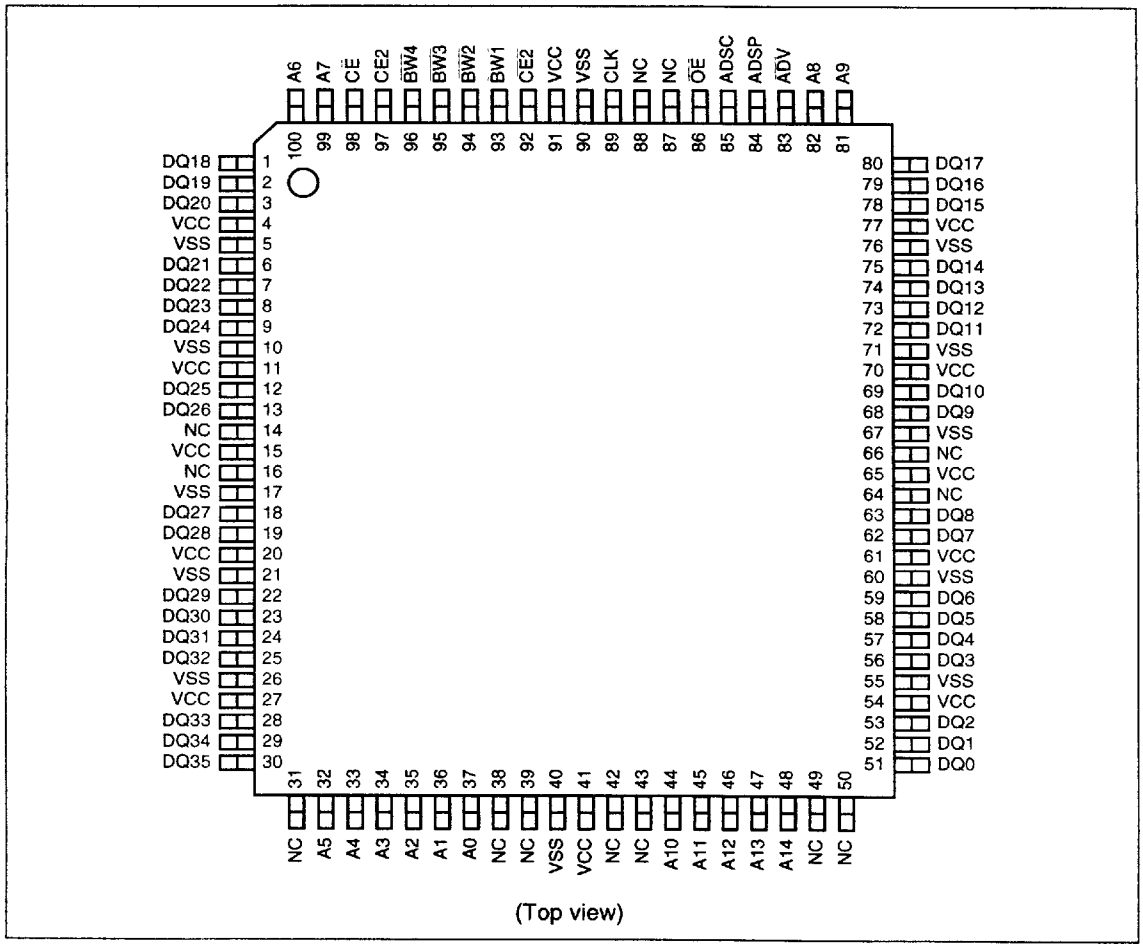
Hitachi semiconductor

ADE-203-237H(Z)

Ordering Information

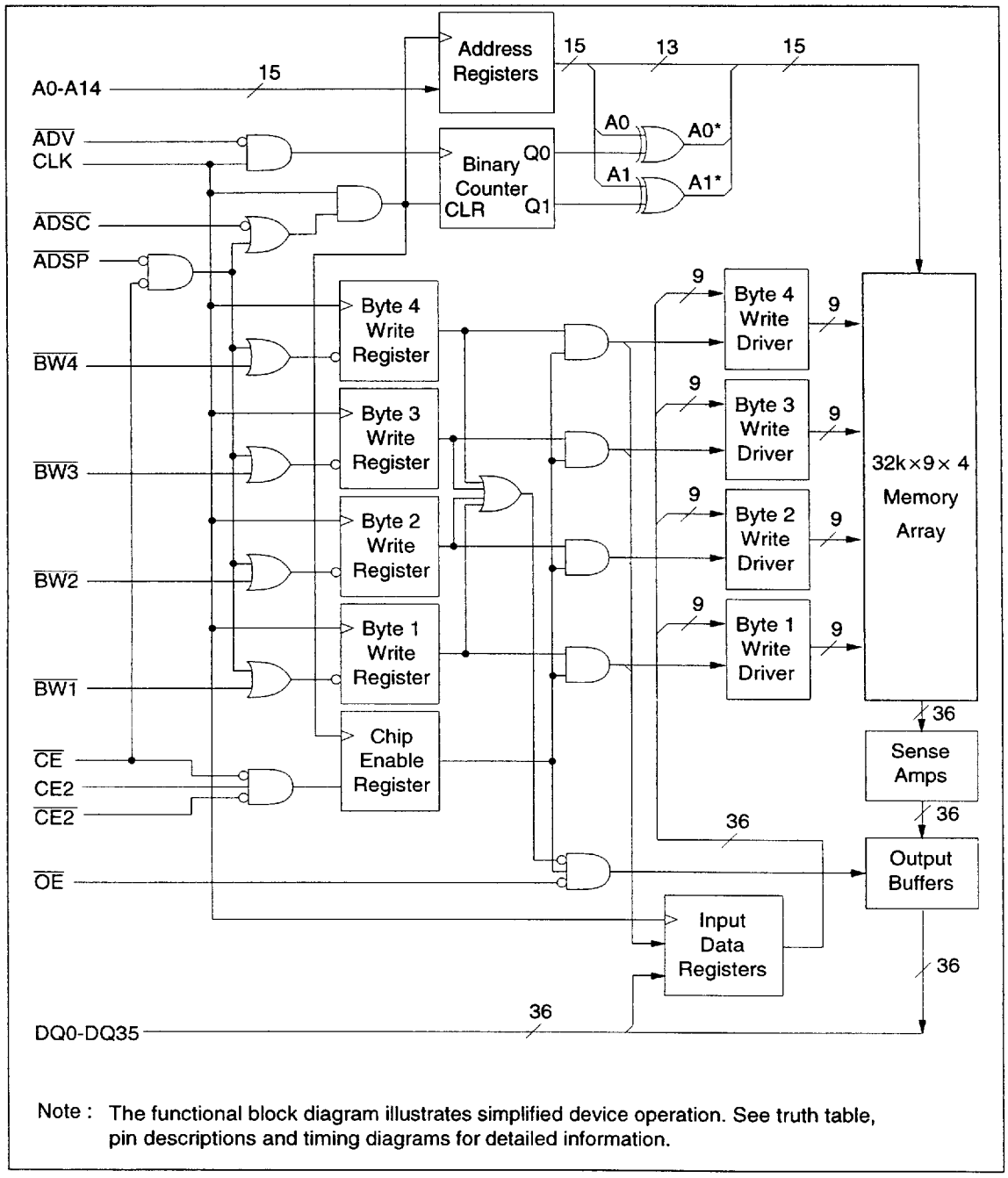
Type Number	Access Time	CPU Clock Rate	Package
HM67B3632FP-9	9ns	66MHz	LQFP 100pin
HM67B3632FP-10	10ns	60MHz	(FP-100H)
HM67B3632FP-11	11ns	60MHz	
HM67B3632FP-12	12ns	50MHz	

Pin Arrangement



(Top view)

Block Diagram



Note : The functional block diagram illustrates simplified device operation. See truth table, pin descriptions and timing diagrams for detailed information.

Pin Descriptions

LQFP pin number(s)	Symbol	Type	Description
37,36,35,34,33,32,100 99,82,81,44,45,46,47,48	A0 - A14	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times around the rising edge of CLK.
93,94,95,96	$\overline{BW1}$,$\overline{BW2}$ $\overline{BW3}$,$\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a write cycle and HIGH for a read cycle. $\overline{BW1}$ controls DQ0-DQ8. $\overline{BW2}$ controls DQ9-DQ17. $\overline{BW3}$ controls DQ18-DQ26. $\overline{BW4}$ controls DQ27-DQ35. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal latches the address, data, chip enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enables: This active low input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active low input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active high input is used to enable the device. This input is sampled when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active low asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active low input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A high on this pin effectively causes wait status to be generated (no address advance). This pin must be high at the rising edge of the first clock after an ADSP cycle is initiated if a write cycle is desired (to ensure use of correct address).

Pin Descriptions (continued)

LQFP pin number(s)	Symbol	Type	Description
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active low input interrupts any ongoing burst, causing a new external address to be latched. A read performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE2}$ and CE2. $\overline{ADSP}$ is ignored if $\overline{CE}$ is high. Power down state is entered if CE2 is low or $\overline{CE2}$ is high.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active low input interrupts any ongoing burst and causes a new external address to be latched. A read or write is performed using a new address if all chip enables are active. Power down state is entered if one or more chip enables are inactive.
14,16,31,38,39,42 43,49,50,64,66,87,88	NC	—	No Connect: These pins are internally not connected.
51,52,53,56,57,58,59, 62,63,68,69,72,73,74, 75,78,79,80,1,2,3,6,7,8, 9,12,1318,19,22,23,24, 25,28,29,30	DQ0-DQ35	Input/ Output	Data Input / Output: Byte1 is DQ0-DQ8; Byte 2 is DQ9-DQ17; Byte 3 is DQ18-DQ26; Byte 4 is DQ27-DQ35. Input data must meet setup and hold times around the rising edge of CLK.
4,11,15,20,27,41,54, 61,65,70,77,91	VCC	Supply	Power Supply: +3.3V±5%.
5,10,17,21,26,40 55,60,67,71,76,90	VSS	Supply	Ground: GND

Burst Sequence Table

External Address	A14-A2	A1	A0
1st Burst Address	A14-A2	A1	A0
2nd Burst Address	A14-A2	$\overline{A1}$	A0
3rd Burst Address	A14-A2	A1	A0

Note: The burst wraps around to its initial state upon completion.

Truth Table

Operation	Address	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{BWi}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power down	None	L	H	X	H	L	X	X	X	L-H	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Notes: 1. H means logic High. L means logic Low. X means don't care for synchronous inputs, and H or L for asynchronous inputs. $\overline{BWi}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, or $\overline{BW4}$) are Low. $\overline{BWi}$=H means all byte write enables signals are High.
2. $\overline{BW1}$ enables writes to Byte1 (DQ0-DQ8). $\overline{BW2}$ enables writes to Byte2 (DQ9-DQ17). $\overline{BW3}$ enables writes to Byte3 (DQ18-DQ26). $\overline{BW4}$ enables writes to Byte4 (DQ27-DQ35).
3. All inputs except for $\overline{OE}$ must meet setup and hold times around the rising edge (L-H) of CLK.
4. Wait status are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be H before the input data required setup time and held H throughout the input data hold time.
6. $\overline{ADSP}$=L always initiates an internal Read at the L-H edge of CLK. A Write is performed by setting one or more byte write enable signals Low for the subsequent L-H edge of CLK. Refer to write timing diagram for clarification.

Asynchronous Truth Table

Operation	$\overline{OE}$	I/O Status
Read	L	Data out
Read	H	High-Z
Write	X	High-Z-Data in
Deselected	X	High-Z

Notes: 1. X means High or Low
2. For a write operation following a read operation. $\overline{OE}$ must be high before the input data required setup time and held high throught the input data hold time.

Absolute Maximum Ratings

Items	Symbol	Rating	unit
Supply voltage	V_{CC}	-0.5 to +4.6	V
Voltage on any pins relative to V_{SS}	V_T	-0.5V to +6.0	V
Power dissipation	P_T	1.4	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage temperature range	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions (Ta=0 to +70°C)

Items	Symbol	min.	max.	unit
Supply voltage(Operating voltage range)	V_{CC}	3.135	3.465	V
Supply voltage to V_{SS}	V_{SS}	0.0	0.0	V
Input high voltage	V_{IH}	2.2	5.5	V
Input low voltage	V_{IL}	-0.5[1)]	0.8	V

Note: -2.0V for undershoot pulse width$\leq t_{KHKH}$min / 2.

Capacitance (f=1.0MHz, Ta=25°C)

Items	Symbol	min.	max.	unit
Input capacitance	C_{in}	—	5	pF
Input/Output capacitance	$C_{I/O}$	—	8	pF

Note: This parameter is sampled and not 100% tested.

DC and Operating Characteristics

(Vcc=3.3V± 5%, Ta=0 to 70°C , unless otherwise noted)

Item	Symbol	test conditions	min	typ	max	unit
Input leakage current	ILI	V_{IN}=Vss to Vcc	-	-	±2.0 1)	µA
Output leakage current	ILO	$\overline{OE}$=V_{IH}	-	-	±10.0 2)	µA
Supply current	Icc	Iout=0mA, all inputs=V_{IH} or V_{IL} cycle time ≧ t_{KHKH}min	-	-	250	mA
Stanby current	I_{SB}(IDOL)	Device selected, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≧ V_{IH} other inputs=V_{IH} or V_{IL} cycle time ≧ t_{KHKH}min	-	-	80	mA
	I_{SB}DC(CMOS)	$\overline{CE}$=V_{IH}, Vcc=MAX all inputs ≦ Vss+0.2 or ≧ Vcc-0.2 all inputs static, CLK frequency=0	-	7	10	mA
	I_{SB}DC(TTL)	$\overline{CE}$=V_{IH}, Vcc=max all inputs ≦ VIL or ≧ V_{IH} min all inputs static, CLK frequency=0	-	16	30	mA
	I_{SB}(AC)	$\overline{CE}$=V_{IH}, $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ ≦ V_{IL} other input ≦ V_{IL} or ≧ V_{IH}, Vcc=max CLK frequency ≦ 66.6MHz	-	120	190	mA
	I_{SB}(AC)	$\overline{CE}$=V_{IH}, $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ ≦ V_{IL} other input ≦ V_{IL} or ≧ V_{IH}, Vcc=max CLK frequency ≦ 30MHz	-	50	80	mA
	I_{SB}(CK RUN)	Device deselected $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≧ V_{IH} other input ≦ V_{IL} or ≧ V_{IH}, Vcc=max CLK frequency ≦ 66.6MHz	-	60	100	mA
	I_{SB}(CK RUN)	Device deselected $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≧ V_{IH} other input ≦ V_{IL} or ≧ V_{IH}, Vcc=max CLK frequency ≦ 30MHz	-	30	50	mA
Output low voltage	V_{OL}	I_{OL}=8mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-4mA	2.4	-	-	V

Notes : 1. ±100µA for Vin ≦ 5.5V
2. ±100µA for Vout ≦ 5.5V

AC Characteristics (Vcc=3.3V± 5%, Ta=0 to 70°C, unless otherwise noted)

Items	Symbol Standard	Symbol Alternate	-9 min	-9 max.	-10 min.	-10 max.	-11 min.	-11 max.	-12 min	-12 max	unit	Notes
Cycle time	t_{KHKH}	t_{CYC}	15	—	15	—	15	—	20	—	ns	
Clock access time	t_{KHQV}	t_{ACK}	—	9	—	10	—	11	—	12	ns	1
Output enable to output valid	t_{GLQV}	t_{OE}	—	5	—	5	—	5	—	6	ns	5
Clock high to output active	t_{KHQX1}	t_{CLZ}	4	—	4	—	4	—	4	—	ns	
Clock high to output change	t_{KHQX2}	t_{COH}	3	—	3	—	3	—	3	—	ns	
Output enable to output active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	
Output disable to output high-Z	t_{GHQZ}	t_{OHZ}	1	6	1	6	1	6	1	6	ns	2
Clock high to output high-Z	t_{KHQZ}	t_{CHZ}	—	6	—	6	—	6	—	6	ns	2
Clock high pulse width	t_{KHKL}	t_{CH}	5	—	5	—	5	—	5	—	ns	
Clock low pulse width	t_{KLKH}	t_{CL}	5	—	5	—	5	—	5	—	ns	
Setup times:			2.5	—	2.5	—	2.5	—	2.5	—	ns	3,4
Address	t_{AVKH}	t_{SA}										
Address status	t_{ADSVKH}	t_{SADS}										
Input data	t_{DVKH}	t_{SD}										
Byte write	t_{WVKH}	t_{SW}										
Address advance	t_{ADVVKH}	t_{SADV}										
Chip Enable	t_{EVKH}	t_{SCE}										
Hold times:			0.5	—	0.5	—	0.5	—	0.5	—	ns	3,4
Address	t_{KHAX}	t_{HA}										
Address status	t_{KHADSX}	t_{HADS}										
Input data	t_{KHDX}	t_{HD}										
Byte write	t_{KHWX}	t_{HW}										
Address advance	t_{KHADVX}	t_{HADV}										
Chip Enable	t_{KHEX}	t_{HCE}										

Notes:
1. Maximum access times are guaranteed for all possible i486™ external bus cycles.
2. Transition is measured ±200mV from steady-state voltage with load of Fig. B. This parameter is sampled.
3. A read cycle is defined by byte write enables all high or $\overline{ADSP}$ low for the required setup and hold times. A write cycle is defined by at least one byte write enable low and $\overline{ADSP}$ high for the required setup and hold times.
4. This is a synchronous device. All address must meet the specified setup and hold times for all rising edge of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is low and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edge of CLK when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.
5. $\overline{OE}$ is a " don't care (H or L)" when a byte write enable is sampled low.

AC Test Conditions

Input timing measurement reference levels.....1.5V

Input pulse levels.....0 to 3.0V

Input rise / fall time.....2ns

Output timing reference level.....1.5V

Output Load.....See Figure A unless otherwise noted

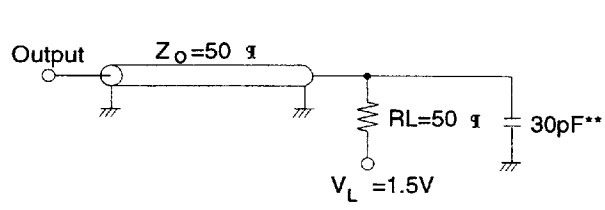


Figure A

** (including the capacitance of tester and jig)

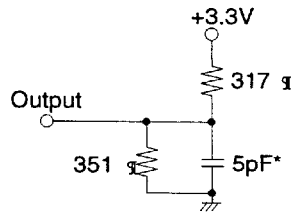
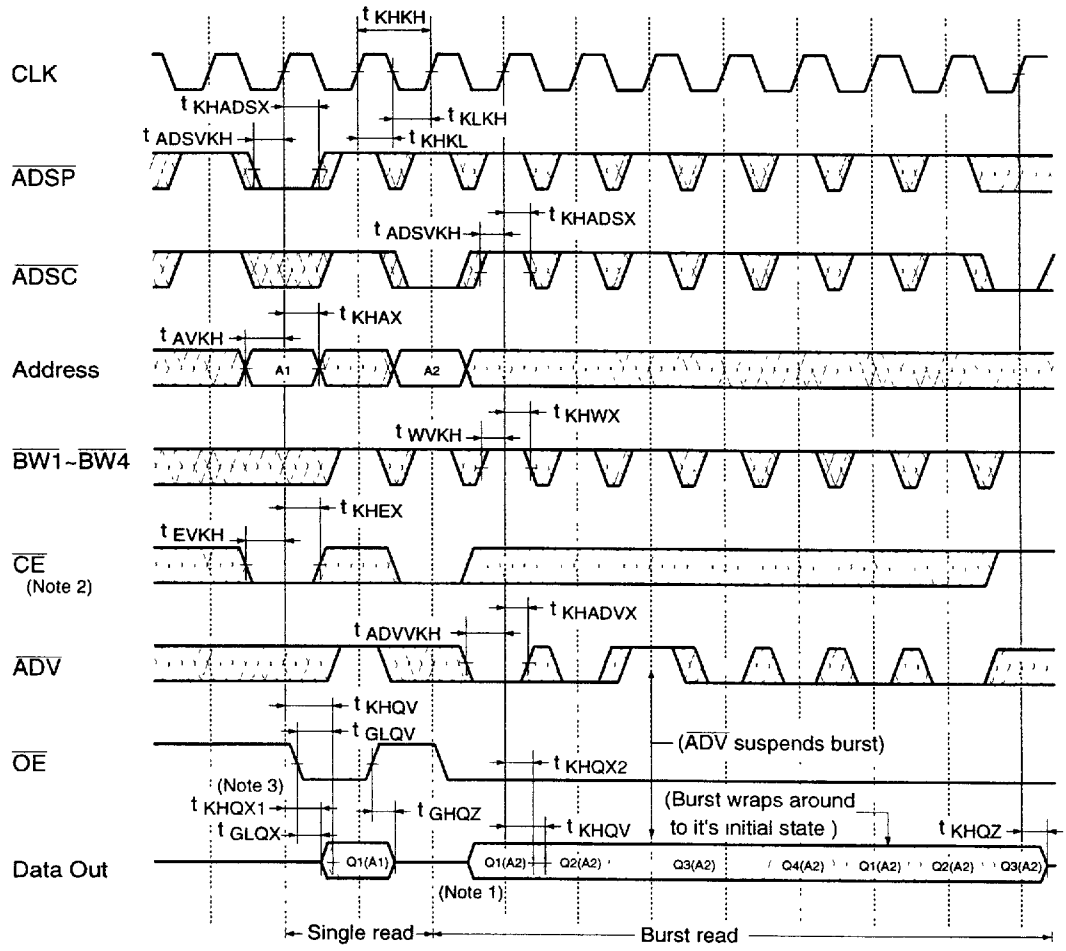


Figure B

* (including scope and jig)

Read Cycle

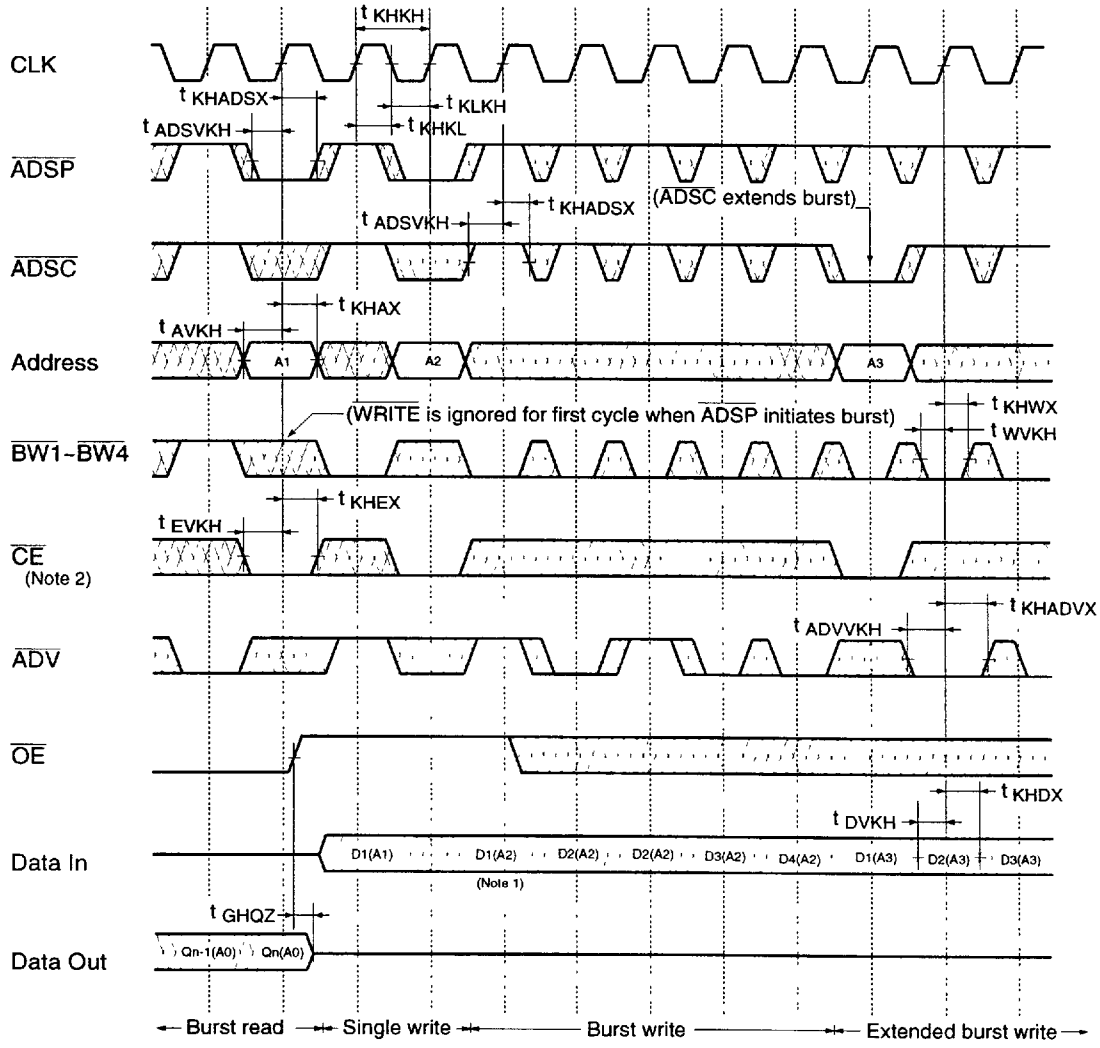


Notes : 1. Q1(A2) represents the first outputs data from the base address A2; Q2(A2) represents the next outputs data in the burst sequence with A2 as the base address.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. When $\overline{CE}$ is low, CE2 is low and CE2 is high. When $\overline{CE}$ is high, CE2 is high and CE2 is low.

3. t_{KHQX1} is defined as the transition time from clock high to output active when a device goes to be selected by $\overline{CE}$ or $\overline{CE2}$ or CE2.

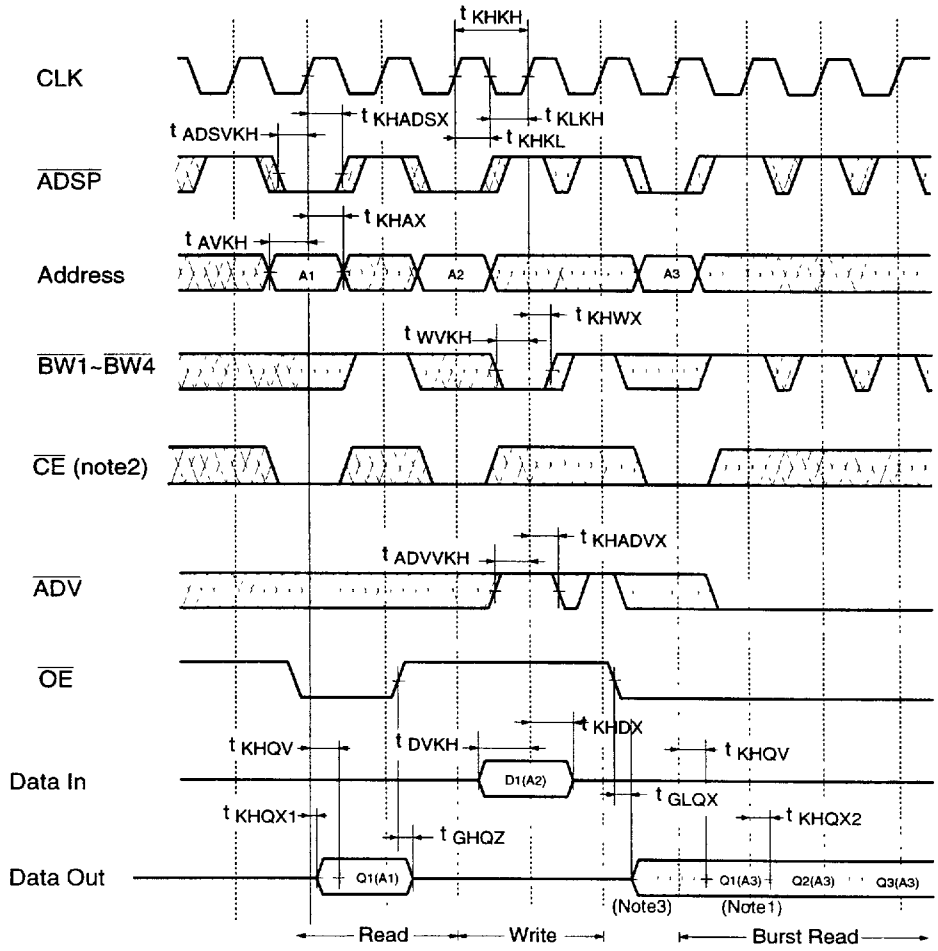
Write Cycle



Notes : 1. D1(A2) represents the first inputs data for the base address A2 ; D2(A2) represents the next inputs data in the burst sequence with A2 as the base address.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. When $\overline{CE}$ is low, CE2 is low and CE2 is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and CE2 is low.

Combination Read / Write Cycle



Notes : 1. Q1(A3) represents the first outputs data for the base address A3 ; Q2(A3) represents the next outputs data in the burst sequence with A3 as the base address.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. When CE is low, $\overline{CE2}$ is low and CE2 is high. When $\overline{CE}$ is high, $\overline{CE2}$ is high and CE2 is low.

3. After write cycle, following Read cycle output Data(Q) is undefined unless an $\overline{ADSP}$, $\overline{ADSC}$, or $\overline{ADV}$ cycle is performed.

Application Examples

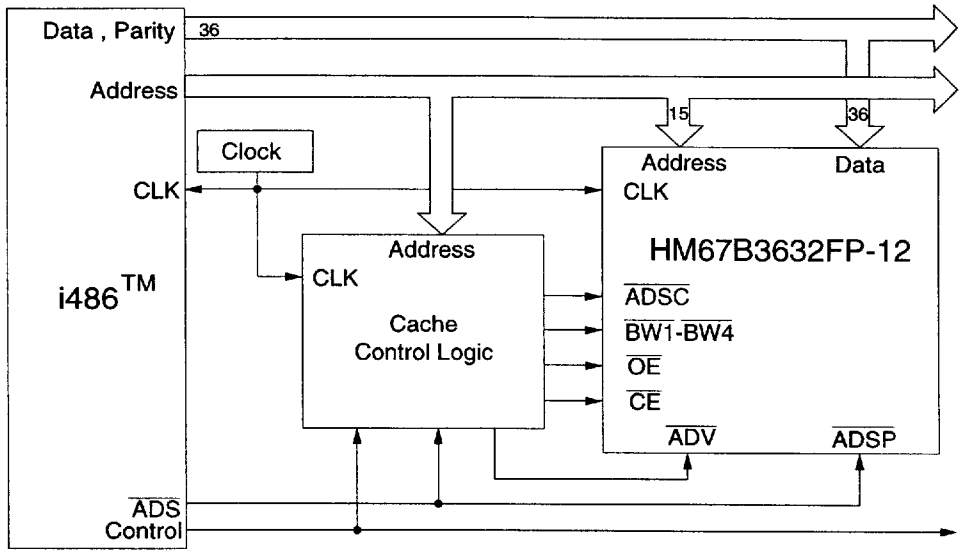


Figure1
128K byte secondary cache with burst for 50MHz 80486™ using one HM67B3632FP-12 synchronous SRAM.

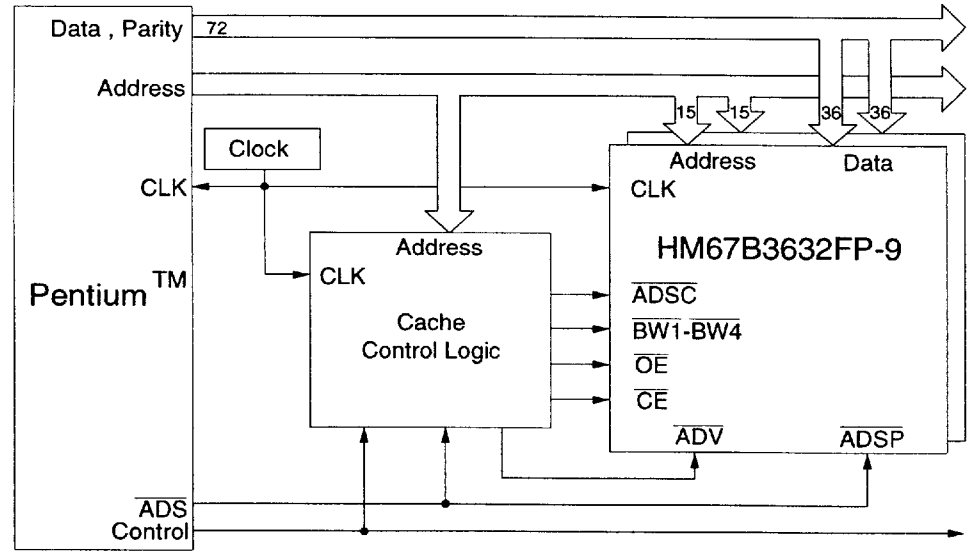
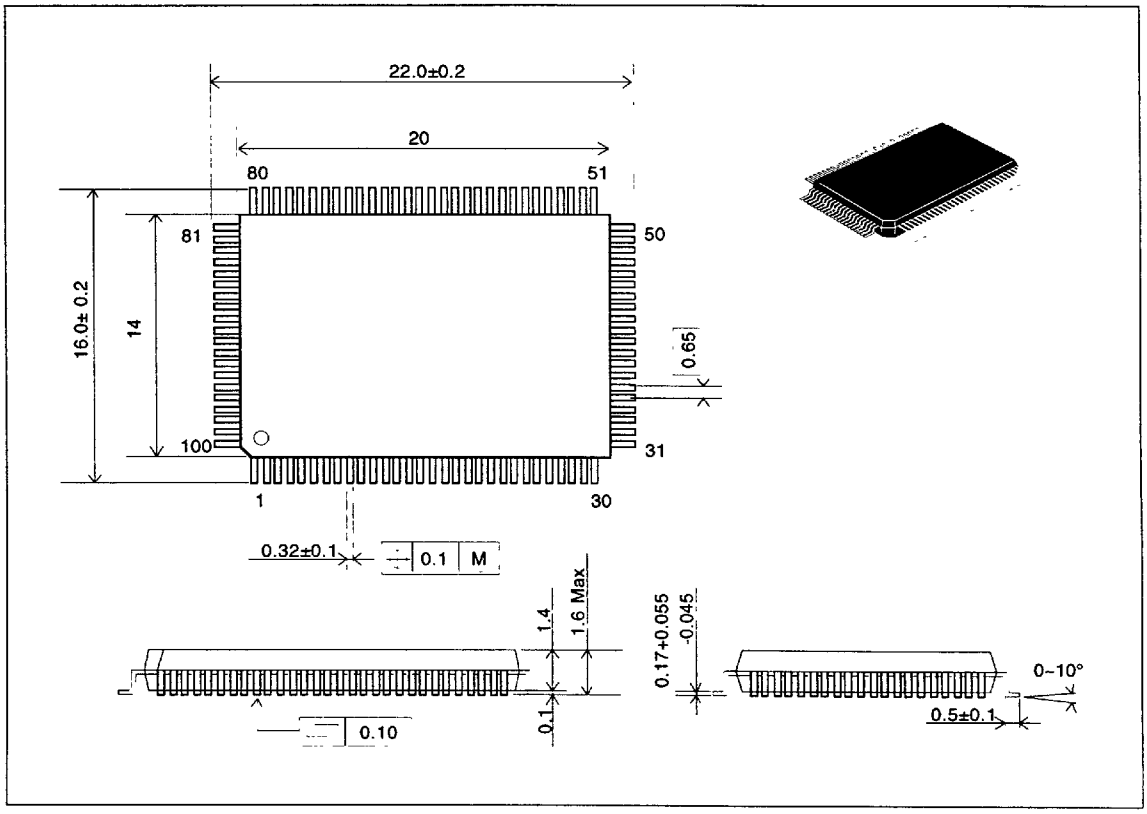


Figure2
256K byte secondary cache with burst for 66MHz Pentium™ using two HM67B3632FP-9 synchronous SRAM.

Package Dimensions

• **FP-100H**

Unit: mm



Revision Record

Revision	Date	Content of modification
0	Mar.31,1994	Initial release
1	Aug.26,1994	Change package form FP100A to FP100G. Revise address A2 to A3 in Write cycle timing. Revise burst write to burst read in combination timing. Change output load B for 3.3V.
2	Oct.20,1994	Add the spec of V_{OH} and V_{OL} Revise $\overline{ADSP}$, $\overline{ADSC}$ in Read cycle timing Revise $\overline{ADSP}$, $\overline{ADV}$ in Write cycle timing Revise address A2 to A1 in Write cycle timing. Change I_{CC} spec 190mA to 250mA Revise the error in I_{SB} test condition
3	Oct.28,1994	Add the spec of I_{SB}(CK RUN) Change t_{KHQX1} from 2ns to 4ns Change load condition including 30pF
4	Dec.27,1994	Add the type Number of HM67B3632FP1-11 and HM67B3632FP-11 Revise the Combination Read/Write cycle timing chart Add the comment "After Write cycle, following Read cycle Output Data(Q) is undefined unless an $\overline{ADSP}$, $\overline{ADSC}$, or $\overline{ADV}$ cycle is performed." Revise the Address of Hitachi Ltd. Vcc=3.3V±0.3V to 3.3V±5% ILO=±2.0μA to ±10.0μA t_{GHQZ}min=2ns to 1ns
5	Feb.20,1995	Revise pin number for DQ0-DQ35, Vcc and Vss in P5. Change the CPU Clock Rate of HM67B3632FP1-10/11, HM67B3632FP-10/11 66MHz to 60MHz
6	Feb 28,1995	Add the notes of t_{KHQZ} is "2" Add the Note3 on Read Cycle timing chart
7	Mar.30,1995	Revise the hight of FP-100H 1.7max to 1.6max Add the LQFP in pin Description
8	Nov. 13,1995	Delete Type Number HM67B3632FP1-* Add 5V tolerant I/O V_{IH}max Vcc+0.5 to 5.5