



**HITTITE
MICROWAVE
CORPORATION**

**GaAs MMIC
Low Distortion
Diversity Switch**

HMC160S14

JUNE 1996

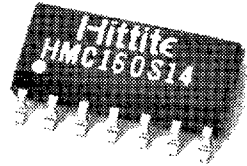
Features

HIGH THIRD ORDER INTERCEPT +54 dBm

SINGLE POSITIVE SUPPLY +3 TO +8V

HIGH POWER CAPABILITY

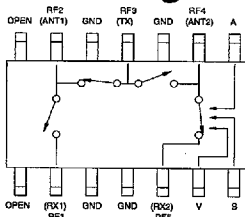
TTL/CMOS CONTROL



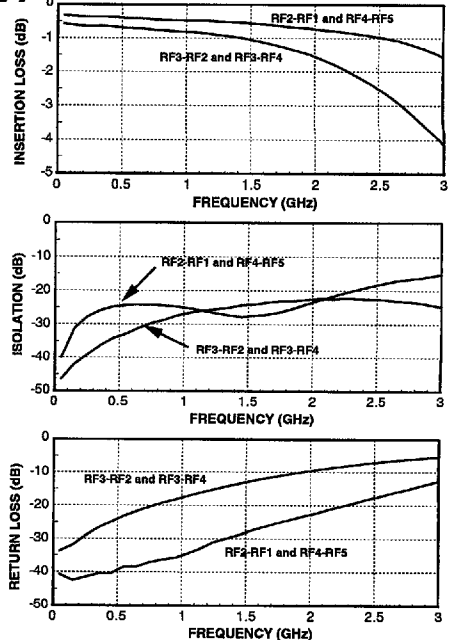
General Description

The HMC160S14 is a low-cost diversity switch in a 14-lead SOIC package for use in transmit-receive applications which require very low distortion at high signal power levels. The device can control signals up to 2.0GHz and is especially suited for 900MHz applications. The switch is used to exchange two antennae between transmitter and two receivers, providing system diversity. The design has exceptional intermodulation performance; providing a +54 dBm third order intercept at 8 Volt bias. On-chip circuitry allows single positive supply operation at very low DC current with control inputs compatible with CMOS and most TTL logic families.

Functional Diagram



Typical Performance



Electrical Performance

PARAMETER	Path	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	RF2-RF1, RF4-RF5	DC - 1.0GHz		0.5	0.8	dB
		DC - 2.0GHz		0.8	1.1	dB
	RF3-RF2, RF3-RF4	DC - 1.0GHz		0.9	1.2	dB
		DC - 2.0GHz		1.6	1.9	dB
Isolation	ALL	DC - 1.0GHz	21	24		dB
		DC - 2.0GHz	19	22		dB
	RF2-RF1, RF4-RF5	DC - 1.0GHz	25	35		dB
		DC - 2.0GHz	17	22		dB
Return Loss	RF3-RF2, RF3-RF4	DC - 1.0GHz	15	18		dB
		DC - 2.0GHz	7.0	9.5		dB
	ALL	0.5 - 1.0GHz	33	35		dBm
		0.5 - 2.0GHz	31	33		dBm
Input Power for 1dB Compression 0/8V Ctl	ALL	0.5 - 1.0GHz	50	55		dBm
		0.5 - 2.0GHz	47	54		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	ALL	DC - 2.0GHz		22		ns
				50		ns

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Low Distortion
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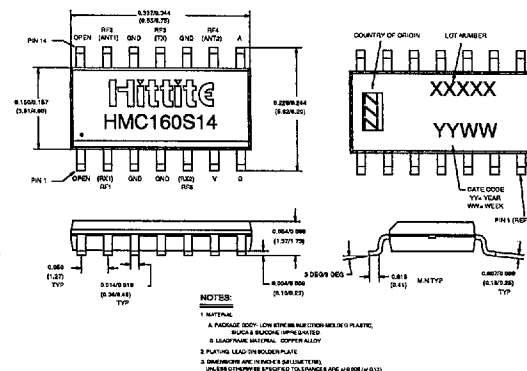
HMC160S14

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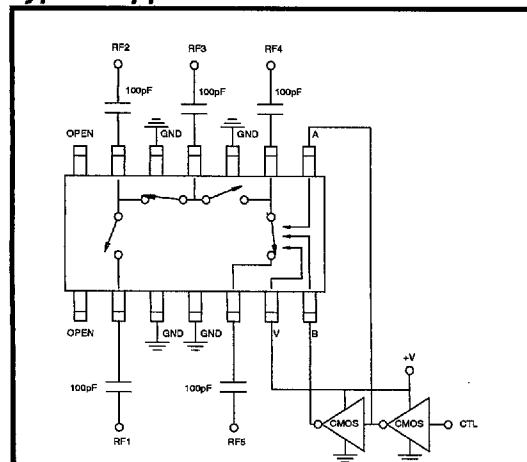
Absolute Maximum Ratings

Bias Voltage Range (Port V)	-0.2 to +12 Vdc
Control Voltage Range (A & B)	-0.2 to +12 Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 deg C

Outline



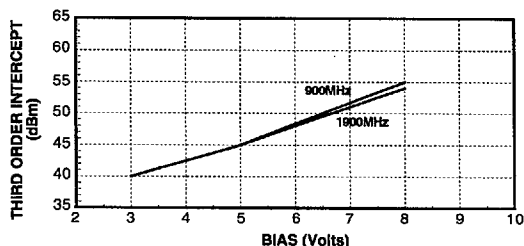
Typical Application Circuit



Notes:

1. Control inputs A and B can be driven directly with CMOS logic (HC) with V of 3 to 8 Volts applied to the CMOS logic gates and to pin V of the RF switch.
2. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
3. Highest RF signal power capability is achieved with V set to +8V. However, the switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.
4. Set V to 5 Volts and use HCT series logic to provide a TTL driver interface.

Distortion vs Bias Voltage



1 Watt Carrier at 900MHz			1 Watt Carrier at 1900MHz		
Bias (Volts)	Third Order Intercept (dBm)	Second Harmonic (dBc)	Third Order Intercept (dBm)	Second Order Intercept (dBm)	Second Harmonic (dBc)
3	40	68	40	81	56
5	45	77	45	90	62
8	55	84	54	90	66

Compression vs Bias Voltage

RF Path RF1-RF2 and RF4-RF5				
Carrier at 900MHz		Carrier at 1900MHz		
Bias (Volts)	Input Power for 0.1dB Compression (dBm)	Input Power for 1dB Compression (dBm)	Input Power for 0.1dB Compression (dBm)	Input Power for 1dB Compression (dBm)
3	25	29	24	28
5	29	34	28	32
8	32	36	31	35

RF Path RF2-RF3 and RF3-RF4				
Carrier at 900MHz		Carrier at 1900MHz		
Bias (Volts)	Input Power for 0.1dB Compression (dBm)	Input Power for 1dB Compression (dBm)	Input Power for 0.1dB Compression (dBm)	Input Power for 1dB Compression (dBm)
3	24	28	23	27
5	28	33	27	31
8	31	35	30	33

Caution: Do not operate in 1dB compression at power levels above +35dBm.

Truth Table

Control Input		Signal Path State			
A	B	RF1-RF2	RF2-RF3	RF3-RF4	RF4-RF5
Low	High	ON	OFF	ON	OFF
High	Low	OFF	ON	OFF	ON

State	Bias Condition
Low	0 to 0.2V @ 20uA Max.
High	+3V @ 50uA Typ to +8V @ 500uA Max

Logic High control voltage must be in the range of V-0.2 to V where V is the applied bias voltage. Recommended bias voltage V is +3 to +8 Volts.

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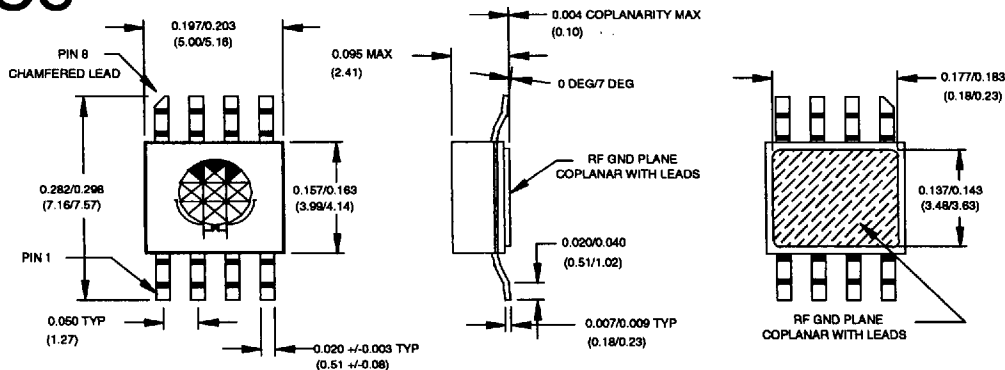
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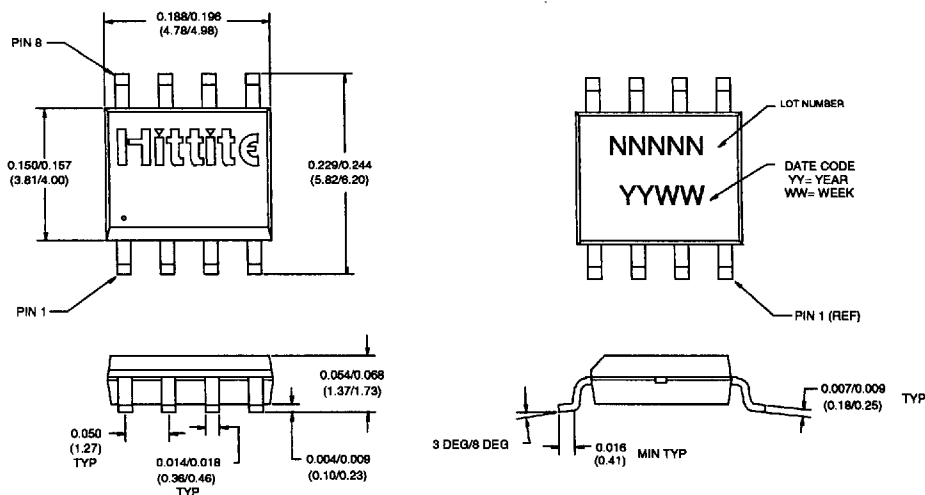
C8



NOTES: FOR 8 LEAD CERAMIC PACKAGE

1. MATERIAL:
A. PACKAGE BODY & COVER: WHITE ALUMINA (92%)
B. LEADS & PACKAGE BOTTOM: COPPER
2. PLATING: ELECTROLYTIC GOLD 100-200 MICRONS OVER
ELECTROLYTIC NICKEL 100 TO 250 MICRONS OVER
3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED
ALL TOLERANCES ARE +/- 0.005 (+/- 0.13)
4. THE PACKAGE BOTTOM, RF GROUND, MUST BE SOLDERED
OR CONDUCTIVE EPOXYED TO THE PCB RF GROUND.
5. NON-HERMETIC EPOXY SEALED COVER
6. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE
C8 PACKAGED PRODUCTS.

S8



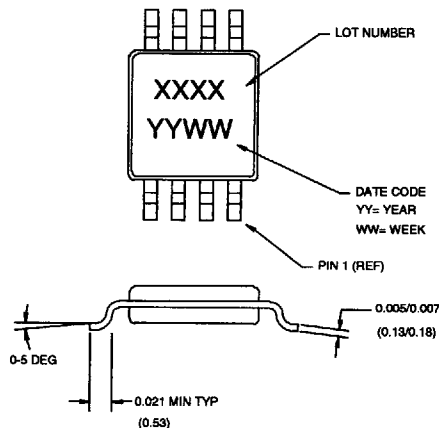
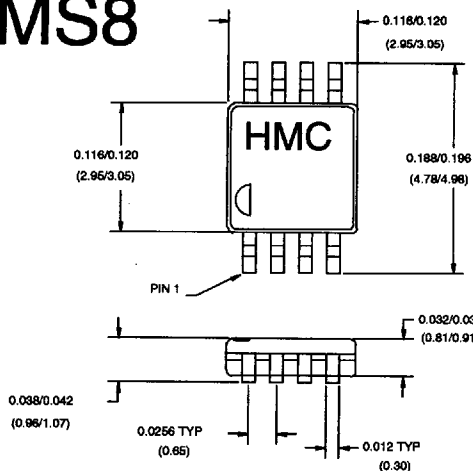
NOTES: FOR 8 LEAD SOIC PACKAGE

1. MATERIAL:
A. PACKAGE BODY: LOW STRESS INJECTION-MOLDED PLASTIC,
SILICA & SILICONE IMPREGNATED.
B. LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS),
UNLESS OTHERWISE SPECIFIED TOLERANCES ARE +/- 0.005 (+/- 0.13)
4. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE
S8 PACKAGED PRODUCTS.



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MS8



NOTES: FOR 8 LEAD MSOP

1. MATERIAL:

A. PACKAGE BODY: LOW STRESS INJECTION-MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED.

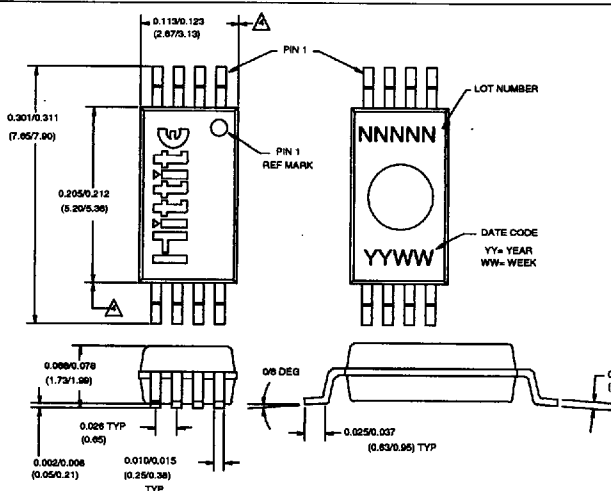
B. LEADFRAME MATERIAL: COPPER ALLOY

2. PLATING: LEAD-TIN SOLDER PLATE

3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED TOLERANCES ARE ± 0.005 (± 0.13)

4. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE MS8 PACKAGED PRODUCTS.

SS8



NOTES: FOR 8 LEAD SSOP

1. MATERIAL:

A. PACKAGE BODY: LOW STRESS INJECTION-MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED.

B. LEADFRAME MATERIAL: COPPER ALLOY

2. PLATING: LEAD-TIN SOLDER PLATE

3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED TOLERANCES ARE ± 0.005 (± 0.13)

△ THESE ARE REFERENCE DIMENSIONS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 (0.15) PER SIDE.

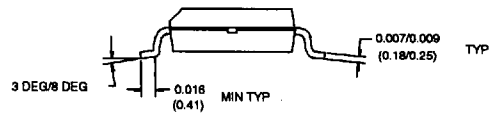
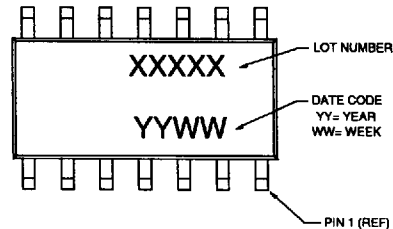
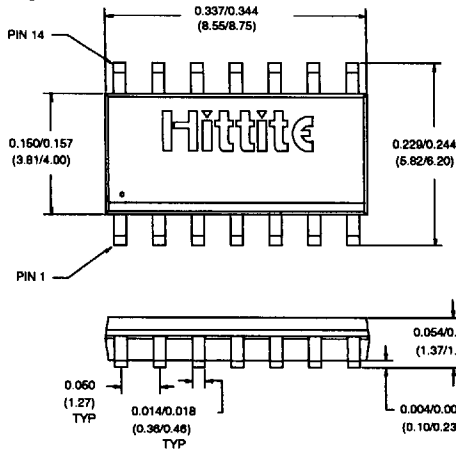
5. COPLANARITY: LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.003 (0.08) AT SEATING PLANE.

6. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE SS8 PACKAGED PRODUCTS.



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S14



NOTES: FOR 14 LEAD SOIC PACKAGE

1. MATERIAL:

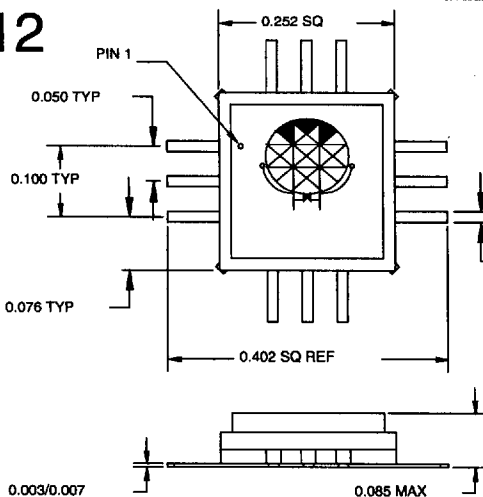
- A. PACKAGE BODY: LOW STRESS INJECTION-MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED.
- B. LEADFRAME MATERIAL: COPPER ALLOY

2. PLATING: LEAD-TIN SOLDER PLATE

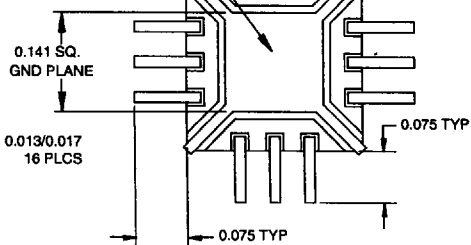
3. DIMENSIONS ARE IN INCHES (MILLIMETERS);
UNLESS OTHERWISE SPECIFIED TOLERANCES ARE
+/-0.005 (+/-0.13)

4. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE
S14 PACKAGED PRODUCTS.

C12



RF GND PLANE
SEE NOTE 5



NOTES: FOR 12 LEAD CERAMIC PACKAGE

1. MATERIAL:

- A. PACKAGE BODY & COVER: WHITE ALUMINA (99%)
- B. LEAD: KOVAR (or) ASTM F15 (ALLOY 42) EQUIVALENT
- 2. PLATING (LEADS): ELECTROLYTIC GOLD 25 MICROINCHES MINIMUM OVER ELECTROLYTIC NICKEL 100 TO 250 MICROINCHES
- 3. DIMENSIONS ARE IN INCHES. UNLESS OTHERWISE SPECIFIED ALL TOLERANCES ARE ±0.005.

4. NON-HERMETIC EPOXY SEALED COVER.

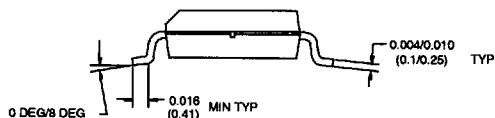
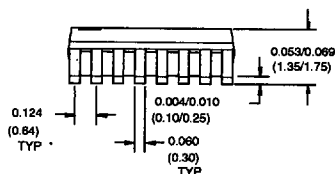
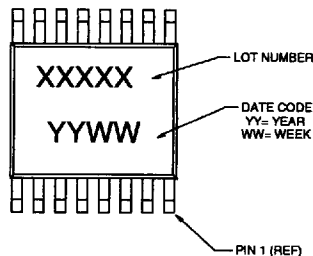
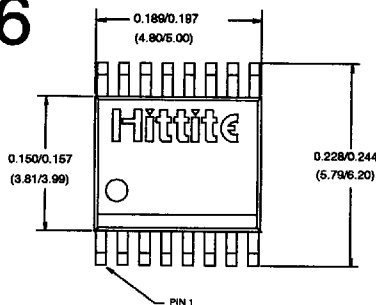
5. THE PACKAGE BOTTOM, RF GROUND, MUST BE
SOLDERED OR CONDUCTIVE EPOXIED TO THE RF PCB GROUND

6. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE
C12 PACKAGED PRODUCTS.



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QS16



NOTES: FOR 16 LEAD QSOP PACKAGE

1. MATERIAL:

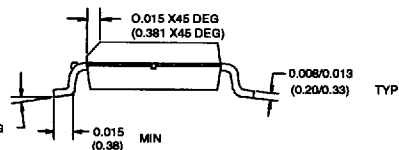
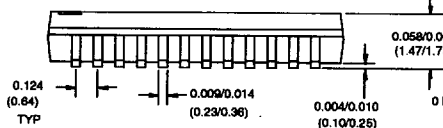
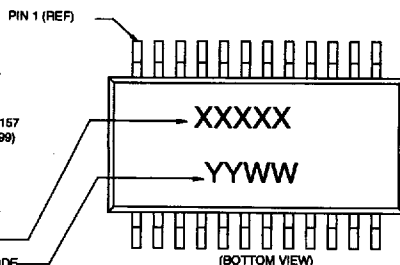
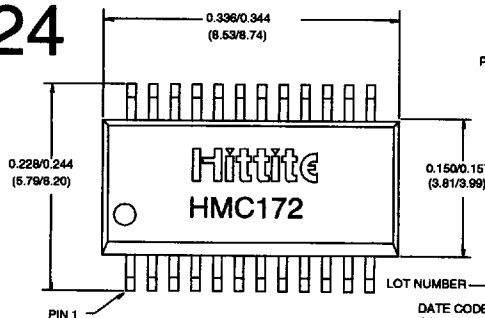
- A. PACKAGE BODY: LOW STRESS INJECTION-MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED.
- B. LEADFRAME MATERIAL: COPPER ALLOY

2. PLATING: LEAD-TIN SOLDER PLATE

- 3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED TOLERANCES ARE ± 0.005 (± 0.13)

- 4. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE QS16 PACKAGED PRODUCTS.

QS24



NOTES: FOR 24 LEAD QSOP PACKAGE

1. MATERIAL:

- A. PACKAGE BODY: LOW STRESS INJECTION-MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED.
- B. LEADFRAME MATERIAL: COPPER ALLOY

2. PLATING: LEAD-TIN SOLDER PLATE

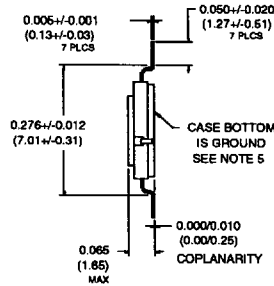
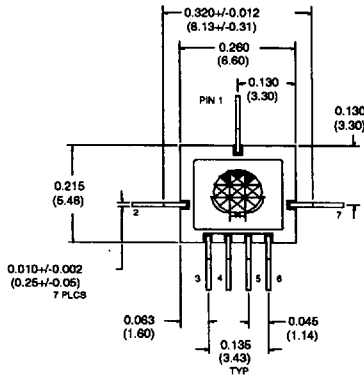
- 3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED TOLERANCES ARE ± 0.005 (± 0.13)

- 4. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE QS24 PACKAGED PRODUCTS.



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G7



NOTES: FOR 7 LEAD CERAMIC PACKAGE

1. MATERIAL:

1.1 G7 PACKAGE:

- A. PACKAGE BODY: WHITE ALUMINA (92%)
- B. LEADS, BASE, & COVER - ASTM F-15 ALLOY
- C. CONDUCTOR TRACES: TUNGSTEN

2. PLATING: ELECTROLYTIC GOLD 50 MICROINCHES MINIMUM, OVER ELECTROLYTIC NICKEL 50 MICROINCHES MINIMUM.

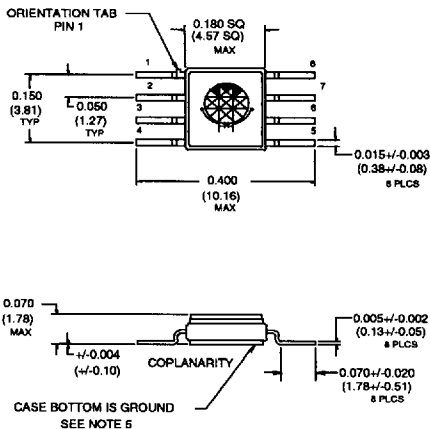
3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED TOLERANCES ARE +/- 0.005 (+/- 0.13)

4. G8 PACKAGE IS AVAILABLE WITH STRAIGHT LEADS, SPECIFY "P7".

5. THE PACKAGE BOTTOM, RF GROUND, MUST BE SOLDERED OR CONDUCTIVE EPOXIED TO THE PCB RF GROUND.

6. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE G7 PACKAGED PRODUCTS.

G8



NOTES: FOR 8 LEAD GLASS/METAL PACKAGE

1. MATERIAL:

1.1 G8 PACKAGE:

- A. PACKAGE BODY: ALUMINA LOADED BOROSILICATE GLASS (#7052 CORNING)
- B. LEADS, BASE, & COVER - ASTM F-16 ALLOY

2. PLATING: ELECTROLYTIC GOLD 50 MICROINCHES MINIMUM, OVER ELECTROLYTIC NICKEL 50 MICROINCHES MINIMUM.

3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED TOLERANCES ARE +/- 0.005 (+/- 0.13)

4. G8 PACKAGE IS AVAILABLE WITH STRAIGHT LEADS, SPECIFY "P8".

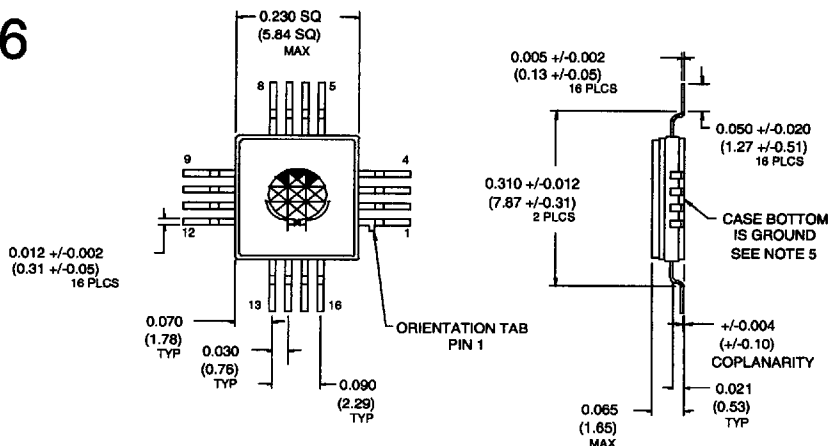
5. THE PACKAGE BOTTOM, RF GROUND, MUST BE SOLDERED OR CONDUCTIVE EPOXIED TO THE PCB RF GROUND.

6. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE G8 PACKAGED PRODUCTS.



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G16



NOTES: FOR 16 LEAD GLASS METAL PACKAGE

1. MATERIAL:

1.1 G16 PACKAGE:

A. PACKAGE BODY: ALUMINA LOADED BOROSILICATE GLASS

(#7052 CORNING)

B. LEADS, BASE, & COVER: ASTM F-15 ALLOY

2. PLATING: ELECTROLYTIC GOLD 50 MICROINCHES MINIMUM, OVER ELECTROLYTIC NICKEL 50 MICROINCHES MINIMUM.

3. DIMENSIONS ARE IN INCHES (MILLIMETERS), UNLESS OTHERWISE SPECIFIED TOLERANCES ARE ± 0.005 (± 0.13)

4. G8 PACKAGE IS AVAILABLE WITH STRAIGHT LEADS, SPECIFY "P16".

5. THE PACKAGE BOTTOM, RF GROUND, MUST BE SOLDERED OR CONDUCTIVE EPOXIED TO THE PCB RF GROUND.

6. CONSULT FACTORY FOR PIN DESIGNATION OF AVAILABLE G16 PACKAGED PRODUCTS.