# HN27C256AG Series — HITACHI/ LOGIC/ARRAYS/MEM

T-46-13-29

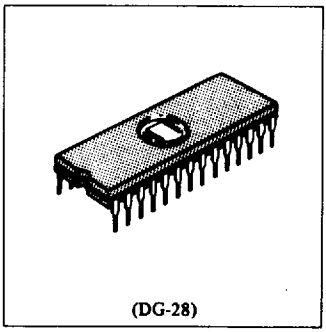
## 32768-Word x 8-Bit UV Erasable and Programmable ROM

This Hitachi HN27C256AG is a 256-kbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation.

Fabricated on advanced fine process and high speed circuitry technique, the HN27C256AG makes high speed access time possible for 16 bit microprocessors such as the 8086 and 68000. And low power dissipation in active and standby modes matches our CMOS 256-kbit EPROM.

In programming operation, the HN27C256AG realizes faster programming time than our conventional 256-kbit EPROM by Hitachi's Fast High-Reliability Programming Algorithm.

Pin arrangement, pin configuration and programming voltage are compatible with our 256-kbit EPROM series, therefore existing programmers can be used with the HN27C256AG.

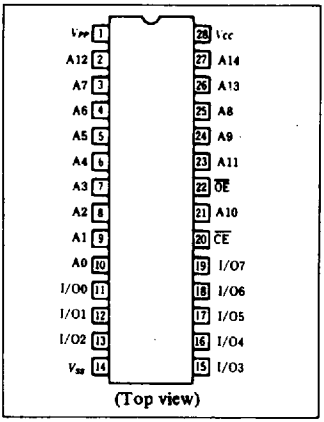


(DG-28)

### Features

- High speed
  - Access time . . . . . 100/120/150ns (max.)
- Low power dissipation
  - Active mode . . . . . 25 mW (typ.) (f = 1 MHz)
  - Standby mode . . . . . 5 μW (typ.)
- High reliability and fast programming
  - Programming voltage: +12.5V DC
  - Fast High-Reliability Programming Algorithm available
- Device identifier mode
  - Manufacturer code and device code

### Pin Arrangement




(Top view)

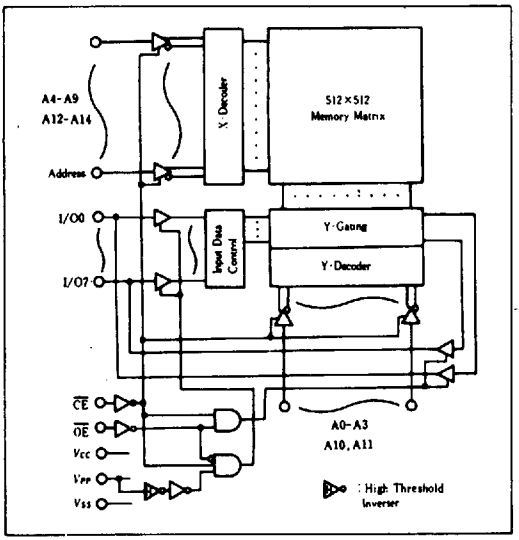
### Ordering Information

| Type No. | Access Time | Package |
|---|---|---|
| HN27C256AG-10 | 100 ns | 600-mil 28-pin cerdip |
| HN27C256AG-12 | 120 ns | |
| HN27C256AG-15 | 150 ns | |

### Pin Description

| Pin Name | Function |
|---|---|
| A0 – A14 | Address |
| I/O0–IO7 | Input/Output |
| $\overline{CE}$ | Chip enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply |
| $V_{PP}$ | Programming power supply |
| $V_{SS}$ | Ground |

### Block Diagram




### Mode Selection

| Mode | $\overline{CE}$ (20) | $\overline{OE}$ (22) | A9 (24) | $V_{PP}$ (1) | $V_{CC}$ (28) | I/O (11 – 13, 15 – 19) |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | x | $V_{CC}$ | $V_{CC}$ | Dout |
| Output disable | $V_{IL}$ | $V_{IH}$ | x | $V_{CC}$ | $V_{CC}$ | High Z |
| Standby | $V_{IH}$ | x | x | $V_{CC}$ | $V_{CC}$ | High Z |
| Program | $V_{IL}$ | $V_{IH}$ | x | $V_{PP}$ | $V_{CC}$ | Din |
| Program verify | $V_{IH}$ | $V_{IL}$ | x | $V_{PP}$ | $V_{CC}$ | Dout |
| Optional verify | $V_{IL}$ | $V_{IL}$ | x | $V_{PP}$ | $V_{CC}$ | Dout |
| Program inhibit | $V_{IH}$ | $V_{IH}$ | x | $V_{PP}$ | $V_{CC}$ | High Z |
| Identifier | $V_{IL}$ | $V_{IL}$ | $V_H$*2 | $V_{CC}$ | $V_{CC}$ | Code |

Notes: 1. x = Don't care.
2. $V_H$ = 12.0V ± 0.5V.

### Absolute Maximum Ratings

| Item | Symbol | Value | Unit |
|---|---|---|---|
| All input and output Voltages*1 | Vin, Vout | –0.6*2 to +7.0 | V |
| A9 input voltage*1 | $V_{ID}$ | –0.6*2 to +13.5 | V |
| $V_{PP}$ voltage*1 | $V_{PP}$ | –0.6 to +13.5 | V |
| $V_{CC}$ voltage*1 | $V_{CC}$ | –0.6 to +7.0 | V |
| Operating temperature range | Topr | 0 to +70 | °C |
| Storage temperature range | Tstg | –65 to +125 | °C |
| Storage temperature range under bias | Tbias | –10 to +80 | °C |

Notes: 1. Relative to $V_{SS}$.
2. Vin, Vout, $V_{ID}$ min = –1.0V for pulse width ≦ 50ns.

**Capacitance** ($Ta$ = 25°C, $f$ = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{in}$ | – | 4 | 8 | pF | $V_{in}$ = 0V |
| Output capacitance | $C_{out}$ | – | 8 | 12 | pF | Vout = 0V |

## Read Operation

**DC Characteristics** ($Ta$ = 0 to +70°C, $V_{CC}$ = 5V ±10%, $V_{PP}$ = $V_{CC}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | – | – | 2 | μA | $V_{in}$ = 0V to $V_{CC}$ |
| Output leakage current | $I_{LO}$ | – | – | 2 | μA | $V_{out}$ = 0V to $V_{CC}$ |
| $V_{PP}$ current | $I_{PP1}$ | – | 1 | 20 | μA | $V_{PP}$ = 5.5V |
| Standby $V_{CC}$ current | $I_{SB1}$ | – | – | 1 | mA | $\overline{CE}$ = VIH |
| | $I_{SB2}$ | – | 1 | 20 | μA | $\overline{CE}$ = $V_{CC}$ ± 0.3V |
| Operating $V_{CC}$ current | $I_{CC1}$ | – | – | 30 | mA | $\overline{CE}$ = $V_{IL}$, $I_{out}$ = 0 mA |
| | $I_{CC2}$ | – | – | 30 | mA | f = 10 MHz, $I_{out}$ = 0 mA |
| | $I_{CC3}$ | – | 5 | 15 | mA | f = 1 MHz, $I_{out}$ = 0 mA |
| Input low voltage*3 | $V_{IL}$ | –0.3*1 | – | 0.8 | V | |
| Input high voltage*3 | $V_{IH}$ | 2.2 | – | $V_{CC}$+1.0*2 | V | |
| Output low voltage | $V_{OL}$ | – | – | 0.45 | V | $I_{OL}$ = 2.1 mA |
| Output high voltage | $V_{OH1}$ | 2.4 | – | – | V | $I_{OH}$ = –1.0 mA |
| | $V_{OH2}$ | $V_{CC}$–0.7 | – | – | V | $I_{OH}$ = –100 μA |

Notes: *1. $V_{IL}$ min = –1.0V for pulse width ≦ 50ns.
*2. $V_{IH}$ max = $V_{CC}$ + 1.5V for pulse width ≦ 20ns.
If $V_{IH}$ is over the specified maximum value, read operation cannot be guaranteed.
*3. Only defined for DC function test. $V_{IL}$ max = 0.45V, $V_{IH}$ min = 2.4V for AC function test.

**AC Characteristics** ($Ta$ = 0 to 70°C, $V_{CC}$ = 5V ±10%, $V_{PP}$ = $V_{CC}$)

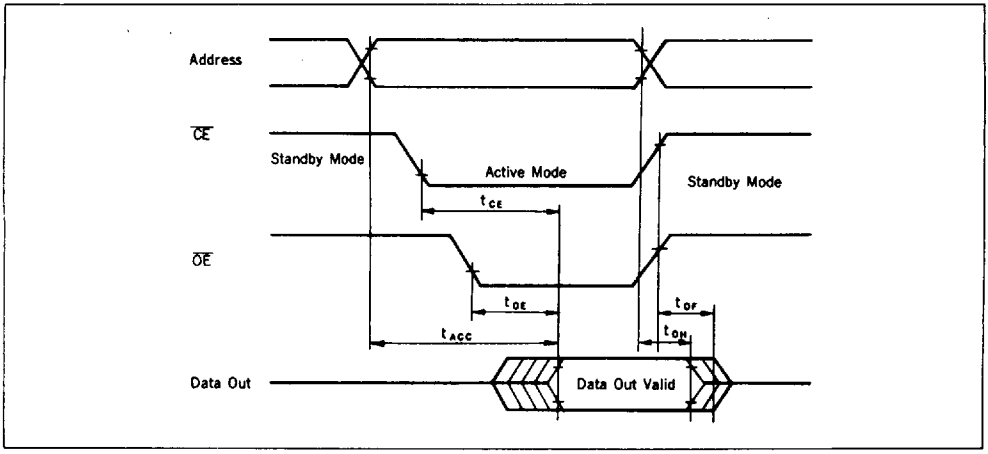
Test condition

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 10ns
- Output load: 1 TTL Gate + 100pF
- Reference lvels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

| Parameter | Symbol | HN27C256AG-10 | | HN27C256AG-12 | | HN27C256AG-15 | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Address to output delay | $t_{ACC}$ | – | 100 | – | 120 | – | 150 | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ |
| $\overline{CE}$ to output delay | $t_{CE}$ | – | 100 | – | 120 | – | 150 | ns | $\overline{OE}$ = $V_{IL}$ |
| $\overline{OE}$ to output delay | $t_{OE}$ | – | 60 | – | 60 | – | 70 | ns | $\overline{CE}$ = $V_{IL}$ |
| $\overline{OE}$ high to output float | $t_{DF}$ | 0 | 35 | 0 | 40 | 0 | 50 | ns | $\overline{CE}$ = $V_{IL}$ |
| Address to output hold | $t_{OH}$ | 5 | – | 5 | – | 5 | – | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ |

Note: $t_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

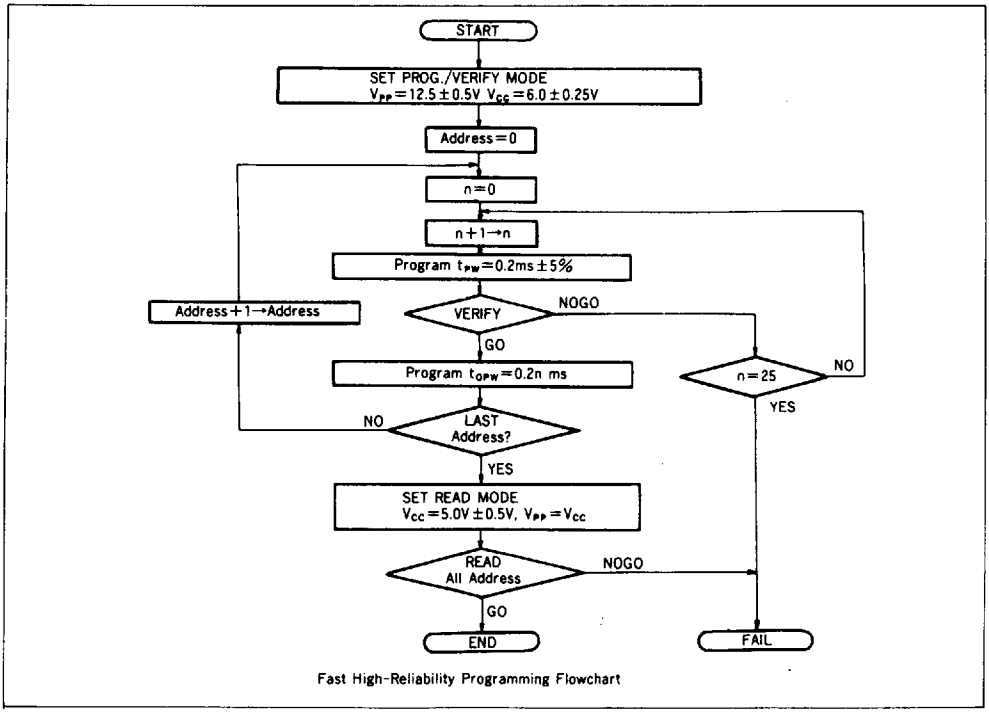
Read Timing Waveform




**Programming Operation**

**Fast High-Reliability Programming**

This device can be applied the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data retension. A theoretical programming time (except brank checking and verifying time) is one-tenth of conventional high performance programming algorithm's. Regarding the model and software version of the programmers available this algorithm, please contact programmer maker.




Fast High-Reliability Programming Flowchart

**DC Characteristics** ($Ta$ = 25°C ± 5°C, $V_{CC}$ = 6V ± 0.25V, $V_{PP}$ = 12.5V ± 0.5V)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | – | – | 2 | μA | $Vin$ = 0V to $V_{CC}$ |
| $V_{PP}$ supply current | $I_{PP}$ | – | – | 30 | mA | $\overline{CE}$ = $V_{IL}$ |
| Operating $V_{CC}$ current | $I_{CC}$ | – | – | 30 | mA | |
| Input low level | $V_{IL}$ | −0.1*5 | – | 0.8 | V | |
| Input high level | $V_{IH}$ | 2.2 | – | $V_{CC}$+0.5*6 | V | |
| Output low voltage during verity | $V_{OL}$ | – | – | 0.45 | V | $I_{OL}$ = 2.1 mA |
| Output high voltage during verify | $V_{OH}$ | 2.4 | – | – | V | $I_{OH}$ = −400 μA |

Notes: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ must not exceed 13.5V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}$ = 12.5V.
4. Do not alter $V_{PP}$ either $V_{IL}$ to 12.5V or 12.5V or 12.5V to $V_{IL}$ when CE = Low.
5. $V_{IL}$ min = −0.6V for pulse width ≦ 20ns.
6. If $V_{IH}$ is over the specified maximum value, programming operation cannot be guaranteed.

**AC Characteristics** ($Ta$ = 25°C ± 5°C, $V_{CC}$ = 6V ± 0.25V, $V_{PP}$ = 12.5V ± 0.5V)

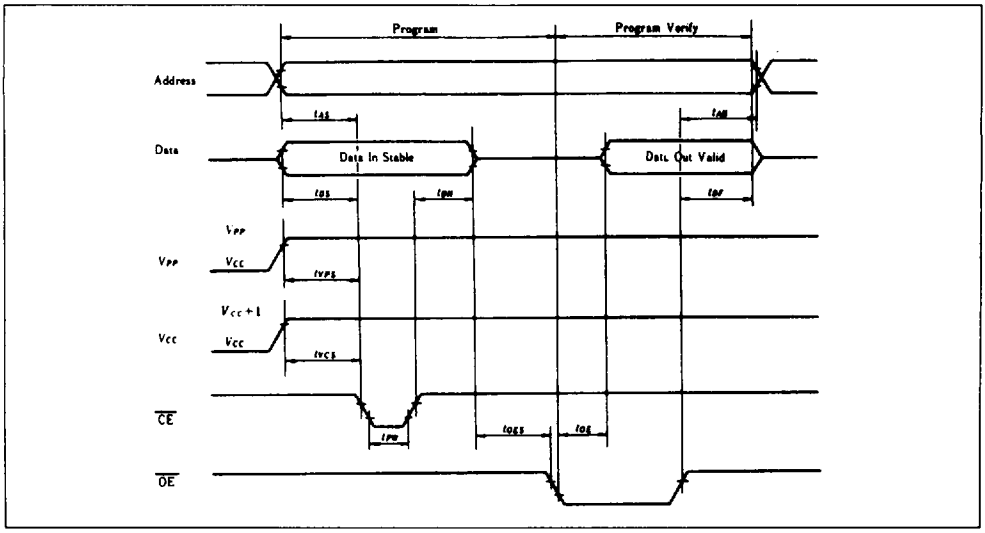
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | 2 | – | – | μs |
| $\overline{OE}$ setup time | $t_{OES}$ | 2 | – | – | μs |
| Data setup time | $t_{DS}$ | 2 | – | – | μs |
| Address hold time | $t_{AH}$ | 0 | – | – | μs |
| Data hold time | $t_{DH}$ | 2 | – | – | μs |
| $V_{PP}$ setup time | $t_{VPS}$ | 2 | – | – | μs |
| $V_{CC}$ setup time | $t_{VCS}$ | 2 | – | – | μs |
| $\overline{CE}$ initial programming pulth width | $t_{PW}$ | 0.19 | 0.20 | 0.21 | ms |
| $\overline{CE}$ overprogramming pulse width | $t_{OPW}$*1 | 0.19 | – | 5.25 | ms |
| Data valid from $\overline{OE}$ | $t_{OE}$ | 0 | – | 150 | ns |
| $\overline{OE}$ to output float delay | $t_{DF}$*2 | – | – | 130 | ns |

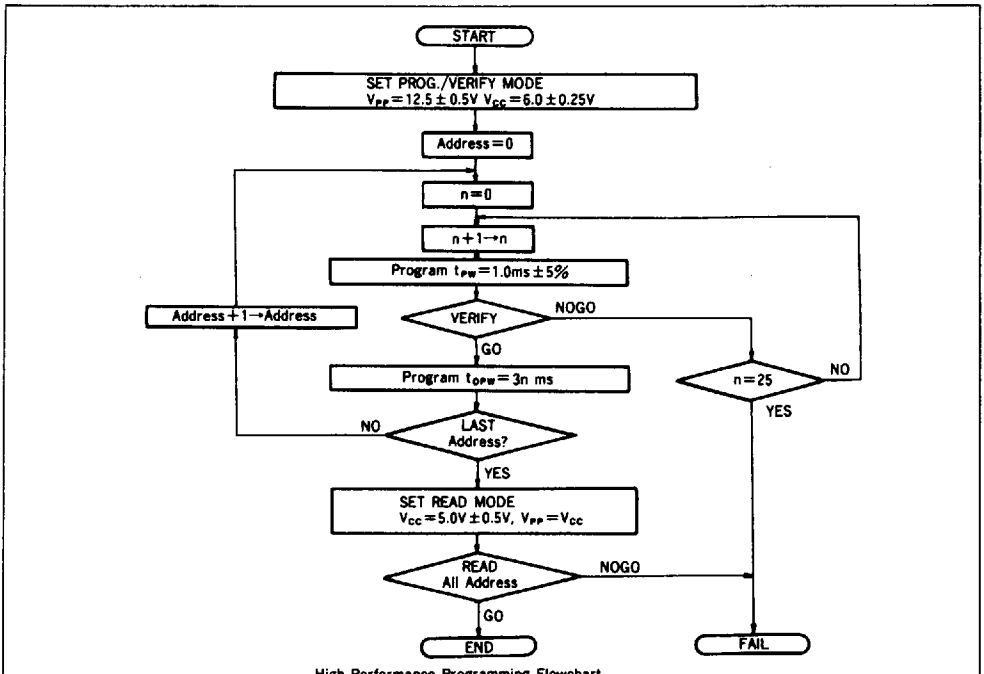
Notes: 1. Refer to the Fast High-Reliability Programming Fowchart for $t_{OPW}$.
2. $t_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform




**High Performance Programming**

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-kbit EPROM series so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.




High Performance Programming Flowchart

**DC Characteristics** ($Ta$ = 25°C ± 5°C, $V_{CC}$ = 6V ± 0.25V, $V_{PP}$ = 12.5V ± 0.5V)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | – | – | 2 | μA | $Vin$ = 0V to $V_{CC}$ |
| $V_{PP}$ supply current | $I_{PP}$ | – | – | 30 | mA | $\overline{CE}$ = $V_{IL}$ |
| Operating $V_{CC}$ current | $I_{CC}$ | – | – | 30 | mA | |
| Input low level | $V_{IL}$ | −0.1*5 | – | 0.8 | V | |
| Input high level | $V_{IH}$ | 2.2 | – | $V_{CC}$+0.5*6 | V | |
| Output low voltage during verify | $V_{OL}$ | – | – | 0.45 | V | $I_{OL}$ = 2.1 mA |
| Output high voltage during verify | $V_{OH}$ | 2.4 | – | – | V | $I_{OH}$ = −400 μA |

Notes:
1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ must not exceed 13.5V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}$ = 12.5V.
4. Do not alter $V_{PP}$ either $V_{IL}$ to 12.5V or 12.5V to $V_{IL}$ when $\overline{CE}$ = Low.
5. $V_{IL}$ min = −0.6V for pulse width ≦ 20ns.
6. If $V_{IH}$ is over the specified maximum value, programming operation. cannot be guaranteed.

**AC Characteristics** ($Ta$ = 25°C ± 5°C, $V_{CC}$ = 6V ± 0.25V, $V_{PP}$ = 12.5V ± 0.5V)

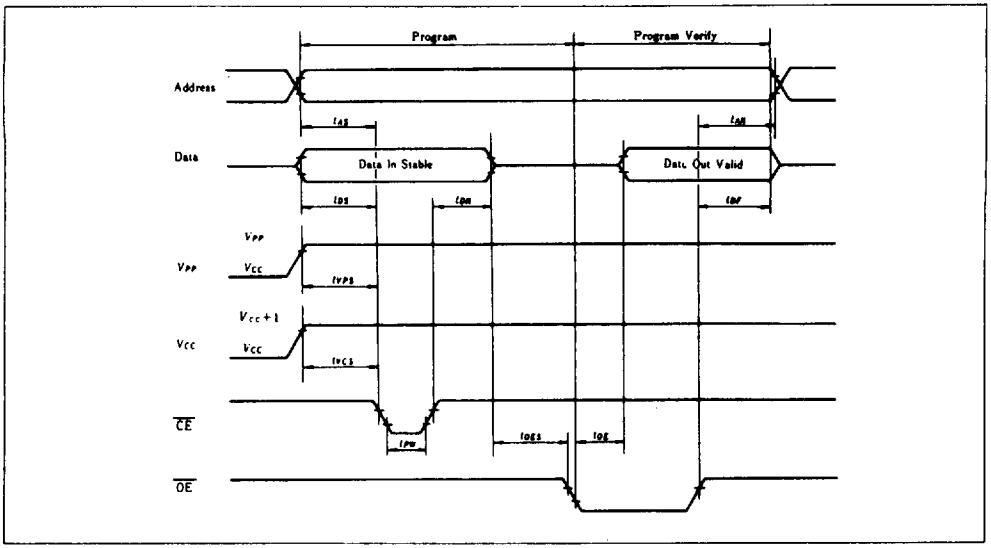
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | 2 | – | – | μs |
| $\overline{OE}$ setup time | $t_{OES}$ | 2 | – | – | μs |
| Data setup time | $t_{DS}$ | 2 | – | – | μs |
| Address hold time | $t_{AH}$ | 0 | – | – | μs |
| Data hold time | $t_{DH}$ | 2 | – | – | μs |
| $V_{PP}$ setup time | $t_{VPS}$ | 2 | – | – | μs |
| $V_{CC}$ setup time | $t_{VCS}$ | 2 | – | – | μs |
| $\overline{CE}$ initial programming pulth width | $t_{PW}$ | 0.95 | 1.0 | 1.05 | ms |
| $\overline{CE}$ overprogramming pulse width | $t_{OPW}$*1 | 2.85 | – | 78.75 | ms |
| Data valid from $\overline{OE}$ | $t_{OE}$ | 0 | – | 150 | ns |
| $\overline{OE}$ to output float delay | $t_{DF}$*2 | – | – | 130 | ns |

Notes:
1. Refer to the high performance programming flowchart for $t_{OPW}$.
2. $t_{DF}$ is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform




**Erase**

Erasure of HN27C256AG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W·sec/cm$^2$.

**Mode Description**

**Device Identifier Mode**

Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

**HN27C256AG Series Identifier Code**

| Identifier | A0 (10) | I/O7 (19) | I/O6 (18) | I/O5 (17) | I/O4 (16) | I/O3 (15) | I/O2 (13) | I/O1 (12) | I/O0 (11) | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer code | $V_{IL}$ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |
| Device code | $V_{IH}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31 |

Notes: 1. A9 = 12.0V ± 0.5V.
2. A1 – A8, A10 – A14, $\overline{CE}$, $\overline{OE}$ = $V_{IL}$.