

1M (128K x 8-bit) OTP EPROM

■ DESCRIPTION

The Hitachi HN27V101A is a 1-Megabit One-Time Programmable Electrically Programmable Read Only Memory organized as 131,072 x 8-bits.

The HN27V101A features a low power supply voltage and low power dissipation. This combination makes the HN27V101A suitable for low power microcomputer systems. The HN27V101A offers high speed programming using page programming mode.

Hitachi's HN27V101A is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-lead Plastic SOP and TSOP packages. The HN27V101A TSOP package is offered in both standard and reverse bend pinouts.

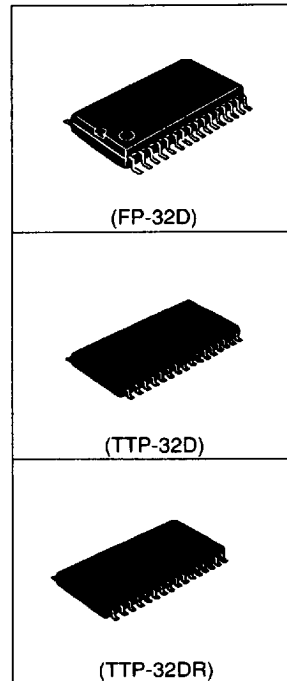
The Plastic SOP and TSOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.

■ FEATURES

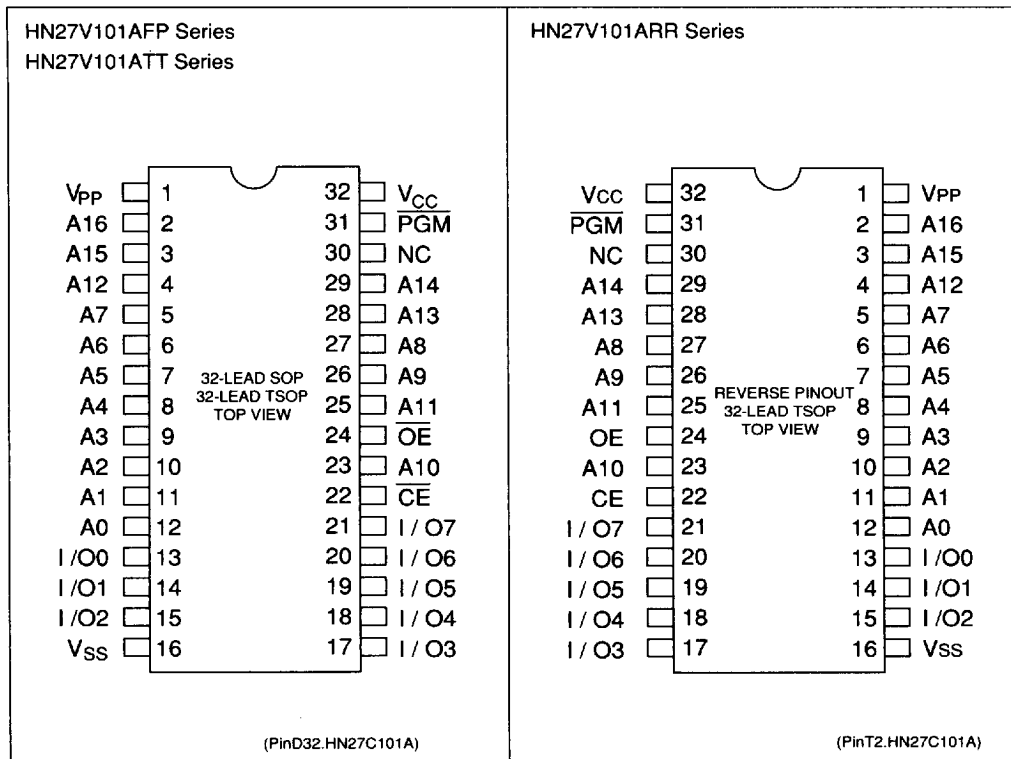
- Address Access Time:
250 ns (max)
- Single Power Supply:
 $V_{CC} = 2.7$ to $5.5V$
- Low Power Dissipation:
Active Mode: 50 mW/MHz (typ)
Standby Mode: 5 μW (typ)
- High Speed Page and Word Programming:
Page Programming Time: 14 sec (typ)
- Programming Power Supply:
 $V_{PP} = 12.5V \pm 0.3V$
- Pin Arrangement:
JEDEC Standard Byte-Wide EPROM
- Packages:
32-lead Plastic SOP
32-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27V101AFP-25	250 ns	32-lead Plastic SOP (FP-32D)
HN27V101ATT-25	250 ns	32-lead Plastic TSOP (TTP-32D)
HN27V101ARR-25	250ns	32-lead Plastic TSOP (TTP-32DR) Reverse bend



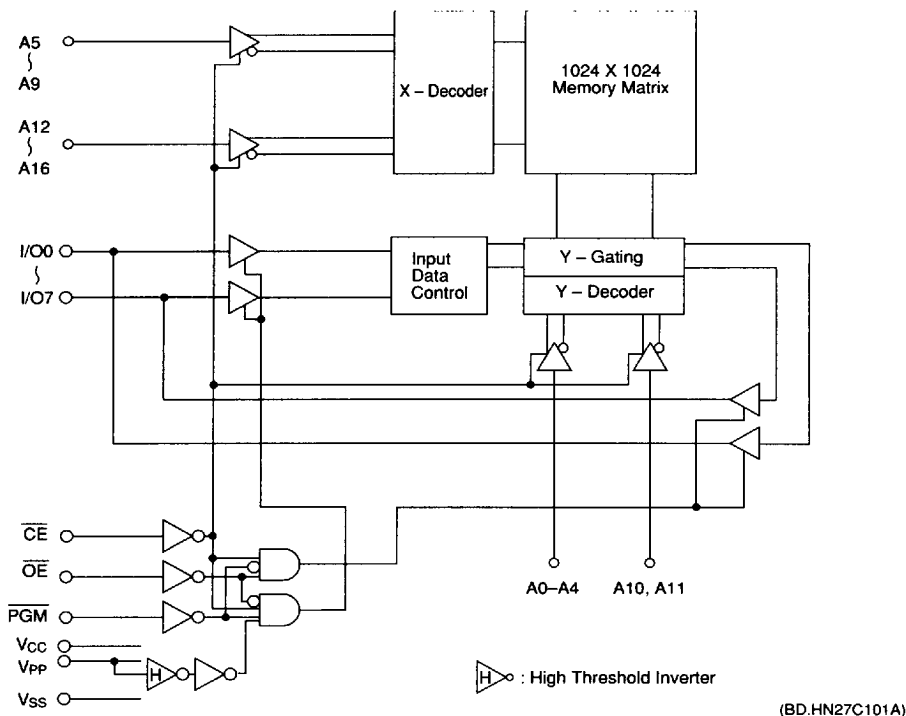
■ PIN ARRANGEMENT



■ PIN DESCRIPTION

Pin Name	Function
A ₀ - A ₁₆	Address
I/O ₀ - I/O ₇	Input/Output
CE	Chip Enable
OE	Output Enable
V _{CC}	Power Supply
V _{PP}	Programming Supply
V _{SS}	Ground
PGM	Programming Enable
NC	No Connection

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X ¹	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Page Data Latch	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IH}	X	D_{IN}
Page Program	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IL}	X	High-Z
Program Inhibit	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H	ID

- Notes: 1. X = Don't Care. $V_{PP} = 0\text{ V to }V_{CC}$.
 2. $11.5\text{ V} \leq V_H \leq 12.5\text{ V}$

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage ¹	V_{CC}	-0.6 to +7.0	V
Programming Voltage ¹	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage ^{1,2}	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_0 and $\overline{OE}$ Voltage ²	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

- Notes: 1. Relative to V_{SS} .
 2. V_{IN} , V_{OUT} , and V_{ID} min = -1.0V for pulse width $\leq$ 20 ns.

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	10	pF	$V_{IN} = 0\text{V}$
Output Capacitance	C_{OUT}	-	15	pF	$V_{OUT} = 0\text{V}$

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC} = 2.7$ to 5.5V , $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	μA	$V_{IN} = 5.5\text{V}$
Output Leakage Current	I_{LO}	-	-	2	μA	$V_{OUT} = 5.5\text{V}/0.45\text{V}$
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	$I_{OUT} = 0\text{mA}$, $\overline{CE} = V_{IL}$
	I_{CC2}	-	-	30	mA	$I_{OUT} = 0\text{mA}$, $f = 4\text{MHz}$
Standby V_{CC} Current	I_{SB}	-	-	1	mA	$CE = V_{IH}$
	I_{SB2}	-	1	20	mA	$\overline{CE} = V_{CC} \pm 0.3\text{V}$
V_{PP} Current	I_{PP1}	-	1	20	μA	$V_{PP} = 5.5\text{V}$
Input Voltage	V_{IH}	2.2	-	$V_{CC} + 1^2$	V	
	V_{IL}	-0.3 ¹	-	0.6/0.8	V	$V_{CC} = 2.7$ to 4.5V / $V_{CC} = 4.5$ to 5.5V
Output Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -400\mu\text{A}$
	V_{OH}	$V_{CC}-0.2$	-	-	V	$I_{OH} = -20\mu\text{A}$
	V_{OL}	-	-	0.45	V	$I_{OL} = 1.0\text{mA}$
	V_{OL}	-	-	0.2	V	$I_{OL} = 2.0\mu\text{A}$

- Notes: 1. V_{IL} min = -1.0 V for pulse width $\leq$ 50 ns.
 2. V_{IH} max = $V_{CC} + 1.5\text{V}$ for pulse width $\leq$ 20 ns.
 If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC} = 2.7$ to $5.5V$, $V_{PP} = V_{CC}$, $T_a = 0$ to $70^{\circ}C$)

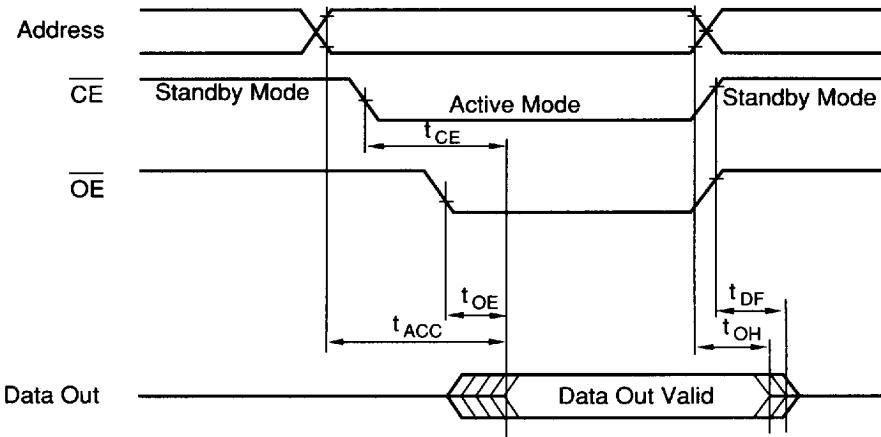
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27V101A-25		Unit	Test Condition
		Min.	Max.		
Address Access Time	t_{ACC}	-	250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
Chip Enable Access Time	t_{CE}	-	250	ns	$\overline{OE} = V_{IL}$
Output Enable Access Time	t_{OE}	-	120	ns	$\overline{CE} = V_{IL}$
Output Disable to High-Z ¹	t_{DF}	0	120	ns	$\overline{CE} = V_{IL}$
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C101A)

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■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

($V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	μA	$V_{IN} = 0 \text{ V to } V_{CC}$
Operating V_{CC} Current	I_{CC}	-	-	30	mA	
Operating V_{PP} Current	I_{PP}	-	-	40	mA	$\overline{CE} = \text{PGM} = V_{IL}$
Input Voltage ³	V_{IH}	2.2	-	$V_{CC} + 5$ ⁶	V	
	V_{IL}	- 0.1 ⁵	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -400 \mu\text{A}$
	V_{OL}	-	-	0.45	V	$I_{OH} = 2.1 \text{ mA}$

- Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width $\leq 20 \text{ ns}$.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

($V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: $\leq 20 \text{ ns}$
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	μs	
Address Hold Time	t_{AH}	0	-	-	μs	
Data Setup Time	t_{DS}	2	-	-	μs	
Data Hold Time	t_{DH}	2	-	-	μs	
Chip Enable Setup Time	t_{CES}	2	-	-	μs	
V_{PP} Setup Time	t_{VPS}	2	-	-	μs	
V_{CC} Setup Time	t_{VCS}	2	-	-	μs	
Output Enable Setup Time	t_{OES}	2	-	-	μs	
Output Disable Time	t_{DF}	0	-	130	ns	
PGM Initial Programming Pulse Width	t_{PW}	0.19	0.20	0.21	ms	
PGM Overprogramming Pulse Width	t_{OPW}	0.19	-	5.25	ms	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Output Enable Pulse During Data Latch	t_{LW}	1	-	-	μs	
Output Enable Hold Time	t_{OEH}	2	-	-	μs	
Chip Enable Hold Time	t_{CEH}	2	-	-	μs	
PGM Setup Time	t_{PGMS}	2	-	-	μs	

- Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

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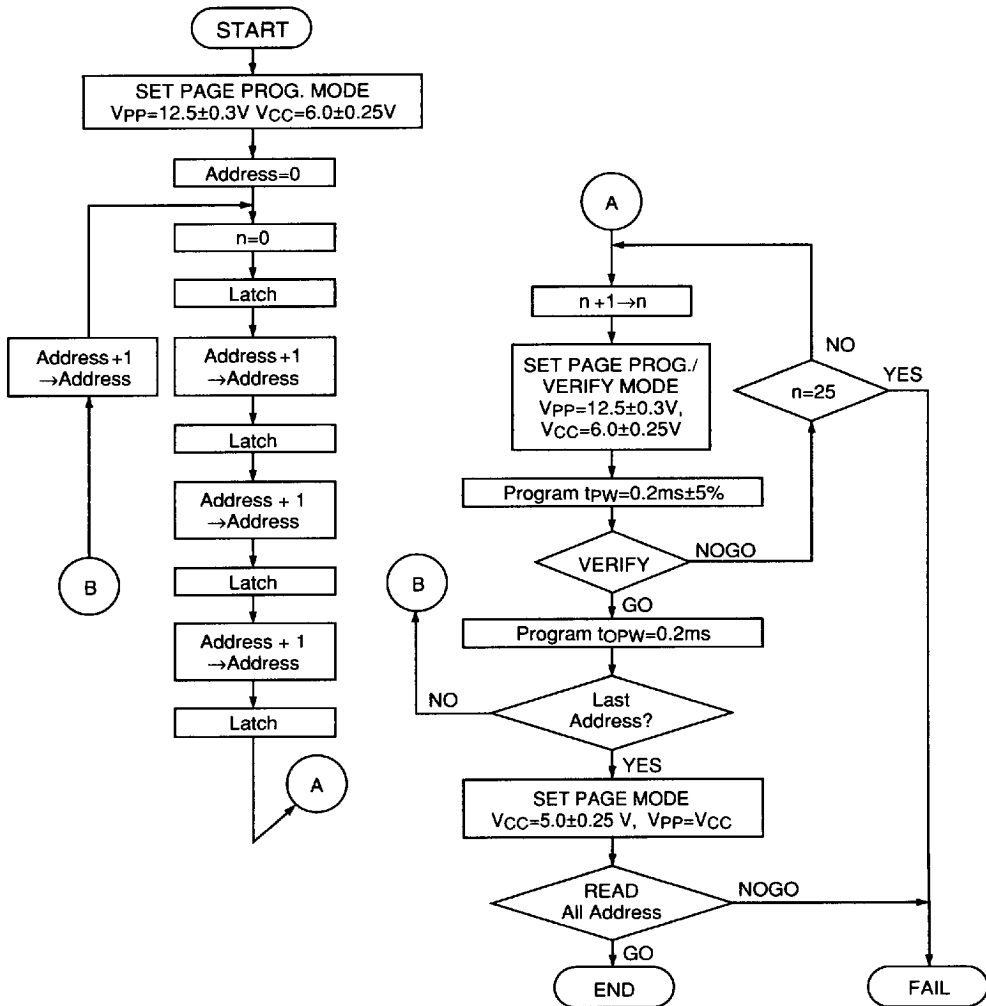
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■ PAGE PROGRAMMING FLOWCHART

The Hitachi HN27V101A can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

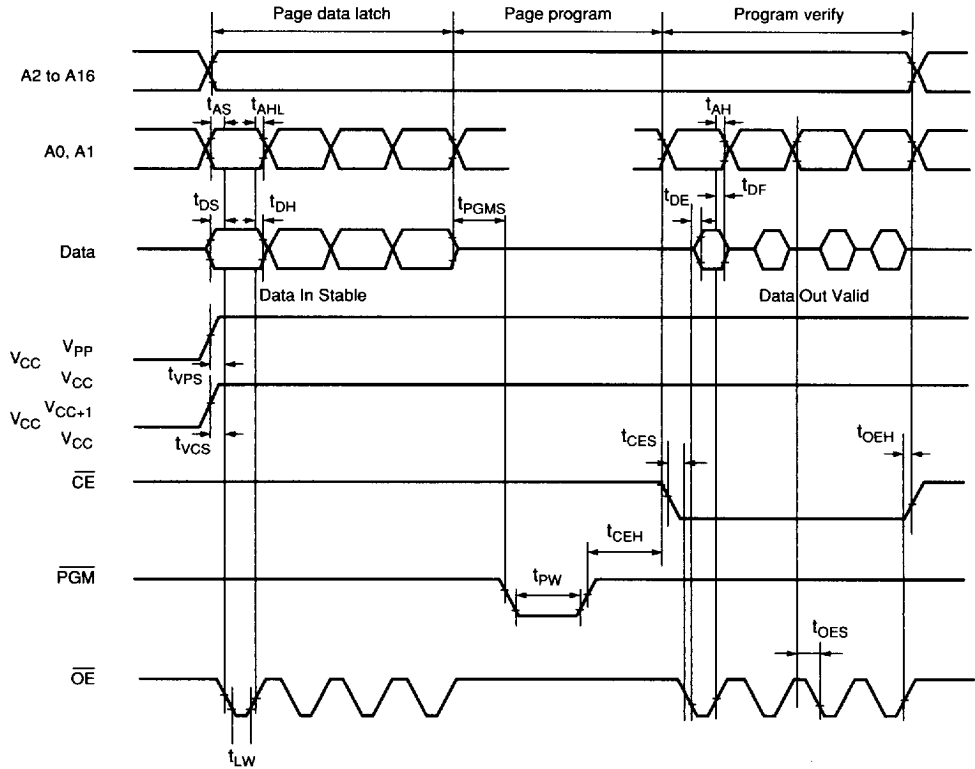


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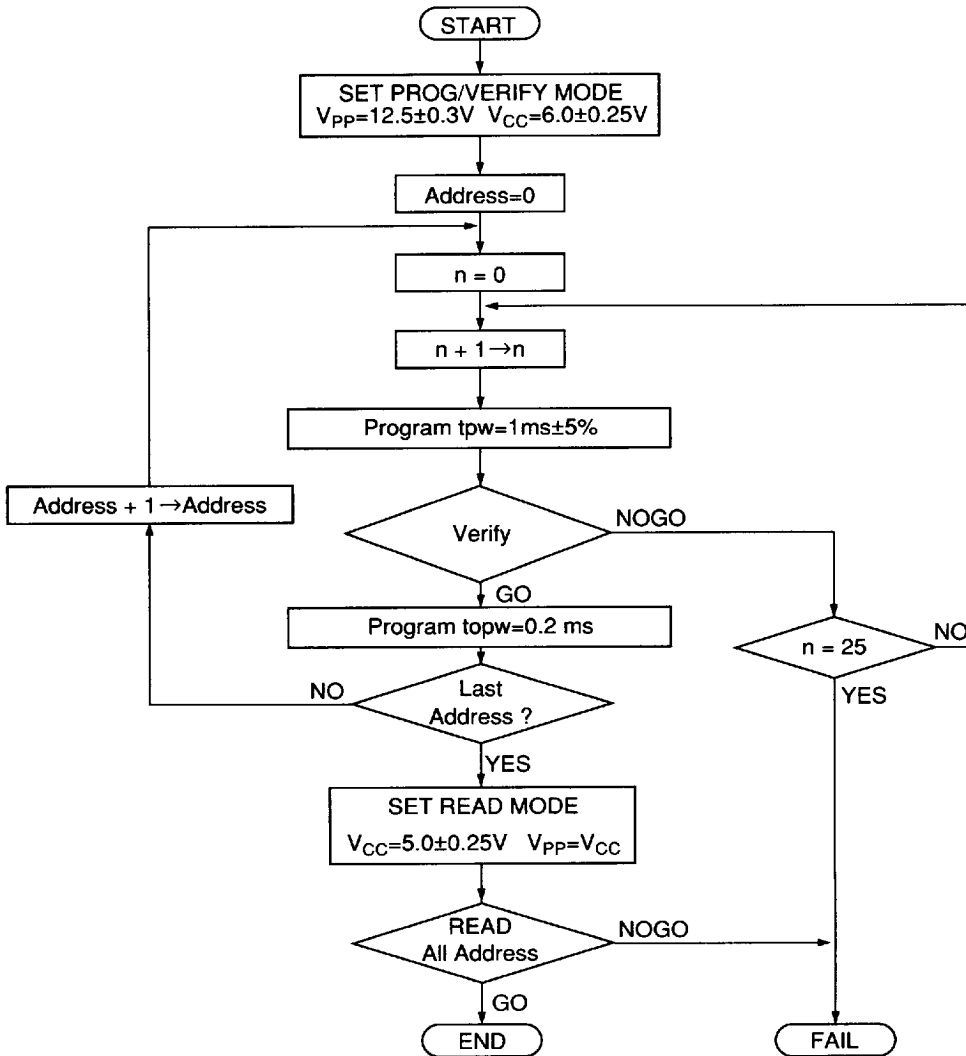
■ PAGE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27C101A)

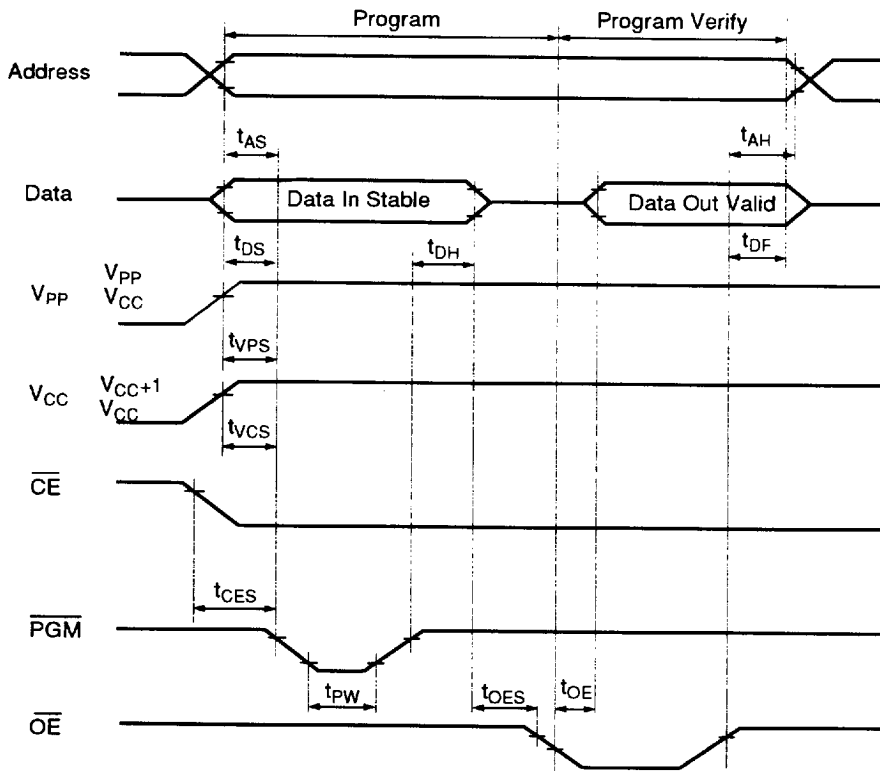
■ BYTE PROGRAMMING FLOWCHART

The Hitachi HN27V101A can be programmed with the high performance Byte Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C101A)

■ BYTE PROGRAMMING TIMING WAVEFORM



(TD P.HN27C101A)

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

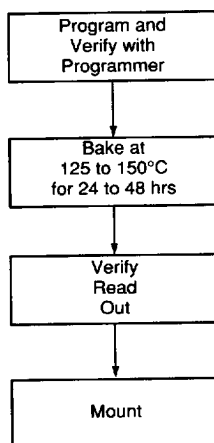
■ HN27C101A SERIES IDENTIFIER CODE

Identifier	A ₀	I/O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	I/O ₀	Hex Data
Manufacturer Code	V _{IL}	0	0	0	0	0	1	1	1	07
Device Code	V _{IH}	0	0	1	1	1	0	0	0	38

- Notes:
1. V_H = 12.0 V ± 0.5V
 2. A₁-A₈, A₁₀-A₁₆, CE, OE = V_{IL}, PGM = V_{IH}
 4. X = Don't Care

■ HN27V101A RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27V101A plastic packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)