

HN58064 Series

8192-word x 8-bit Electrically Erasable and Programmable ROM.

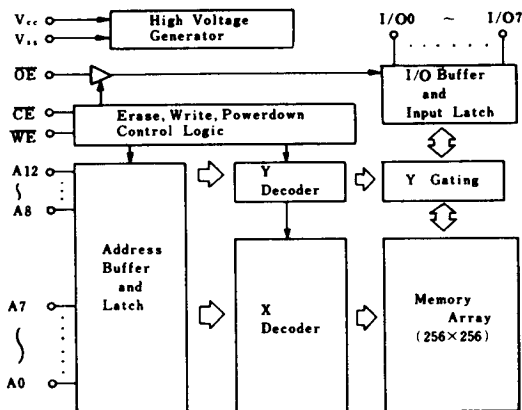
■ FEATURES

- Single 5V Supply
- Address, Data, $\overline{CE}$, $\overline{OE}$ Latches
- Byte Erase / Byte Write Time. 10 ms typ.
- Chip Erase Time 20 ms typ.
- Fast Access Time. 250/300ns max.
- Low Power Dissipation. 300mW typ. (Active)
125mW typ. (Standby)
- Comforms to JEDEC Byte-Wide Standard
- Reliable N-channel MNOS Technology
- 10000 Erase/Write Cycles

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58064P-25	250ns	600 mil 28 pin Plastic DIP
HN58064P-30	300ns	

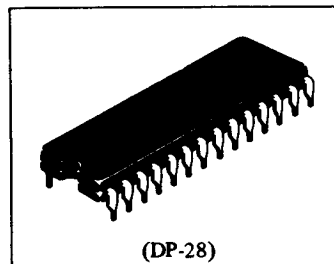
■ BLOCK DIAGRAM



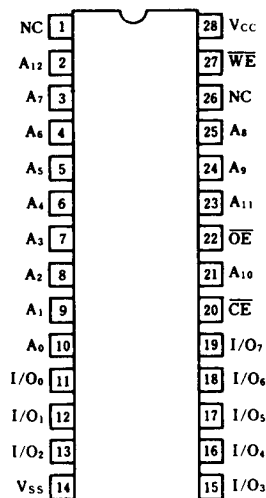
■ MODE SELECTION

	PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11~13, 15~19)
MODE					
Read		V_{IL}	V_{IL}	V_{IH}	Dout
Standby		V_{IH}	X	X	High Z
Byte Erase		V_{IL}	V_{IH}	V_{IL}	Din = V_{IH}
Byte Write		V_{IL}	V_{IH}	V_{IL}	Din
Chip Erase		V_{IL}	V_{IL}	V_{IL}	Din = V_{IH}
Deselect		V_{IL}	V_{IH}	V_{IH}	High Z

X: V_{IH} or V_{IL}



■ PIN ARRANGEMENT



(Top View)

A0 – A12	Address Input
I/O0 – I/O7	Data in / Data out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
Vcc	Power (+5V)
Vss	GND
NC	No Connect



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	-0.6 to +7.0	V
Input Voltage*1	V_{in}	-0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

Note: *1. With Respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	-0.1	-	0.8	V
	V_{IH}	2.0	-	$V_{CC} + 1$	V
Operating Temperature	T_{opr}	0	-	70	°C

■ DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC} = 5.5\text{V}$, $V_{in} = 5.5\text{V}$	-	-	10	μA
Output Leakage Current	I_{LO}	$V_{CC} = 5.5\text{V}$, $V_{out} = 5.5/0.4\text{V}$	-	-	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE} = V_{IH}$	-	25	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE} = V_{IL}$	-	60	100	mA
Input Low Voltage	V_{IL}		-0.1	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC} + 1$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{ mA}$	-	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.4	-	-	V

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	-	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	-	-	12	pF

■ AC TEST CONDITIONS

Input Pulse Levels: 0.4V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Output Load: 1TTL Gate + 100pF
 Reference Level for Measuring Timing: 0.8V and 2.0V



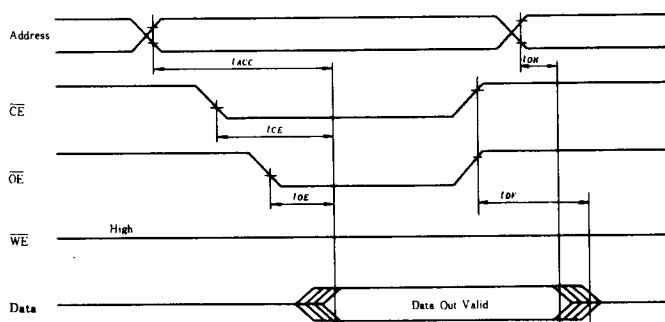
■ AC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

● READ OPERATION

Parameter	Symbol	Test Condition	HN58064-25		HN58064-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	—	250	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	—	250	—	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	—	100	—	150	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	0	—	0	—	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	0	90	0	130	ns

Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

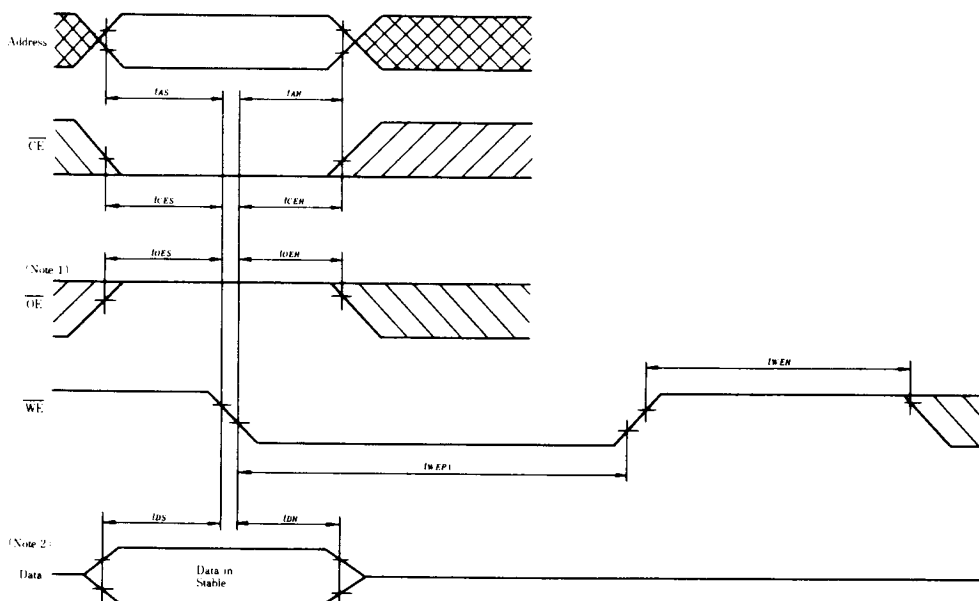
● WAVE FORM READ CYCLE



● BYTE ERASE AND BYTE WRITE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		0	—	—	ns
Address Hold Time	t_{AH}		100	—	—	ns
CE Setup Time	t_{CES}		0	—	—	ns
CE Hold Time	t_{CEH}		100	—	—	ns
OE Setup Time	t_{OES}		0	—	—	ns
OE Hold Time	t_{OEH}		100	—	—	ns
WE Pulse Width	t_{WEP1}		8	10	15	ms
WE High Time	t_{WEH}		1000	—	—	ns
Data Setup Time	t_{DS}		0	—	—	ns
Data Hold Time	t_{DH}		100	—	—	ns

● WAVE FORM ERASE AND WRITE CYCLE



- Notes: 1. $\overline{CE}$ or $\overline{OE}$ should be "1" and in Standby Mode or Deselect Mode before Write/Erase operation.
 2. I/O0 to I/O7 must be "1" in Byte Erase.

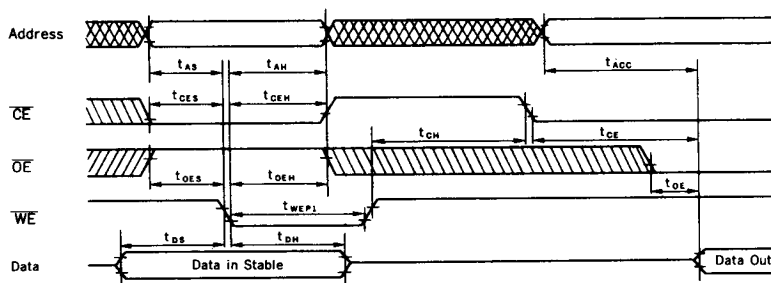


● Read Cycle after Byte Erase or Byte Write

Parameter	Symbol	HN58064-25			HN58064-30			Unit
		min*1	typ	max	min*1	typ	max	
Address setup time	t_{AS}	0	—	—	0	—	—	ns
Address hold time	t_{AH}	100	—	—	100	—	—	ns
$\overline{CE}$ setup time	t_{CES}	0	—	—	0	—	—	ns
$\overline{CE}$ hold time	t_{CEH}	100	—	—	100	—	—	ns
$\overline{OE}$ setup time	t_{DES}	0	—	—	0	—	—	ns
$\overline{OE}$ hold time	t_{DEH}	100	—	—	100	—	—	ns
$\overline{WE}$ pulse width	t_{WEPI}	10	12	15	10	12	15	ms
$\overline{CE}$ high time	t_{CH}	10	—	—	10	—	—	μ s
Data setup time	t_{DS}	0	—	—	0	—	—	ns
Data hold time	t_{DH}	100	—	—	100	—	—	ns
Address to output delay time	t_{ACC}	250	—	—	300	—	—	ns
$\overline{CE}$ to output delay time	t_{CE}	250	—	—	300	—	—	ns
$\overline{OE}$ to output delay time	t_{OE}	100	—	—	150	—	—	ns

Note: 1. Use this device in longer cycle than this value.

● Read Timing Waveform after Byte Erase or Byte Write



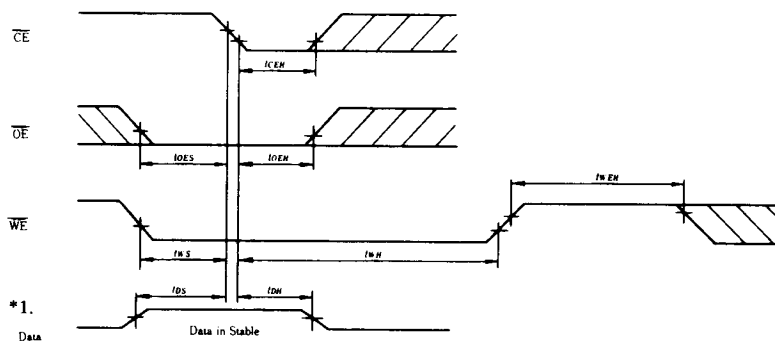
- Notes: 1. $\overline{CE}$ or $\overline{OE}$ should be high and in standby mode or deselect mode before write/erase operation.
 2. I/O0 to I/O7 must be "1" in byte erase.



● CHIP ERASE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
CE Hold Time	t_{CEH}		100	—	—	ns
OE Setup Time	t_{OES}		0	—	—	ns
OE Hold Time	t_{OEH}		100	—	—	ns
WE Setup Time	t_{WS}		0	—	—	ns
WE Pulse Width	t_{WH}		15	20	25	ms
WE High Time	t_{WEH}		1000	—	—	ns
Data Setup Time	t_{DS}		0	—	—	ns
Data Hold Time	t_{DH}		100	—	—	ns

● WAVE FORM CHIP ERASE



- Notes: 1. 1/00 ~ 7 must be "1" in Chip Erase Operation.
 2. Don't Care about Address.

