

# HN61256P, HN61256FP

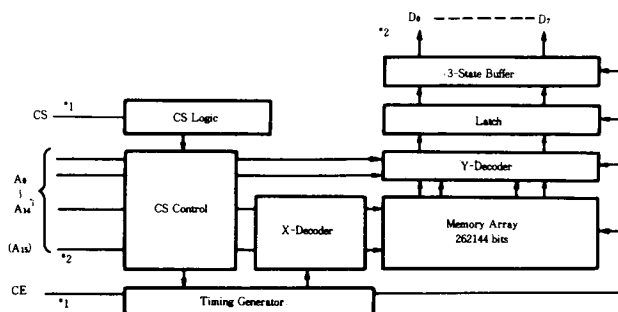
## 32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

### ■ FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply ( $\pm 10\%$ )
- Low power consumption: Operation 7.5mW (typ.), Standby 5 $\mu$ W (typ.)
- TTL compatible
- Access time: 3.5 $\mu$ s (max)

### ■ BLOCK DIAGRAM

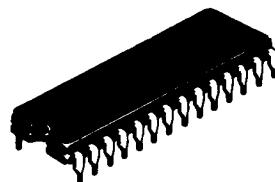


\*1 Active level defined at mask level.

\*2 Mask programmable selection of either 4-bit or 8-bit organization.

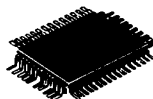
In 4-bit organization, data outputs are D<sub>0</sub> to D<sub>3</sub>.

HN61256P



(DP-28)

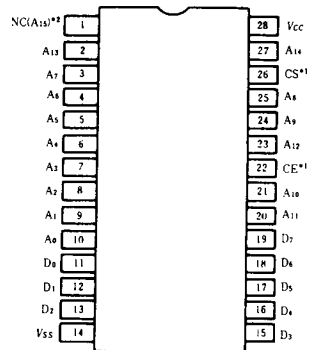
HN61256FP



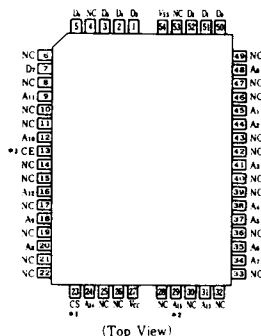
(FP-54)

### ■ PIN ARRANGEMENT

#### ● HN61256P



#### ● HN61256FP



\*1. Active level defined by user.

\*2. Upper address of 4-bit organization.



# **■ ABSOLUTE MAXIMUM RATINGS**

| Item                           | Symbol    | Rating             | Unit |
|--------------------------------|-----------|--------------------|------|
| Supply Voltage*                | $V_{CC}$  | $-0.3 \sim +7.0$   | V    |
| All Input and output Voltage*  | $V_I$     | $-0.3 \sim V_{CC}$ | V    |
| Operating Temperature          | $T_{op}$  | $0 \sim +75$       | °C   |
| Storage Temperature Range      | $T_{stg}$ | $-55 \sim +125$    | °C   |
| Bias Storage Temperature Range | $T_{bss}$ | $-20 \sim +85$     | °C   |

Note: \* Referenced to  $V_{SS}$ .

# **■ ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0 \sim +75^\circ C$ )

| Item                                | Symbol                                                | Test Conditions                                                                                            | min | typ** | max      | Unit          |
|-------------------------------------|-------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----|-------|----------|---------------|
| Input "High" Level Voltage          | $V_{IH}$                                              |                                                                                                            | 2.4 | —     | $V_{CC}$ | V             |
| Input "Low" Level Voltage           | $V_{IL}$                                              |                                                                                                            | 0   | —     | 0.8      | V             |
| Output "High" Level Voltage         | $V_{OH}$                                              | $I_{OH} = -100 \mu A$                                                                                      | 2.4 | —     | —        | V             |
| Output "Low" Level Voltage          | $V_{OL}$                                              | $I_{OL} = 1.6 mA$                                                                                          | —   | —     | 0.4      | V             |
| Input Leakage Current               | $I_{LI}$                                              | $V_{II} = 0 \sim 5.5 V$                                                                                    | —   | —     | 2.5      | $\mu A$       |
| Output "High" Level Leakage Current | $I_{LOH}$                                             | $CE = 0.8 V$                                                                                               | —   | —     | 5        | $\mu A$       |
| Output "Low" Level Leakage Current  | $I_{LOL}$                                             | $CE = 2.4 V$                                                                                               | —   | —     | 5        | $\mu A$       |
| Supply Current                      | In stand-by<br>$I_{SB}$<br>In operation<br>$I_{CC}^*$ | $CS \leq V_{CC} - 0.2 V$<br>$CS \leq 0.2 V$<br>$I_{CC} = 4.0 mA$ , $L_{in} = 0 mA$ ,<br>$R_T = 3.0 \Omega$ | —   | 1     | 30       | $\mu A$<br>mA |
| Input Capacitance                   | $C_{in}^{***}$                                        | $V_{II} = 0 V$ , $f = 1 MHz$ , $T_a = 25^\circ C$                                                          | —   | 1.5   | 3.0      | pF            |
| Output Capacitance                  | $C_{out}^{***}$                                       | $V_{II} = 0 V$ , $f = 1 MHz$ , $T_a = 25^\circ C$                                                          | —   | —     | 10       | pF            |

\* Steady state current \*\*  $V_{CC} = 5V$ ,  $T_a = 25^\circ C$

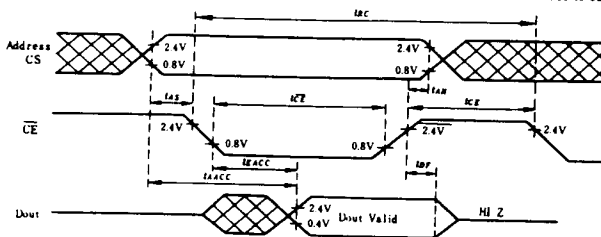
\*\*\* This parameter is sampled and not 100% tested.

# **■ AC CHARACTERISTICS**

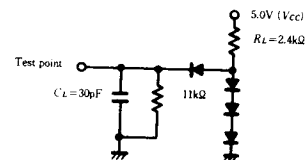
● READ CYCLE ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0 \sim +75^\circ C$ ,  $t_r = t_f = 20 ns$ )

| Item                        | Symbol     | min  | max | Unit    |
|-----------------------------|------------|------|-----|---------|
| Read Cycle Time             | $t_{RC}$   | 4.0  | —   | $\mu s$ |
| Address Access Time         | $t_{AAC}$  | —    | 3.5 | $\mu s$ |
| Chip Enable Access Time     | $t_{EACC}$ | —    | 3.0 | $\mu s$ |
| Data Hold Time from Address | $t_{DP}^*$ | 0.05 | 0.5 | $\mu s$ |
| Address Set-up Time         | $t_{AS}$   | 0.5  | —   | $\mu s$ |
| Address Hold Time           | $t_{AH}$   | 0    | —   | $\mu s$ |
| Chip Enable ON Time         | $t_{CE}$   | 3.0  | —   | $\mu s$ |
| Chip Enable OFF Time        | $t_{CE}$   | 0.5  | —   | $\mu s$ |

\*  $t_{DP}$  defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.



# **● AC TEST LOAD**



- Notes) 1.  $t_r = t_f = 20 ns$ .  
2.  $C_L$  includes jig capacitance.  
3. All diodes are 1S2074 (D).



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