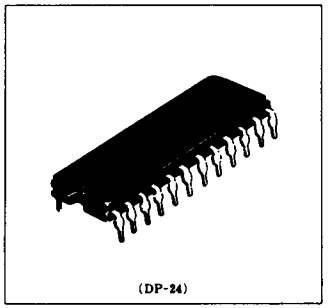
HN61365P

8192-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN61365P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS input and the memory content are defined by the user. The chip select input deselects the output and puts the chip in a power-down mode.

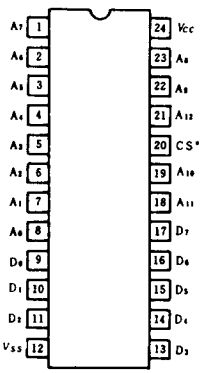


(DP-24)

■FEATURES

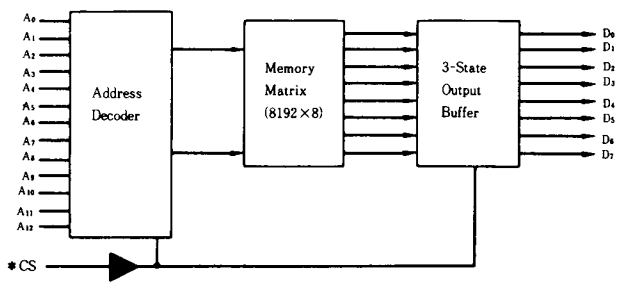
- Fully Static Operation
- Automatic Power Down
- Single +5 V Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



* Active level defined by the user.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
All Input and Output Voltage*	V_T	−0.3 to +7.0	V
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (under bias)	T_{bias}	−20 to +85	°C

* with respect to V_{SS}

■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	℃

* With respect to V_{SS}

■ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, V_{SS}=0V, Ta=−20 to +75℃)

Item	Symbol	Test Conditions		min	typ**	max	Unit
Input Voltage	V_{IH}			2.2	—	V_{CC}	V
	V_{IL}			−0.3	—	0.8	V
Output Voltage	V_{OH}	I_{OH}=−205μA		2.4	—	—	V
	V_{OL}	I_{OL}=3.2mA		—	—	0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0~5.5V		—	—	2.5	μA
Output Leakage Current	I_{LOH}	CS=0.8V, $\overline{CS}$=2.2V	V_{out}=2.4V	—	—	10	μA
	I_{LOL}		V_{out}=0.4V	—	—	10	μA
Active Supply Current	I_{CC}*	V_{CC}=5.5V, I_{OUT}=0mA, t_{RC}=min, duty=100%		—	10	25	mA
Stand by Supply Current	I_{SB}	$\overline{CS}$≧V_{CC}−0.2V, CS≦0.2V, V_{CC}=5.5V		—	1	30	μA
Input Capacitance	C_{in}***	V_{in}=0V, f=1MHz, Ta=25℃		—	—	10	pF
Output Capacitance	C_{out}***			—	—	15	pF

* Steady state current ** V_{CC}=5V, T_a=25℃ *** This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS

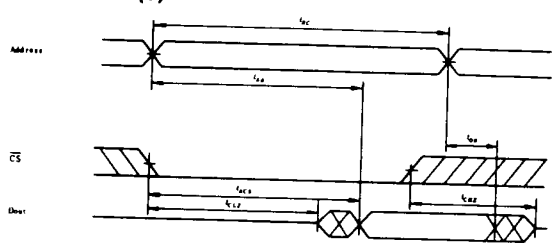
●READ CYCLE (V_{CC}=5V±10%, V_{SS}=0V, Ta=−20 to +75℃, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}*	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

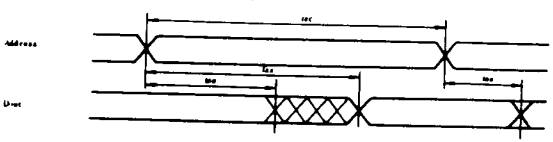
* t_{CHZ} defind the time at which the output achives the open circuit condition and is not reference to output voltage levels.

■TIMING WAVEFORM

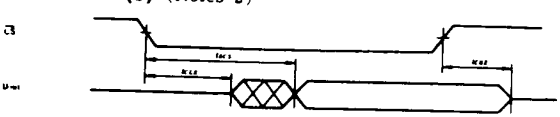
●READ CYCLE (1)



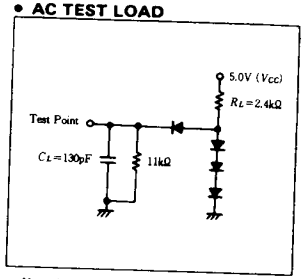
●READ CYCLE (2) (Notes 1)



●READ CYCLE (3) (Notes 2)



● AC TEST LOAD



Notes) 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

Notes)
1. Device is continuously selected
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. Input pulse level : 0.8 to 2.4V
4. Input and output timing reference level : 1.5V