

# HN62302B Series

## 2M (256K x 8-bit) Mask ROM

### ■ DESCRIPTION

The Hitachi HN62302B is a 2-Megabit CMOS Mask Programmable ROM organized as 262,144 x 8 bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

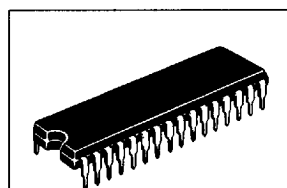
Hitachi's HN62442B is offered with JEDEC-Standard pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages.

### ■ FEATURES

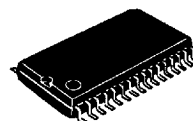
- Single Power Supply:  
 $V_{CC} = 5 V \pm 10\%$
- Fast Access Times:  
170 ns/200 ns (max)
- Low Power Consumption:  
Active Current: 100 mW (typ)  
Standby Current: 5  $\mu$ W (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:  
JEDEC Standard Byte-Wide EPROM
- Packages:  
32-pin Plastic DIP  
32-lead Plastic SOP  
32-lead Plastic TSOP (Type II)

### ■ ORDERING INFORMATION

| Type No.   | Access Time      | Package                           |
|------------|------------------|-----------------------------------|
| HN62302BP  | 170 ns<br>200 ns | 32-pin Plastic DIP<br>(DP-32)     |
| HN62302BF  | 170 ns<br>200 ns | 32-lead Plastic SOP<br>(FP-32D)   |
| HN62302BTT | 170 ns<br>200 ns | 32-lead Plastic TSOP<br>(TTP-32D) |



(DP-32)

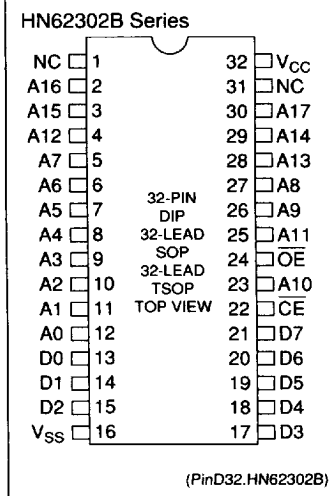


(FP-32D)



(TTP-32D)

### ■ PIN ARRANGEMENT



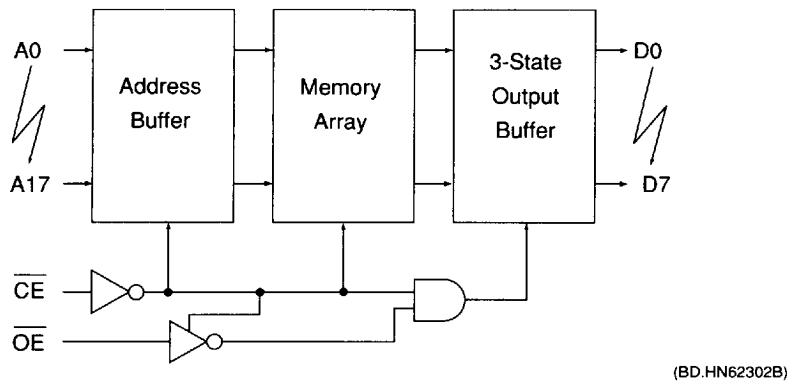
4496203 0025251 178

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BLOCK DIAGRAM



PIN DESCRIPTION

| Pin Name                         | Function      |
|----------------------------------|---------------|
| A <sub>0</sub> - A <sub>17</sub> | Address       |
| D <sub>0</sub> - D <sub>7</sub>  | Output        |
| $\overline{\text{CE}}$           | Chip Enable   |
| $\overline{\text{OE}}$           | Output Enable |
| V <sub>CC</sub>                  | Power Supply  |
| V <sub>SS</sub>                  | Ground        |
| NC                               | No Connection |

ABSOLUTE MAXIMUM RATINGS

| Item                                      | Symbol            | Value                         | Unit |
|-------------------------------------------|-------------------|-------------------------------|------|
| Supply Voltage <sup>1</sup>               | V <sub>CC</sub>   | -0.3 to +7.0                  | V    |
| All Input and Output Voltage <sup>1</sup> | V <sub>T</sub>    | -0.3 to V <sub>CC</sub> + 0.3 | V    |
| Operating Temperature Range               | T <sub>OPR</sub>  | 0 to +70                      | °C   |
| Storage Temperature Range                 | T <sub>STG</sub>  | -55 to +125                   | °C   |
| Temperature Under Bias                    | T <sub>BIAS</sub> | -20 to +85                    | °C   |

Note: 1. Relative to V<sub>SS</sub>.

CAPACITANCE

(V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 25°C, V<sub>IN</sub> = 0V, f = 1MHz)

| Item                            | Symbol           | Min. | Typ. | Max. | Unit |
|---------------------------------|------------------|------|------|------|------|
| Input Capacitance <sup>1</sup>  | C <sub>IN</sub>  | -    | -    | 15   | pF   |
| Output Capacitance <sup>1</sup> | C <sub>OUT</sub> | -    | -    | 15   | pF   |

Note: 1. This parameter is sampled and not 100% tested.

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■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $+70^\circ C$ )

| Item                       | Symbol   | Min. | Typ. | Max.           | Unit    | Test Condition                                              |
|----------------------------|----------|------|------|----------------|---------|-------------------------------------------------------------|
| Input Leakage Current      | $I_{LI}$ | -    | -    | 10             | $\mu A$ | $V_{IN} = 0$ to $V_{CC}$                                    |
| Output Leakage Current     | $I_{LO}$ | -    | -    | 10             | $\mu A$ | $\overline{CE} = 2.2V$ , $V_{OUT} = 0$ to $V_{CC}$          |
| Operating $V_{CC}$ Current | $I_{CC}$ | -    | -    | 50             | mA      | $V_{CC} = 5.5V$ , $ID_{OUT} = 0$ mA, $t_{RC} = \text{min.}$ |
| Standby $V_{CC}$ Current   | $I_{SB}$ | -    | -    | 30             | $\mu A$ | $V_{CC} = 5.5V$ , $\overline{CE} \geq V_{CC} - 0.2V$        |
| Input Voltage              | $V_{IH}$ | 2.2  | -    | $V_{CC} + 0.3$ | V       |                                                             |
|                            | $V_{IL}$ | -0.3 | -    | 0.8            | V       |                                                             |
| Output Voltage             | $V_{OH}$ | 2.4  | -    | -              | V       | $I_{OH} = -205 \mu A$                                       |
|                            | $V_{OL}$ | -    | -    | 0.4            | V       | $I_{OL} = 1.6$ mA                                           |

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $+70^\circ C$ )

Test Conditions

- Input pulse levels: 0.8 / 2.4V
- Input rise and fall times:  $\leq 10$  ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

| Item                                           | Symbol    | HN62302B-17 |      | HN62302B-20 |      | Test Unit |
|------------------------------------------------|-----------|-------------|------|-------------|------|-----------|
|                                                |           | Min.        | Max. | Min.        | Max. |           |
| READ Cycle Time                                | $t_{RC}$  | 170         | -    | 200         |      | ns        |
| Address Access Time                            | $t_{AA}$  | -           | 170  | -           | 200  | ns        |
| Chip Enable Access Time                        | $t_{ACE}$ | -           | 170  | -           | 200  | ns        |
| Output Enable Access Time                      | $t_{OE}$  | -           | 70   | -           | 100  | ns        |
| Output Hold Time from Address Change           | $t_{DHA}$ | 0           | -    | 0           | -    | ns        |
| Output Hold Time from Chip Enable              | $t_{DHC}$ | 0           | -    | 0           | -    | ns        |
| Output Hold Time from Output Enable            | $t_{DHO}$ | 0           | -    | 0           | -    | ns        |
| Chip Enable to Output in High-Z <sup>1</sup>   | $t_{CHZ}$ | -           | 70   | -           | 70   | ns        |
| Output Enable to Output in High-Z <sup>1</sup> | $t_{OHZ}$ | -           | 70   | -           | 70   | ns        |
| Chip Enable to Output in Low-Z                 | $t_{CLZ}$ | 10          | -    | 10          | -    | ns        |
| Output Enable to Output in Low-Z               | $t_{OLZ}$ | 10          | -    | 10          | -    | ns        |

Note: 1.  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ 4496203 0025253 T40 ■

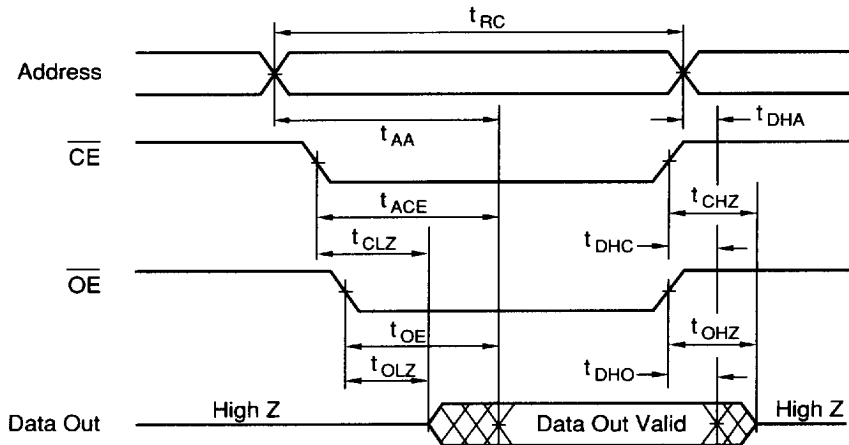
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■ READ TIMING WAVEFORM



(TD.R.HN62302B)

- Note:
1.  $t_{\text{DHA}}$ ,  $t_{\text{DHC}}$ ,  $t_{\text{DHO}}$  are determined by the faster time.
  2.  $t_{\text{AA}}$ ,  $t_{\text{ACE}}$ ,  $t_{\text{OE}}$  are determined by the slower time.
  3.  $t_{\text{CLZ}}$ ,  $t_{\text{OLZ}}$  are determined by the slower time.

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