

HN62304B Series

HN62324B Series

524288-Word × 8-Bit CMOS Mask Programmable ROM

HN62304B, HN62324B Series is a 4-Mbit CMOS mask-programmable ROM organized as 524288-word x 8-bits. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

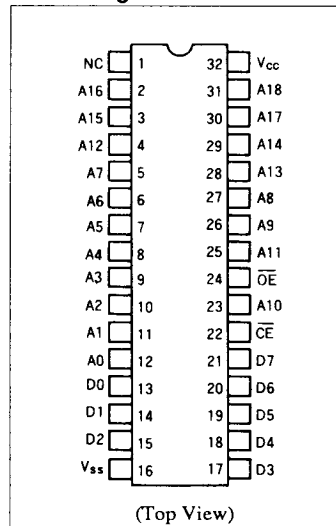
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max.)
- Low power: Active 100 mW (typ)
Standby 5 μ W (typ)
- Byte-Wide Data Organization

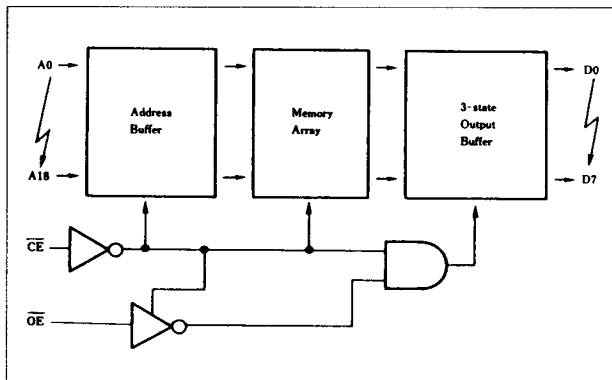
Ordering Information

Type No.	Address Access Time	Package
HN62304BP	200 ns	600 mil 32-pin
HN62324BP	150 ns	plastic DIP
HN62304BF	200 ns	32-pin
HN62324BF	150 ns	plastic SOP

Pin Arrangement



Block Diagram



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Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V _{CC}	-0.3 to +7.0	V
Terminal voltage*1	V _T	-0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C
Bias temperature	T _{bias}	-20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, T_a = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{HI}	2.2	—	V _{CC} + 0.3	V
	V _{IL}	-0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 0 to +70°C)

Item	Symbol	Min	Max	Unit	Test Conditions
Power supply current	I _{CC}	—	50	mA	V _{CC} = 5.5 V, I _{OUT} = 0 mA, t _{RC} = Min
	I _{SB}	—	30	μA	V _{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current	I _{LI}	—	10	μA	V _{IN} = 0 to V _{CC}
Output leak current	I _{LO}	—	10	μA	$\overline{CE} = 2.2$ V, V _{OUT} = 0 to V _{CC}
Output voltage	V _{OH}	2.4	—	V	I _{OH} = -205 μA
	V _{OL}	—	0.4	V	I _{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 25°C, V_{in} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	C _{in}	—	15	pF
Output capacitance*1	C _{out}	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.



AC Operating Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to } +70^\circ\text{C}$)**Test Conditions**

Input pulse level: 0.8 to 2.4 V
 I/O timing reference level: 1.5 V
 Input rise/fall time: 10 ns

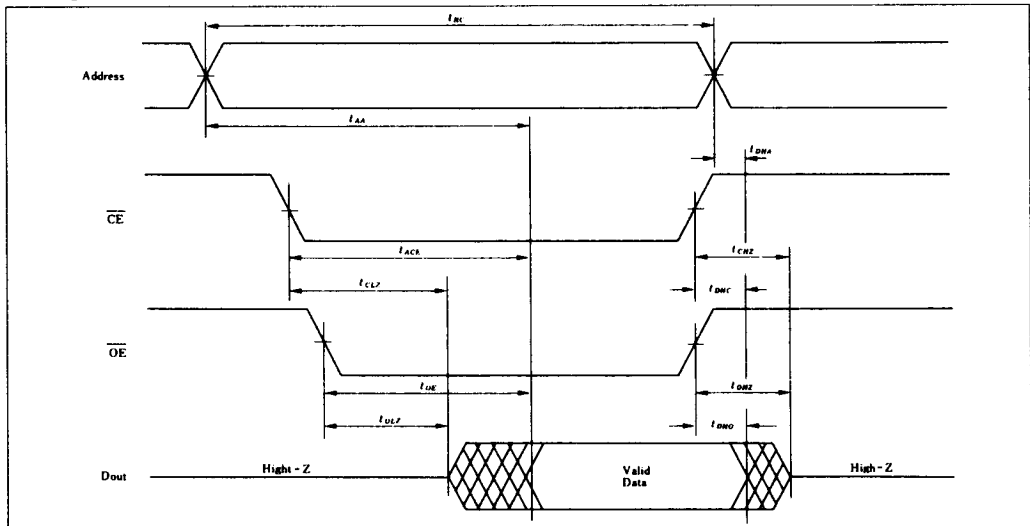
Output load: 1 TTL gate + $C_L = 100\text{ pF}$
 (including jig capacitance)

Item	Symbol	HN62324B		HN62304B		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}^{*1}	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}^{*1}	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns

Note: *1 t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.



Timing Waveform



- Notes:
1. t_{DHA} , t_{DHC} , t_{DHO} ; Determined by whichever is faster.
 2. t_{AA} , t_{ACE} , t_{OE} ; Determined by whichever is slower.
 3. t_{CLZ} , t_{OLZ} ; Determined by whichever is slower.

