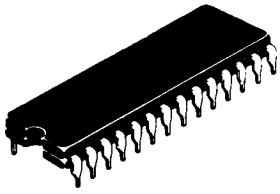
HN623258P, HN623258F

32768-Word × 8-Bit CMOS Mask Programmable ROM

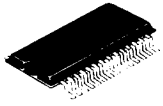
HN623258P/F is a 256-Kbit CMOS mask-programable ROM organized as 32768-word x 8-bit. It can be operated with a battery because of low power consumption.

HN623258P



(DP-28)

HN623258F

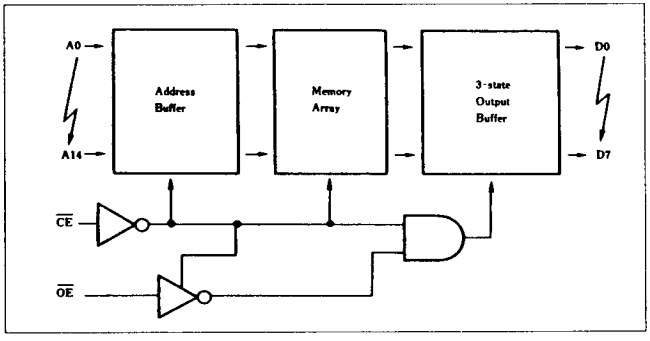


(FP-28DA)

Features

- Low power: Active 100 mW (typ), Standby 5 µW (typ)
- Addres access time: 200 ns (max)
- Single 5 V
- TTL compatible
- Wired OR is permitted for the output in three states

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	Vcc	–0.3 to +7.0	V
Terminal voltage*1	VT	–0.3 to Vcc +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

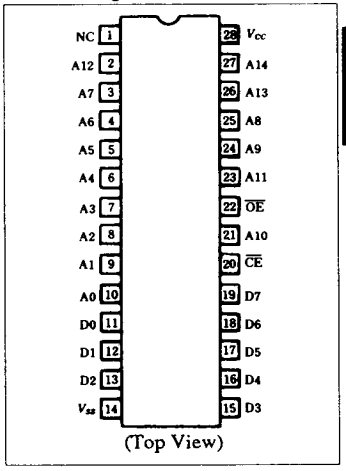
Note: *1. With respect to Vss.

Recommended Operating Conditions

(Vss = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	VIH	2.2	—	Vcc + 0.3	V
	VIL	–0.3	—	0.8	V

Pin Arrangement



(Top View)

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	45	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current		$\|I_{LI}\|$	—	10	µA	V_{IN} = 0 to 5.5 V
Output leak current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacity	Cin	—	10	pF
Output capacity	Cout	—	15	pF

Note: This parameter is samples and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

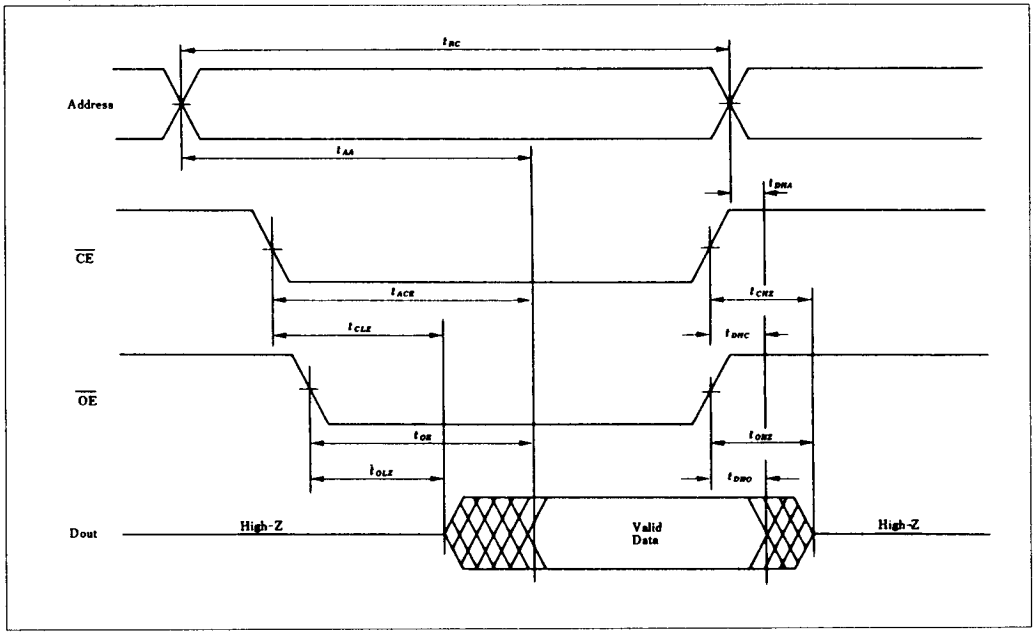
Test Condition

Input pulse level: 0.8 to 2.4V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	Min	Max	Unit
Cycle time	t_{RC}	200	—	ns
Address access time	t_{AA}	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	200	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
Output Holt Time from Address Change	t_{DHA}	0	—	ns
$\overline{CE}$ to Output in High Z*1	t_{CHZ}	—	70	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
$\overline{OE}$ access time	t_{OE}	—	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{OE}$ to Output in High Z*1	t_{OHZ}	—	70	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns

Note: *1 t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.