HN62344B Series — HITACHI/ LOGIC/ARRAYS/MEM

524288-word × 8-bit CMOS Mask Programmable Read Only Memory

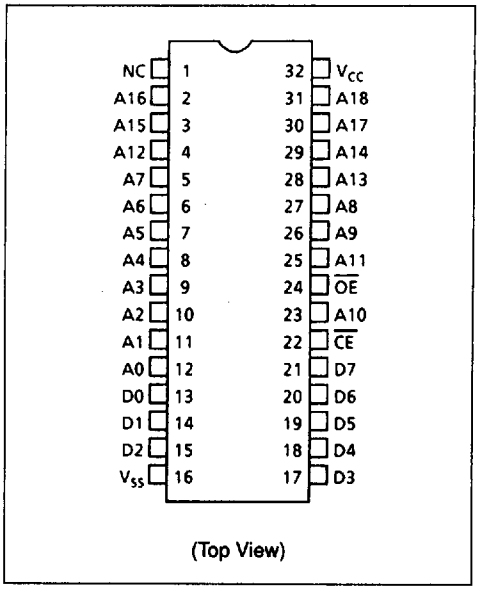
T-46-13-15

The HN62344B is a 4-Mbit CMOS mask-programmable ROM organized as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

Features

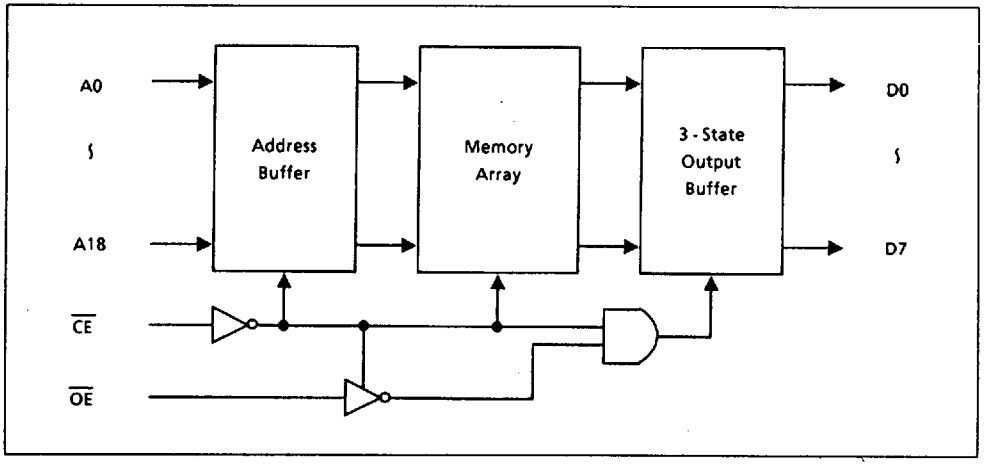
- Single +5 V power supply
- Wired OR is permitted for the output in three states.
- TTL compatible
- Maximum access time: 100 ns (max)
- Low power consumption: 150 mW (typ) active
  5 µW (typ) standby
- Byte-wide data organization
- Pin compatible with JEDEC (EP-ROM)

Pin Arrangement



(Top View)

Block Diagram



Ordering Informations

Type No.	Access time	Package
HN62344BP	100 ns	600-mil 32-pin plastic DIP (DP-32)
HN62344BF	100 ns	32-pin plastic SOP (FP-32D)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.45	V

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DC Electrical Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	60	mA	V_{CC} = 5.25 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.25 V, $\overline{CE} \geq V_{CC} - 0.2$ V
		I_{SB2}	—	3	mA	V_{CC} = 5.25 V, $\overline{CE} \geq$ 2.4 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.4 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = −205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	C_{IN}	—	15	pF
Output capacitance	C_{OUT}	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Electrical Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C)

- Output load: 1 TTL gate + CL = 100 pF (including jig capacitance)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	100	—	ns
Address access time	t_{AA}	—	100	ns
$\overline{CE}$ access time	t_{ACE}	—	100	ns
$\overline{OE}$ access time	t_{OE}	—	55	ns
Output hold time from address change	t_{DHA}	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*1	—	40	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*1	—	40	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	ns

Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

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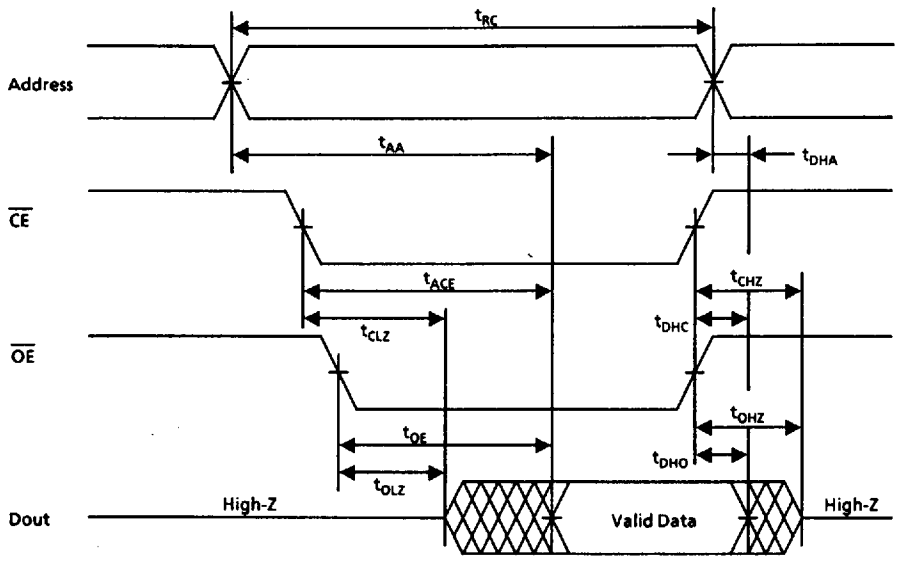
Timing Diagram



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.