

HN62404 Series**HN62424 Series**

T-46-13-15

262144-Word × 16-Bit/524288-Word × 8-Bit CMOS Mask Programmable ROM

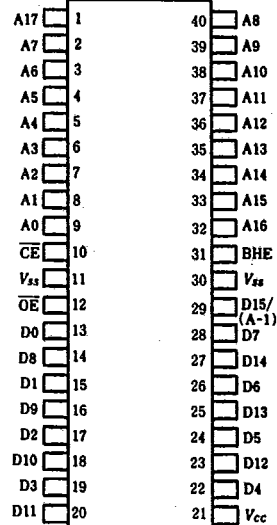
HN62404, HN62424 Series is a 4-Mbit CMOS mask-programmable ROM organized either as 262144-word x 16-bit or as 524288-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

Features

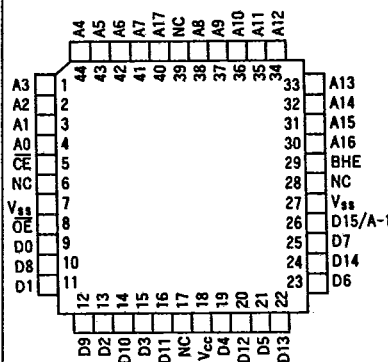
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max)
- Low power: Active 100 mW (typ)
Standby 5 μ W (typ)
- Byte-Wide or Word-Wide Data Organization (switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62404P	200 ns	600 mil 40-pin
HN62424P	150 ns	plastic DIP
HN62404FP	200 ns	44-pin
HN62424FP	150 ns	plastic QFP

Pin Arrangement**HN62404, HN62424P**

(Top View)

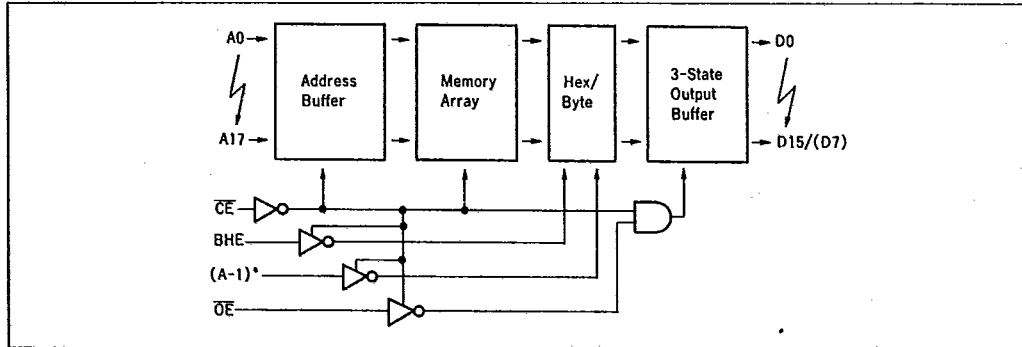
HN62404FP, HN62424FP

(Top View)



Block Diagram

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BHE = V_{IH} : 16 bits (D15–D0)BHE = V_{IL} : 8 bits (D7–D0)

*1: A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_I	–0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C
Bias temperature	T_{bias}	–20 to +85	°C

Note: *1. With respect to V_{SS} .Recommended Operating Conditions ($V_{SS} = 0$ V, $T_a = 0$ to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics ($V_{CC} = 5$ V $\pm 10\%$, $V_{SS} = 0$ V, $T_a = 0$ to +70°C)

Item	Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active I_{CC}	—	50	mA	$V_{CC} = 5.5$ V, $I_{DOUT} = 0$ mA, $t_{rc} = \text{Min}$
	Standby I_{SB}	—	30	μA	$V_{CC} = 5.5$ V, $CE \geq V_{CC} - 0.2$ V
Input leak current	$ I_{LI} $	—	10	μA	$V_{IN} = 0$ to V_{CC}
Output leak current	$ I_{LO} $	—	10	μA	$CE = 2.2$ V, $V_{OUT} = 0$ to V_{CC}
Output voltage	V_{OH}	2.4	—	V	$I_{OH} = -205$ μA
	V_{OL}	—	0.4	V	$I_{OL} = 1.6$ mA



Capacitance ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{in} = 0\text{ V}$, $f = 1\text{ MHz}$)

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Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)**Test Conditions**

Input pulse level: 0.8 to 2.4 V

Output load:

1 TTL gate + $C_L = 100\text{ pF}$

I/O timing reference level: 1.5 V

(including jig capacitance)

Input rise/fall time: 10 ns

Item	Symbol	HN62424		HN62404		Unit
		Min	Max	Min	Max	
Cycle time	trc	150	—	200	—	ns
Address access time	tAA	—	150	—	200	ns
CE access time	tACE	—	150	—	200	ns
OE access time	tOE	—	70	—	100	ns
BHE access time	tBHE	—	150	—	200	ns
Output Hold Time from Address Change	tDHA	0	—	0	—	ns
Output Hold Time from CE	tDHC	0	—	0	—	ns
Output Hold Time from OE	tDHO	0	—	0	—	ns
Output Hold Time from BHE	tDHB	0	—	0	—	ns
CE to Output in High Z	tCHZ*1	—	70	—	70	ns
OE to Output in High Z	tOHZ*1	—	70	—	70	ns
BHE to Output in High Z	tBHZ*1	—	70	—	70	ns
CE to Output in Low Z	tCLZ	10	—	10	—	ns
OE to Output in Low Z	tOLZ	10	—	10	—	ns
BHE to Output in Low Z	tBLZ	10	—	10	—	ns

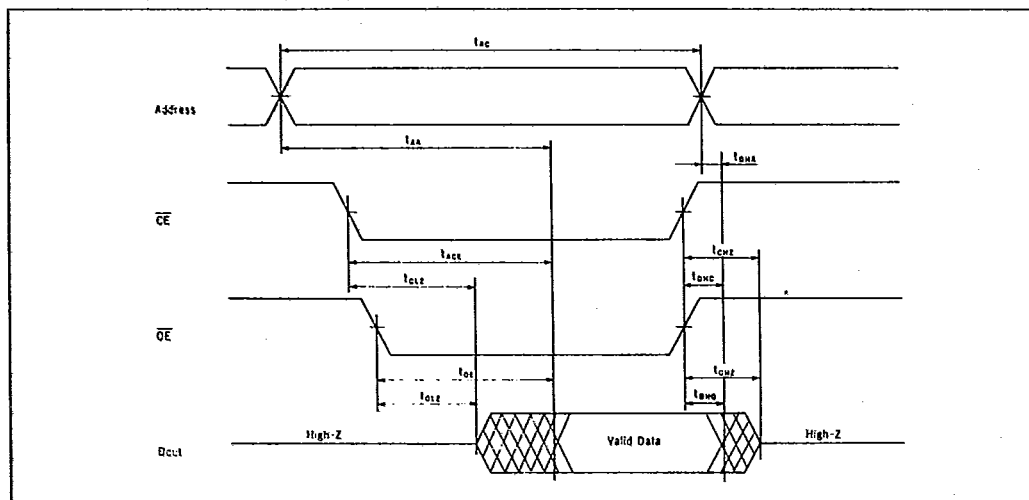
Note: *1 tCHZ, tOHZ, and tBHZ define the time at which the output goes to the high impedance state and is not referenced to output voltage level.



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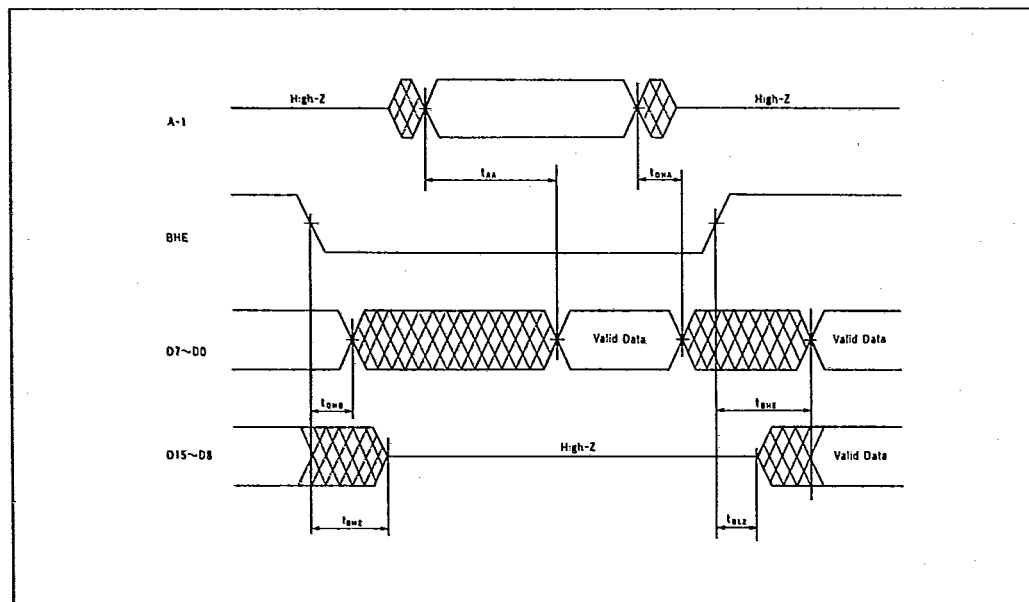
Timing Waveform

Word Mode (BHE = "V_{IH}") or Byte Mode (BHE = "V_{IL}")



- Notes: 1. IDHA, IDHC, IDHO; Determined by whichever is faster.
 2. t_{aa}, t_{oe}, t_{ol}; Determined by whichever is slower.
 3. t_{clz}, t_{olz}; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



- Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A17~A0 are fixed.
 2. D15/A-1 terminal is of output state when BHE = V_{IH}, CE and OE are of selected state.
 At this time, an input signal that is of the inverse phase to the output should not be impressed.

