HN62W5016N Series

Low Voltage (3.3 ± 0.3 V), High Speed, and Burst (A0, A1 Burst) 524288-word × 32-bit/1048576-word × 16-bit CMOS MASK Programmable ROM

HITACHI

Under development
Rev. 0.00
Nov., 1994

The HN62W5016N is a 16-Mbit CMOS mask-programmable ROM organized either as 524,288 words by 32 bits or as 1,048,576 words by 16 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns is the most suitable to the system using a high speed micro-computer by 32 bits.

Ordering Information

Type No.	Access time	Package
HN62W5016NF-12	120 ns	70 pin
HN62W5016NF-15	150 ns	plastic SSOP

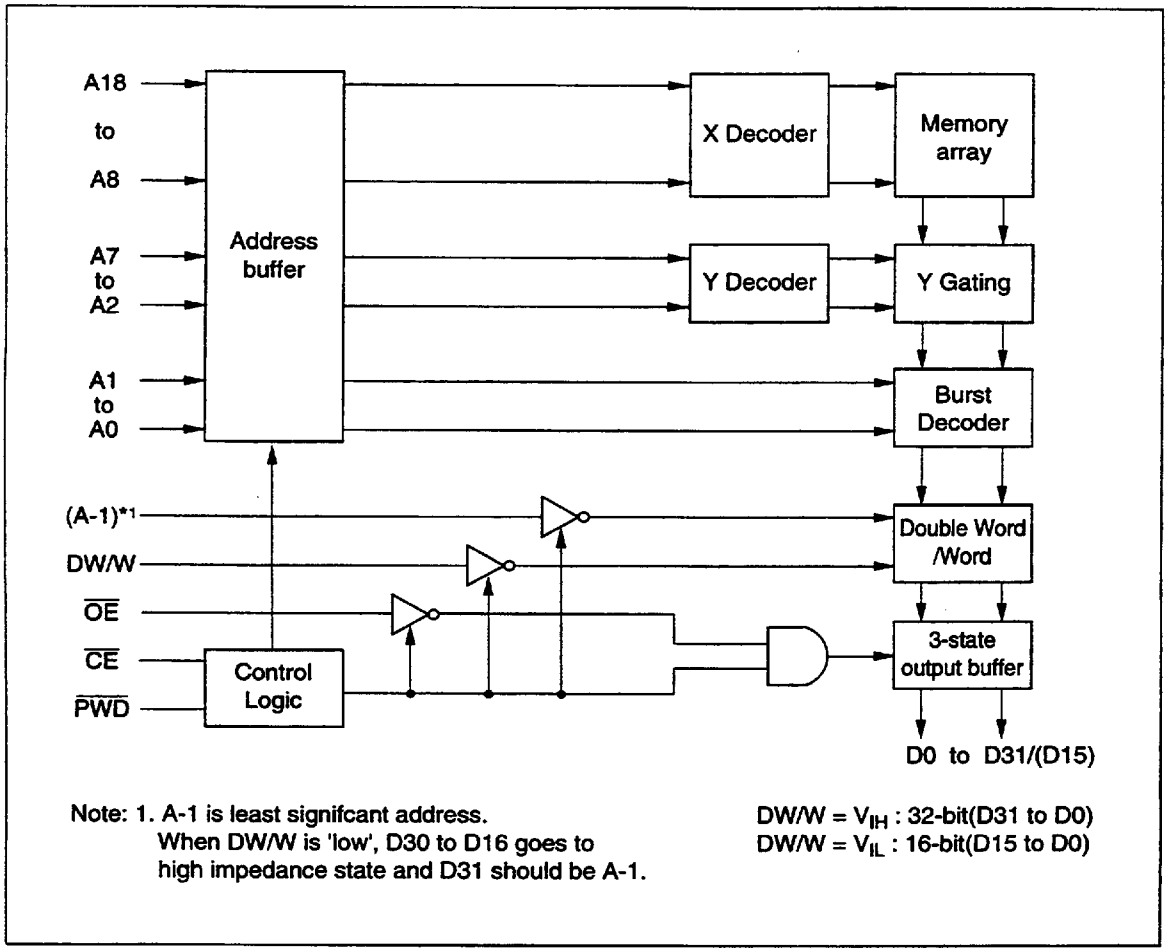
Features

- Low voltage operation: 3.3 V ± 0.3 V
- High Speed
  Normal access time: 120 ns/150 ns (max)
  Burst access time: 40 ns/50 ns (max)
- Low power consumption:
  360 mW (max) active
  0.72 mW (max) standby
  36 µW (max) power down mode
- Double word-wide or word-wide data organization with DW/W
- 4 double-word burst access on double word-wide mode
  8 word burst access on word-wide mode
- Three-state data output for or-tying
- LVTTL compatible

Note: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

Block Diagram

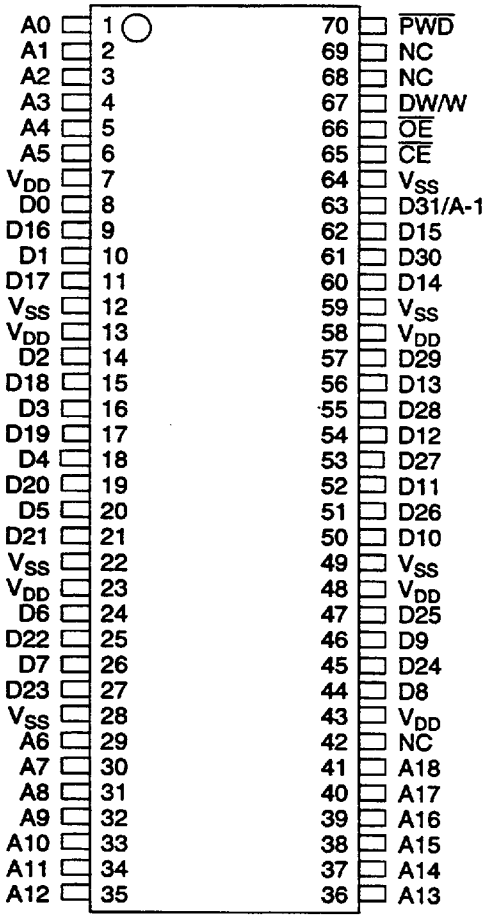


Note: 1. A-1 is least signifcant address.
When DW/W is 'low', D30 to D16 goes to high impedance state and D31 should be A-1.

DW/W = V_{IH} : 32-bit(D31 to D0)
DW/W = V_{IL} : 16-bit(D15 to D0)

Pin Arrangement

HN62W5016NF



(Top view)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.3 to +5.5	V	1
All input and outpu tvoltage	Vin, Vout	–0.3 to V_{DD} + 0.3	V	1
Operating temperatue range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{DD} = 3.3 ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Item		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{DD}	—	100	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB1}	—	200	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq 2.2$ V
	Power down	I_{PWD}	—	10	µA	V_{DD} = 3.6 V, $\overline{PWD} \leq 0.2$ V
Input leakage current		$\|I_{IL}\|$	—	10	µA	V_{IN} = 0 to V_{DD}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{DD}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –2 mA
		V_{OL}	—	0.4	V	I_{OL} = 2 mA

Capacitance (V_{DD} = 3.3 ±0.3 V, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	10	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Electrical Characteristics (V_{DD} = 3.3 ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

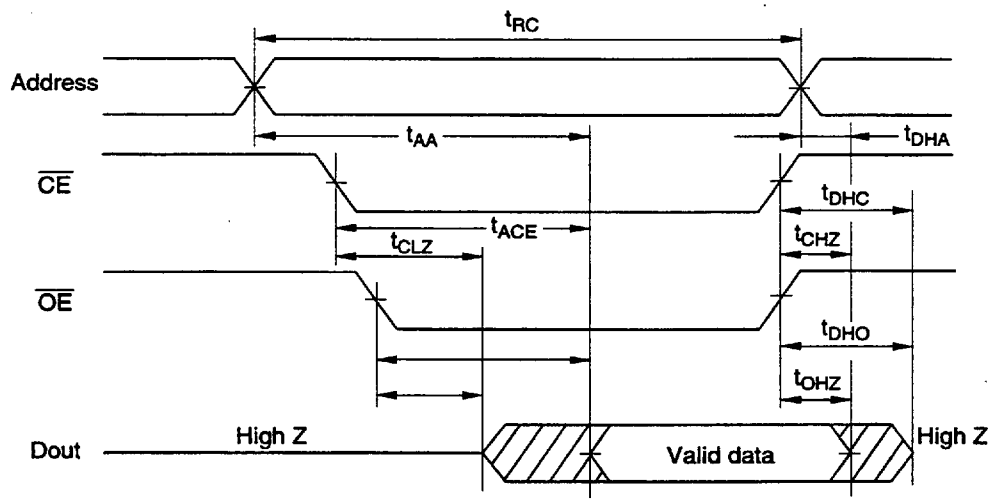
- Output load: 1TTL + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5 ns

		HN62W5016N-12		HN62W5016N-15			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Burst read cycle time	t_{BC}	40	—	50	—	ns	
Address access	t_{AA}	—	120	—	150	ns	
Burst access time	t_{BA}	—	40	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns	
DW/W access time	t_{DWW}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from DW/W	t_{DHD}	0	—	0	—	ns	
Output hold time from $\overline{PWD}$	t_{DHP}	0	—	0	—	ns	
$\overline{CE}$ to output in high Z	t_{CHZ}	—	40	—	50	ns	1
$\overline{OE}$ to output in high Z	t_{OHZ}	—	40	—	50	ns	1
DW/W to output in high Z	t_{DHZ}	—	40	—	50	ns	1
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	5	—	ns	
DW/W to output in low Z	t_{DLZ}	5	—	5	—	ns	
Recovery time from $\overline{PWD}$	t_R	10	—	10	—	µs	

Note: 1. t_{CHZ}, t_{OHZ} and t_{DHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

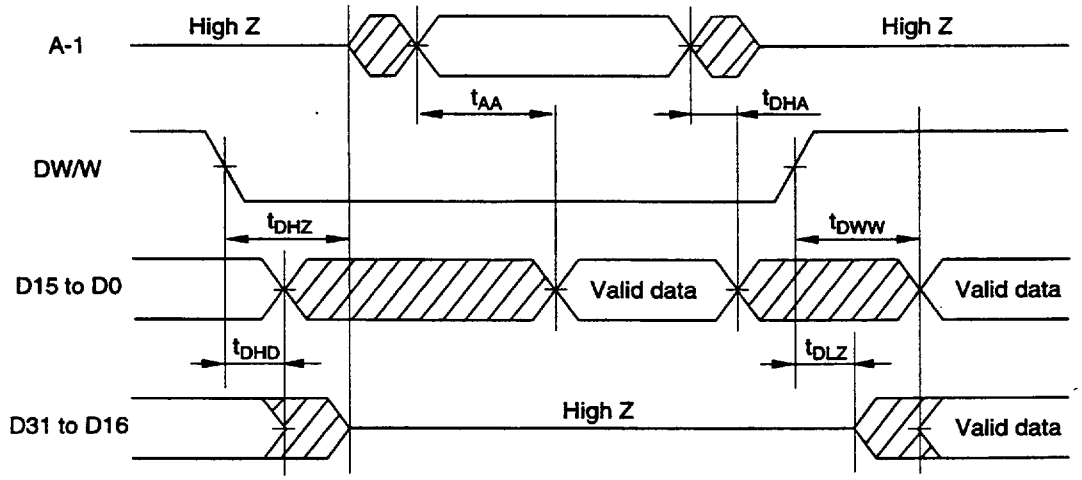
Timing Diagram

(1) Double word mode (DW/W = 'Hign') or Word mode (DW/W = 'Low')



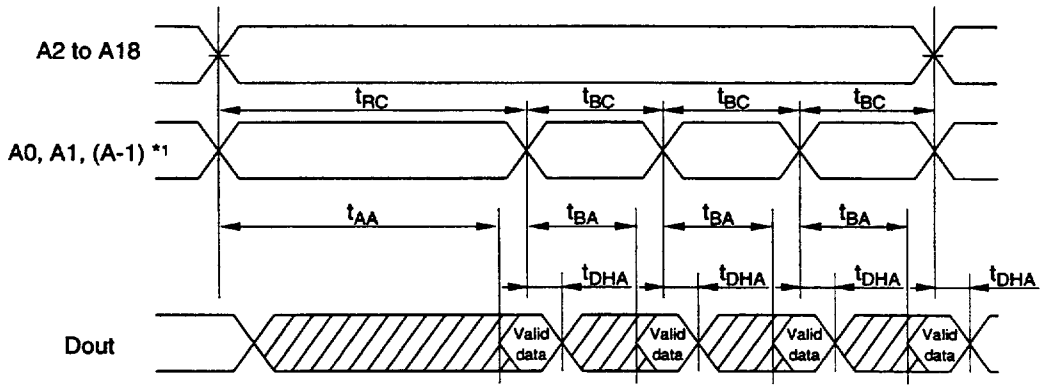
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

(2) Double word mode, Word mode switch



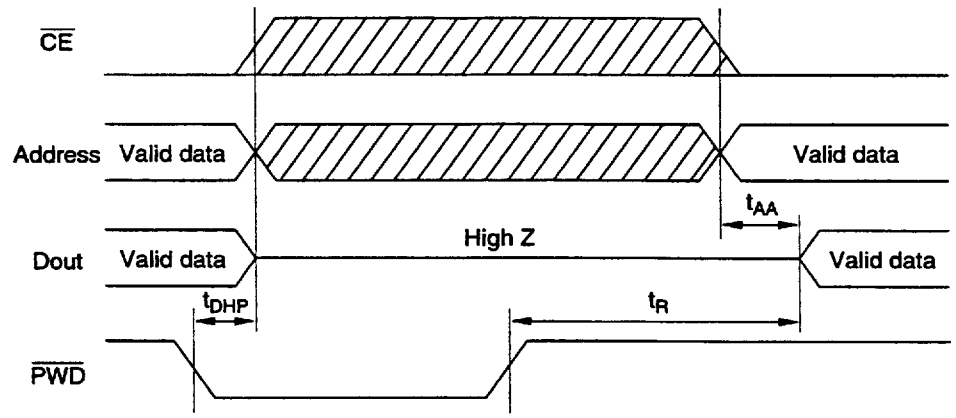
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A18 to A0 are valid.
2. D31/A-1 pin is in the output state when DW/W is DW/W is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the oinput signals of opposite phase to the output must not be applied them.

(3) Burst mode

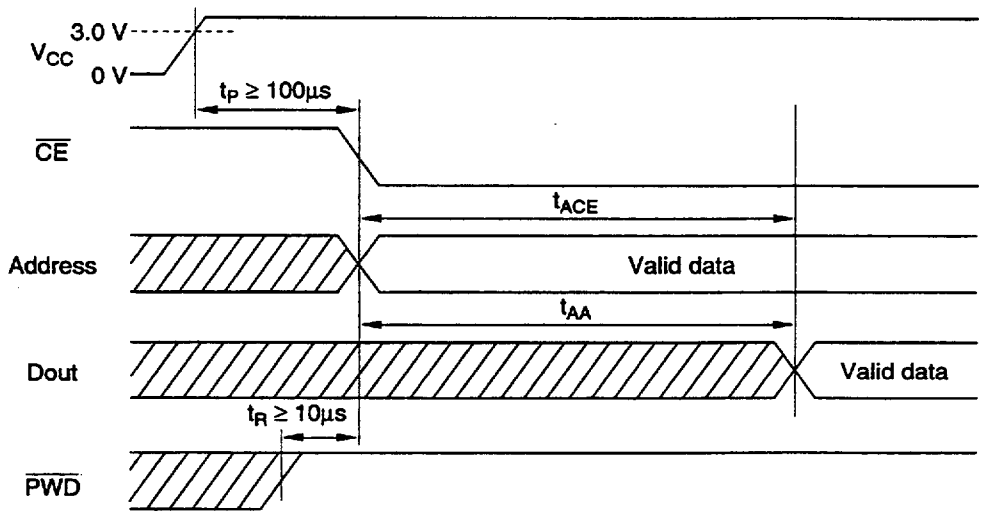


Notes: 1. Burat address is determind as below
Double word mode (DW/W = 'High'): A0, A1
Word mode (DW/W = 'Low'): A-1, A0, A1
2. $\overline{CE}$ and $\overline{OE}$ are enable.

(4) Power down mode



Power Up Sequence



Notes: 1. This device is used ATD(Address Transition Detector). Therefore, transfer either $\overline{CE}$ or address(A18 to A2) after power up to 3.0 V.
3. t_P, t_R: Determined by slower.