HEWLETT PACKARD

Silicon Bipolar Monolithic Variable Gain Amplifier

Technical Data

HPVA-0180

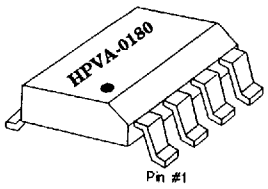
Features

- **3 dB Bandwidth: DC to 2.5 GHz**
- **Temperature Compensated Bias**
- **Single Ended or Differential Operation**
- **Low Cost Plastic Surface Mount Package**
- **Linearized Gain Control (S_{21} Magnitude)**

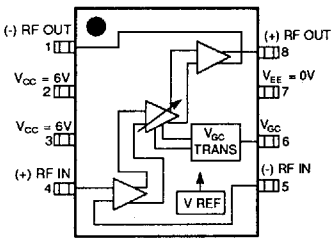
Applications

- **VHF/UHF Transceivers**
- **RF Data Links**
- **Broadband LAN's**

Plastic SO-8 Package



Functional Block Diagram and Pin Configuration



HPVA-0180
Absolute Maximum Ratings, T_A = 25°C*

Device Voltage, V_{CC} ..... 7 Volts
RF Input Power, P_{in} ..... +10 dBm
Gain Control Voltage, V_{GC} ..... 0 Volts to V_{CC}
Junction Temperature, T_j ..... +150°C
Storage Temperature, T_{stg} ..... -55° to +150°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Care should be taken to prevent Electro Static Discharge (ESD) that could permanently damage the device. (Class II sensitivity)

Notes:

1. A θ_{JA} of 200°C/W should be used for derating and junction temperature calculations: $T_J = (P_D \times \theta_{JA}) + T_A$
2. Maximum soldering temperature is 260°C for 5 seconds.

Description

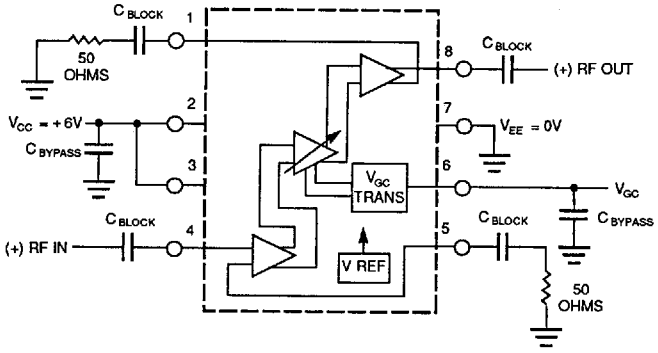
The HPVA-0180 is a silicon monolithic variable gain amplifier in a plastic surface mount SO-8 package. It is designed for wide or narrow bandwidth applications from DC to 2.5 GHz. The amplifier provides 20 dB gain (26 dB in differential operation) with 20 dB gain control over its entire DC to 2.5 GHz bandwidth, and dissipates only 250 mW from a single 6 volt power supply. The device may be operated in any combination of single-ended or differential input/output configurations.

The internal signal path of the amplifier is fully differential to achieve the highest possible immunity against transition noise. The HPVA-0180 also features a band-gap voltage reference to stabilize the bias against temperature variations and a gain control linearizer for linear gain change with gain control voltage variation.

The device is manufactured using Hewlett-Packard's 13 GHz F_t, 25 GHz F_{max} silicon bipolar integrated circuit process.

Electrical Specifications, T_A = 25°C

Symbol	Parameters / Test Conditions: V_{CC} = 6 V, Z_o = 50 Ohms, Single Ended Operation, Gain Set = +20 dB	Units	Min.	Typ.	Max.
G	Small Signal Gain $\|S_{21}\|^2$, V_{GC} = 5 Volts, f = 300 MHz	dB		21	
F_{3dB}	3 dB Bandwidth	GHz		2.5	
V_{GC}	Gain Control Range f = 300 MHz, V_{GC} = 3 to 5 Volts	dB		20	
P_{1dB}	Output Power at 1 dB Gain Comp. f = 300 MHz	dBm		-3	
IP_3	Output 3rd Order Intercept Point, F1 = 300 MHz, F2 = 305 MHz	dBm		7	
NF	50 Ohm Noise Figure f = 300 MHz	dB		16	
VSWR	Input VSWR V_{GC} = 3 to 5 Volts, f = 10 MHz to 2,000 MHz			1.8	
	Output VSWR V_{GC} = 3 to 5 Volts, f = 10 MHz to 2,000 MHz			1.8	
$\|S_{12}\|^2$	Isolation, $\|S_{12}\|^2$, f = 300 MHz	dB		32	
ΔG	Gain Flatness f = 10 MHz to 2,000 MHz	dB		±0.8	
I_{CC}	Supply Current	mA	30	41	60
I_{GC}	Gain Control Supply Current	mA		0.1	



Transmission lines (50 ohms) are recommended for all RF input and output connections. The use of chip capacitors and chip resistors will minimize unwanted parasitics.

Typical Biasing Configuration

FIBER OPTICS

HPVA-0180 Typical S-Parameters

Z_O = 50 Ohms, T_A = 25° C, V_{CC} = 6 V, V_{GC} Set for Nominal +20 dB Gain.

Frequency	S_{11}		S_{21}			S_{12}			S_{22}	
MHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
10	0.23	0	20.3	10.38	-2	-44.3	0.007	-34	0.09	2
50	0.24	-4	20.2	10.23	-9	-39.3	0.011	-113	0.10	7
100	0.21	-3	20.3	10.31	-17	-40.9	0.009	68	0.12	29
200	0.23	-3	20.2	10.25	-35	-33.7	0.021	56	0.16	26
300	0.19	-9	20.1	10.05	-53	-32.0	0.025	38	0.20	23
400	0.14	-1	19.8	9.75	-70	-27.0	0.045	23	0.20	17
500	0.15	18	19.4	9.32	-87	-27.7	0.041	15	0.24	16
600	0.18	29	19.0	8.94	-102	-26.5	0.047	3	0.29	0
700	0.25	31	18.7	8.65	-116	-27.7	0.041	-30	0.28	-21
800	0.28	23	18.8	8.66	-130	-29.2	0.035	-31	0.27	-43
900	0.30	11	19.0	9.88	-145	-31.8	0.026	-61	0.24	-66
1,000	0.28	-3	19.0	8.91	-161	-30.7	0.029	-76	0.21	-90
1,100	0.27	-15	19.3	9.24	-178	-40.9	0.009	-47	0.16	-109
1,200	0.23	-25	19.4	9.33	166	-37.3	0.014	-21	0.14	-110
1,300	0.20	-32	19.4	9.35	149	-36.3	0.015	3	0.15	-125
1,400	0.14	-34	19.6	9.59	132	-31.1	0.028	10	0.16	-142
1,500	0.12	-42	19.5	9.45	115	-30.1	0.031	-13	0.15	-156
1,600	0.09	-37	19.5	9.40	97	-28.3	0.039	0	0.15	-168
1,700	0.10	-10	19.3	9.21	79	-28.2	0.039	-16	0.14	-168
1,800	0.10	-14	19.5	9.45	62	-25.9	0.051	-32	0.11	-179
1,900	0.11	-21	19.4	9.29	45	-24.7	0.058	-46	0.16	174
2,000	0.12	-54	19.6	9.58	28	-24.1	0.062	-62	0.17	167
2,100	0.10	-68	19.9	9.85	9	-25.6	0.053	-49	0.21	159
2,200	0.10	-83	20.0	10.00	-12	-24.3	0.061	-60	0.28	139
2,300	0.06	-163	19.8	9.79	-33	-22.7	0.073	-71	0.34	122
2,400	0.08	158	19.5	9.43	-56	-23.6	0.066	-84	0.40	105
2,500	0.11	126	18.7	8.57	-76	-25.1	0.055	-90	0.43	90
2,600	0.17	103	17.7	7.89	-95	-24.6	0.059	-101	0.44	80
2,700	0.20	84	16.7	6.80	-115	-22.8	0.072	-99	0.46	66
2,800	0.24	69	15.6	6.00	-134	-23.7	0.065	-101	0.48	61
2,900	0.29	48	14.8	5.50	-153	-21.6	0.083	-115	0.45	56
3,000	0.36	45	14.0	5.03	-169	-23.0	0.071	-125	0.42	52
3,100	0.35	27	13.1	4.50	178	-23.7	0.065	-115	0.44	52
3,200	0.38	31	12.0	4.00	162	-21.0	0.089	-119	0.39	48
3,300	0.43	27	11.3	3.67	147	-20.9	0.091	-135	0.33	47
3,400	0.48	24	10.3	3.28	130	-20.6	0.094	-144	0.32	42
3,500	0.47	23	9.2	2.88	115	-20.2	0.098	155	0.24	43
4,000	0.40	15	5.1	1.81	44	-19.0	0.112	-166	0.18	90

HPVA-0180 Typical Performance Parameters

Z_O = 50 Ohms, T_A = 25° C, V_{CC} = 6 V, V_{GC} Set for Nominal +20 dB Gain.

Frequency MHz	Linear Phase Deviation (Deg.)	Relative Phase (Deg.)	Gain Deviation (dB)	Group Delay (ns)	Input VSWR	Output VSWR
10	-0.3	0.0	0.0	0.52	1.6	1.2
50	-0.7	-10.7	-0.01	0.46	1.6	1.2
100	-1.1	-19.5	0.00	0.49	1.6	1.3
200	-2.2	-37.0	-0.01	0.49	1.6	1.4
300	-3.0	-50.9	-0.02	0.48	1.5	1.5
400	-4.0	-72.1	-0.54	0.49	1.4	1.5
500	-4.0	-88.5	-0.93	0.46	1.4	1.7
600	-2.4	-103.5	-1.30	0.42	1.5	1.8
700	0.1	-117.6	-1.58	0.39	1.7	1.8
800	2.4	-131.7	-1.57	0.39	1.8	1.7
900	3.6	-147.1	-1.35	0.43	1.8	1.6
1,000	4.0	-163.1	-1.32	0.45	1.8	1.5
1,100	3.8	-180.0	-1.00	0.47	1.8	1.4
1,200	4.3	-196.1	-0.92	0.44	1.5	1.4
1,300	4.5	-212.4	-0.91	0.46	1.5	1.4
1,400	3.6	-229.7	-0.68	0.48	1.3	1.4
1,500	2.9	-247.1	-0.82	0.48	1.3	1.4
1,600	1.8	-264.7	0.85	0.49	1.2	1.4
1,700	0.6	-282.4	-1.04	0.50	1.3	1.3
1,800	0.1	-299.4	-0.82	0.48	1.2	1.3
1,900	-0.8	-317.0	-0.96	0.48	1.2	1.4
2,000	-1.2	-334.0	-0.69	0.47	1.3	1.4
2,100	-3.8	-353.0	-0.45	0.53	1.2	1.6
2,200	-7.5	-373.4	-0.29	0.56	1.2	1.8
2,300	-13.0	-395.2	-0.51	0.61	1.1	2.1
2,400	-18.8	-417.6	-0.83	0.62	1.2	2.4
2,500	-22.0	-437.4	-1.66	0.55	1.3	2.6
2,600	-24.8	-456.7	-2.46	0.53	1.4	2.5
2,700	-27.9	-476.5	-3.67	0.55	1.5	2.8
2,800	-31.0	-495.9	-4.75	0.55	1.7	2.8
2,900	-33.5	-514.9	-5.51	0.52	1.8	2.6
3,000	-32.4	-530.5	-6.29	0.43	2.2	2.4
3,100	-29.1	543.9	-7.26	0.37	2.1	2.5
3,200	-28.6	-559.9	-8.29	0.44	2.3	2.2
3,300	-26.7	-574.8	-9.29	0.43	2.6	2.1
3,400	-27.9	-591.8	-10.01	0.46	2.8	1.8
3,500	-25.5	-606.4	-11.12	0.42	3.0	1.7
4,000	-14.0	-677.5	-15.18	0.37	2.3	1.4

HPVA-0180 Typical Parameters

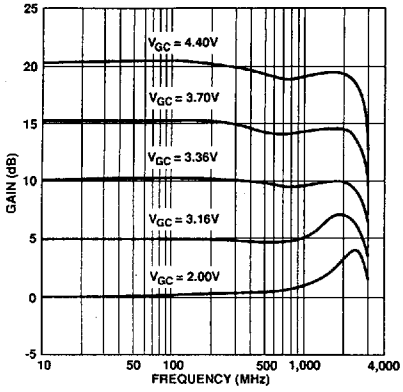


Figure 1. Typical Gain vs. Frequency over Gain Control Range at 25° C

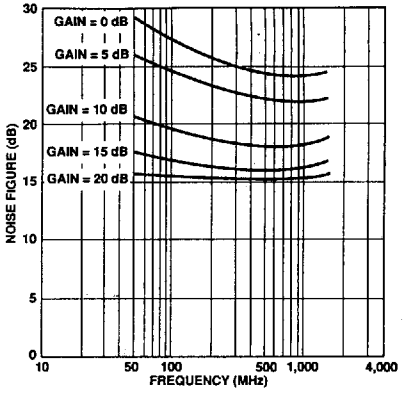


Figure 2. Typical Noise Figure vs. Frequency over Gain Control Range at 25° C

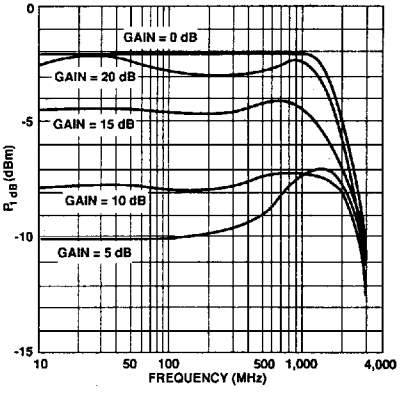


Figure 3. Typical $P_{1\ dB}$ vs. Frequency over Gain Control Range at 25° C

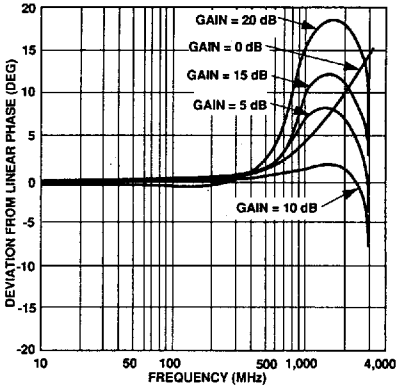


Figure 4. Typical Linear Phase vs. Frequency over Gain Control Range at 25° C

(continued)

HPVA-0180 Typical Parameters

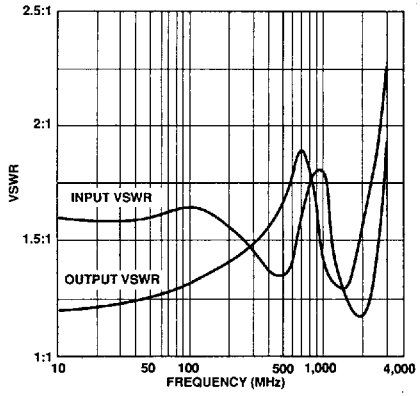


Figure 5. Typical Input and Output VSWR vs. Frequency Gain = 20 dB at 25° C

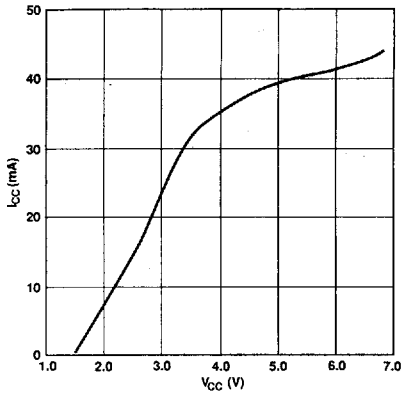


Figure 6. Typical I_{CC} vs. V_{CC} at 25°C

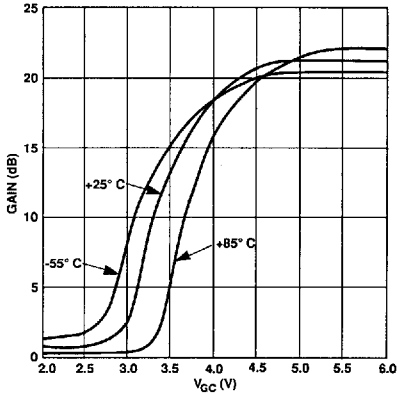


Figure 7. Typical Gain vs. V_{GC} at 300 MHz at Three Temperatures

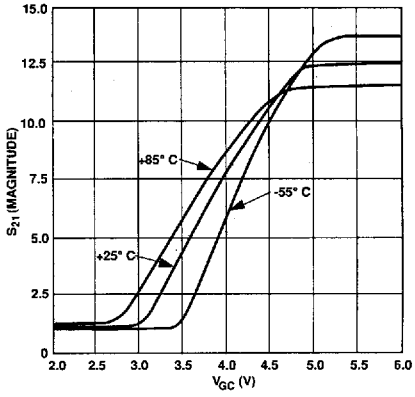


Figure 8. Typical S_{21} vs. V_{GC} at 300 MHz at Three Temperatures

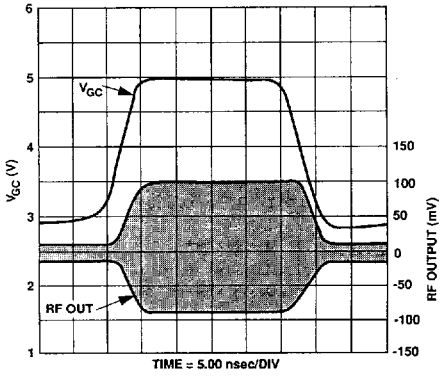


Figure 9. Typical Pulsed V_{GC} Response with RF Frequency of 100 MHz at 25°C

Theory of Operation

Figure 10 shows the simplified schematic for the HPVA-0180. The signal path is a cascade of an input buffer, a variable-gain stage, and an output buffer. The input buffer provides 50 Ω input impedance and proper bias voltage for the variable-gain stage. The variable-gain stage is the main amplifier, whose voltage gain can be adjusted by the gain-controlling voltage, V_{GC}. The output buffer has 50 Ohm output impedance and is designed to drive 50 Ohm loads. The HPVA-0180 also contains a V_{GC} translator and a band-gap voltage reference. The V_{GC} translator takes the external gain-controlling voltage, V_{GC}, and generates V_{GC1} and V_{GC2} to control the variable-gain stage. The V_{GC} translator also linearizes the HPVA-0180's gain with respect to V_{GC}. The band-gap voltage reference generates a bias voltage, V_{bias}, to drive all of the current sources in the circuit. The voltage V_{bias} is temperature compensated so that the output current of all of the current sources will remain stable over a wide temperature range.

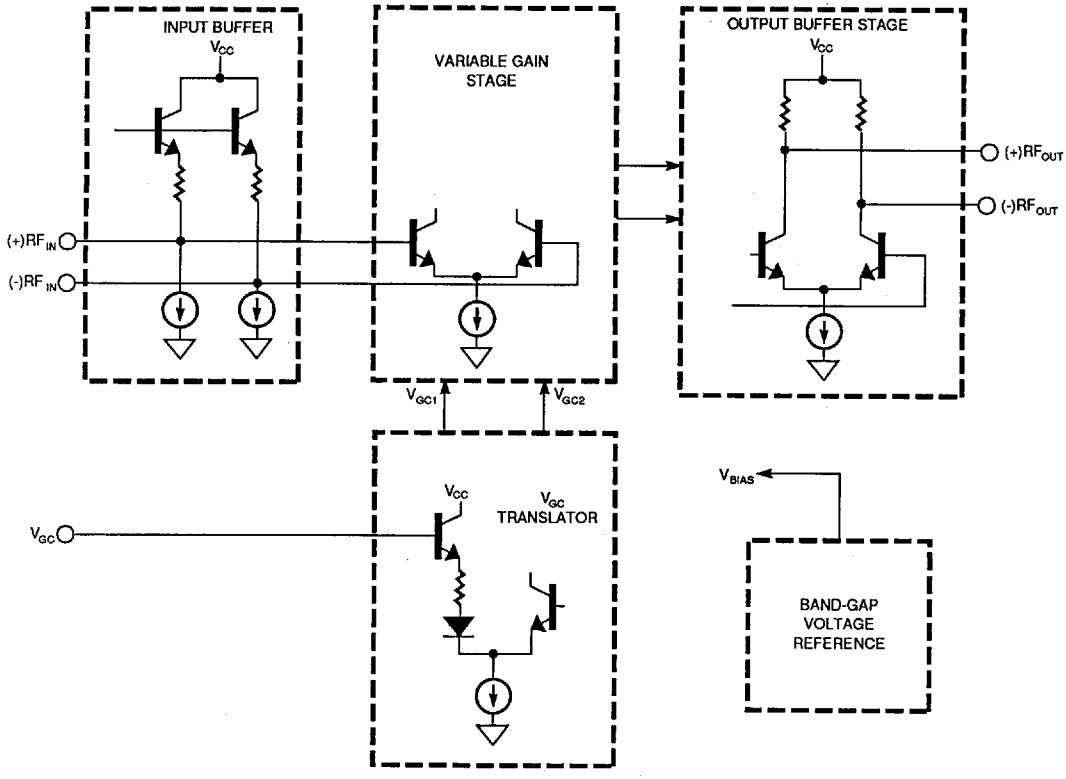
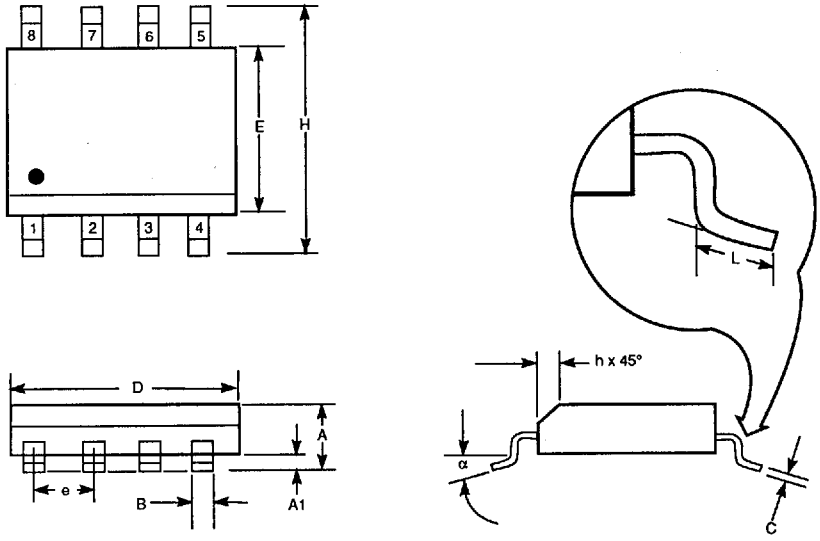


Figure 10. HPVA-0180 Simplified Schematic

Package Dimensions

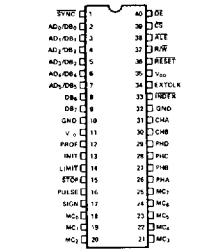
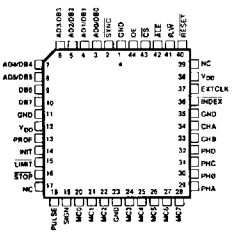
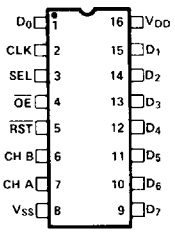
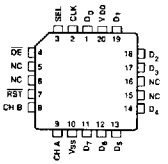
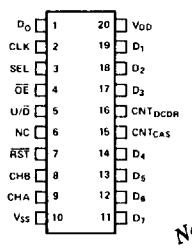
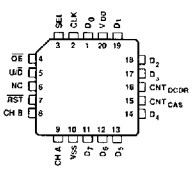
Plastic SO-8 Package



Symbol	Dimensions	
	Min.	Max.
A	1.35 (0.053)	1.75 (0.068)
A1	0.10 (0.004)	0.25 (0.0098)
B	0.35 (0.0138)	0.49 (0.0192)
C	0.19 (0.007)	0.25 (0.0098)
D	4.80 (0.189)	5.00 (0.197)
E	3.80 (0.150)	4.00 (0.157)
e	1.27 BSC (0.050)	
H	5.80 (0.228)	6.20 (0.244)
h	0.25 (0.010)	0.50 (0.020)
L	0.40 (0.016)	1.27 (0.050)
α	0°	8°

Meets JEDEC outline dimensions.
Dimensions are in millimeters (inches)

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	New HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	New HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61