HS-6664RH

Radiation Hardened 8K x 8 CMOS PROM

September 1995

Features

- 1.2 Micron Radiation Hardened Bulk CMOS
- Total Dose 3 x 10^5 RAD (Si)
- Transient Output Upset >5 x 10^8 RAD (Si)/s
- LET >100 MEV-cm^2/mg
- Fast Access Time - 35ns (Typical)
- Single 5V Power Supply
- Single Pulse 10V Field Programmable
- Synchronous Operation
- On-Chip Address Latches
- Three-State Outputs
- NiCr Fuses
- Low Standby Current <500μA (Pre-Rad)
- Low Operating Current <15mA/MHz
- Military Temperature Range -55°C to +125°C

Description

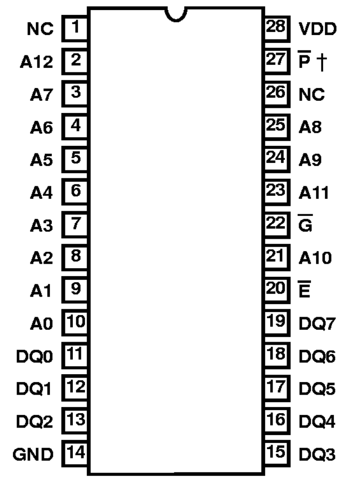
The Harris HS-6664RH is a radiation hardened 64K CMOS PROM, organized in an 8K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and utilizes synchronous circuit design techniques to achieve high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with microprocessors that use a multiplexed address/data bus structure. The output enable control ($\overline{G}$) simplifies system interfacing by allowing output data bus control in addition to the chip enable control ($\overline{E}$). All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

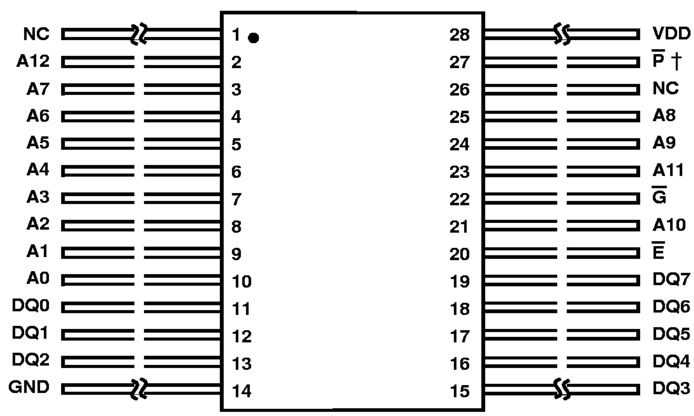
Applications for the HS-6664RH CMOS PROM include low power microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, and processor control storage.

Pinouts

28 LEAD CERAMIC SBDIP
CASE OUTLINE D28.6 MIL-STD-1835, CDIP2-T28
TOP VIEW



28 LEAD FLATPACK
CASE OUTLINE K28.A MIL-STD-1835, CDFP3-F28
TOP VIEW



† P must be hardwired at all times to VDD, except during programming.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 3197.3

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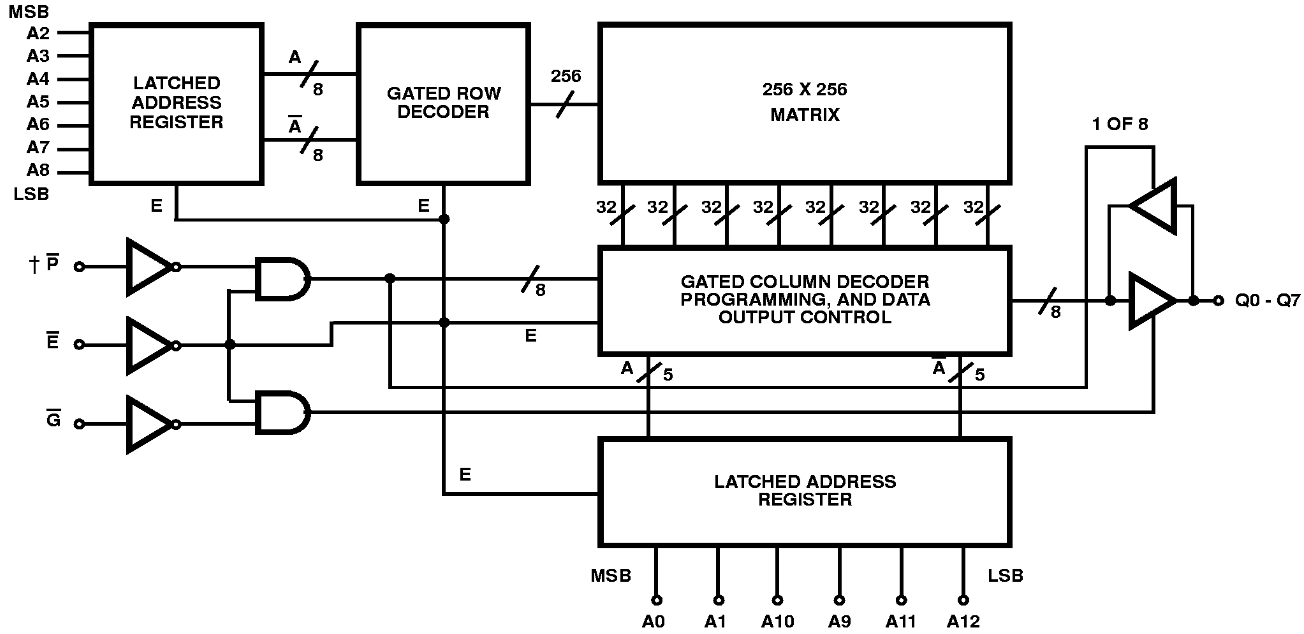
Functional Diagram



† P must be hardwired at all times to VDD, except during programming.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

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Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND) . . . . . +7.0V
Input or Output Voltage
Applied for All Grades . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . -65^oC to $+150^oC$
Junction Temperature . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . $+300^oC$
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance θ_{JA} θ_{JC}
Braze Seal DIP Package . . . . $40.0^oC/W$ $4.0^oC/W$
Braze Seal Flatpack Package . . . . $53.4^oC/W$ $6.0^oC/W$
Maximum Package Power Dissipation at $+125^oC$
Braze Seal DIP Package 1.75W
Braze Seal Flatpack Package 936mW
Gate Count . . . . 26,817 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . -55^oC to $+125^oC$
Input Low Voltage (VIL) . . . . 0V to +0.8V
Input High Voltage (VIH) . . . . +2.4V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -2.0mA	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	3.5	-	V
Output High Voltage	VOH2	VDD = 4.5V, IO = 100μA	3	$-55^oC \leq T_A \leq +125^oC$	VDD -0.3V	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 4.8mA	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VDD	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-10.0	10.0	μA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD, $\overline{P}$ Not Tested	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-1.0	1.0	μA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VI = VDD or GND	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	500	μA
Operating Supply Current	IDDOP	VDD = 5.5V, $\overline{G}$ = VDD, (Note 3), f = 1MHz, IO = 0mA, VI = VDD or GND	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	15	mA
Functional Test	FT	VDD = 4.5V (Note 4)	7, 8A, 8B	$-55^oC \leq T_A \leq +125^oC$	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. All tests performed with $\overline{P}$ hardwired to VDD.
3. Typical derating = 15mA/MHz increase in IDDOP.
4. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.45V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	20	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	60	ns
Address Setup Time	TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Address Hold Time	TELAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	12	-	ns

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Low Width	TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	60	-	ns
Chip Enable High Width	TEHEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Read Cycle Time	TELEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	80	-	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF.
3. All tests performed with $\overline{P}$ hardwired to VDD.
4. Address Access Time (TAVQV) = TELQV + TAVEL = 65ns (maximum).

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETER	SYMBOL	(NOTE 2) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 3	$T_A = +25^oC$	-	15	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	1, 3	$T_A = +25^oC$	-	12	pF
Chip Enable Time	TELQX	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable Time	TGLQX	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Disable Time	TEHQZ	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	-	15	ns
Output Disable Time	TGHQZ	VDD = 4.5V and 5.5V	3	$-55^oC \leq T_A \leq +125^oC$	-	15	ns

NOTES:

1. All measurements referenced to device GND.
2. All tests performed with $\overline{P}$ hardwired to VDD.
3. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after design or process changes which would affect these characteristics.

TABLE 4. POST 100K RAD AC AND DC ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: All AC and DC parameters are tested at the $+25^oC$ pre-irradiation limits.

TABLE 5. BURN-IN DELTA PARAMETERS ($+25^oC$)

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±50µA
Input Leakage Current	IOZ	±1µA
	II	±100nA
Output Low Voltage	VOL	±60mV
Output High Voltage	VOH	±400mV

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TABLE 6. APPLICABLE SUBGROUPS

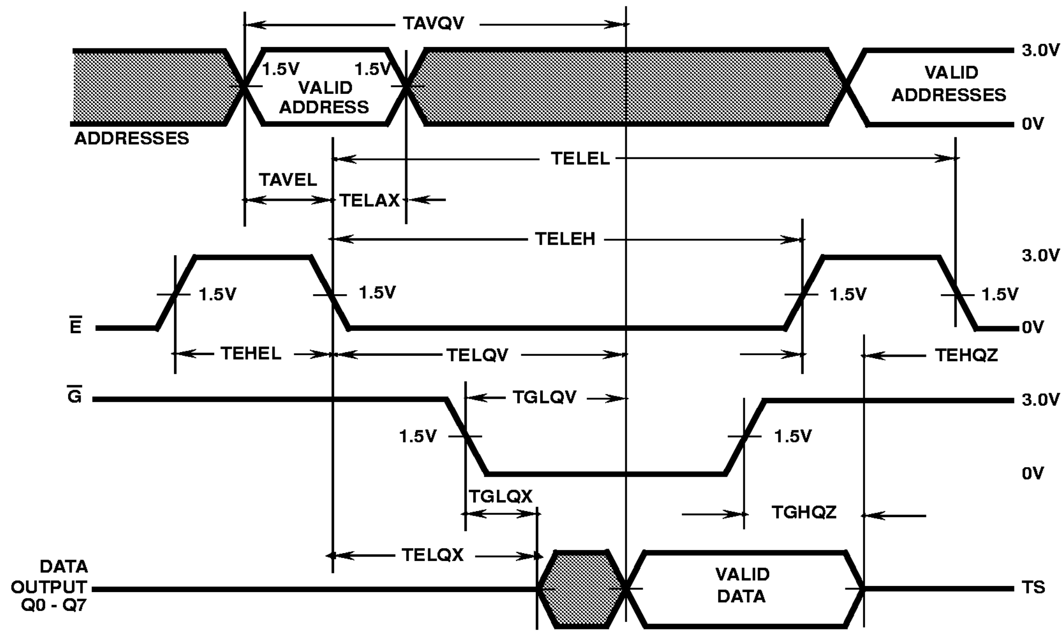
CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (*Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7,9	N/A
Group C (Optional)		Samples/5005	N/A	1, 7, 9
Group D (Optional)		Samples/5005	1, 7, 9	1, 7, 9
Group E, Subgroup 2 (Note 1)		Samples/5005	1, 7, 9	1, 7, 9

NOTE:

1. Harris may exercise its option to perform to a small lot sampling plan of 5 units per lot.

Timing Waveform

READ CYCLE



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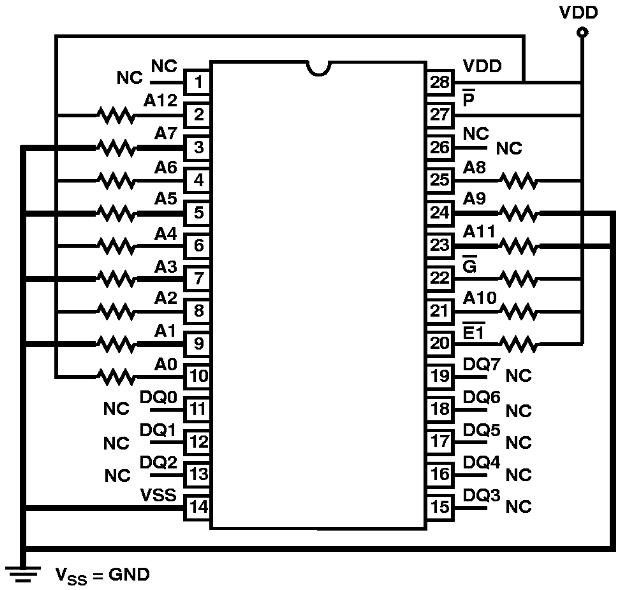
Burn-In Circuits

HS1-6664RH 28 LEAD (8K x 8 PROM DIP)
HS9-6664RH 28 LEAD (8K x 8 PROM FLATPACK)

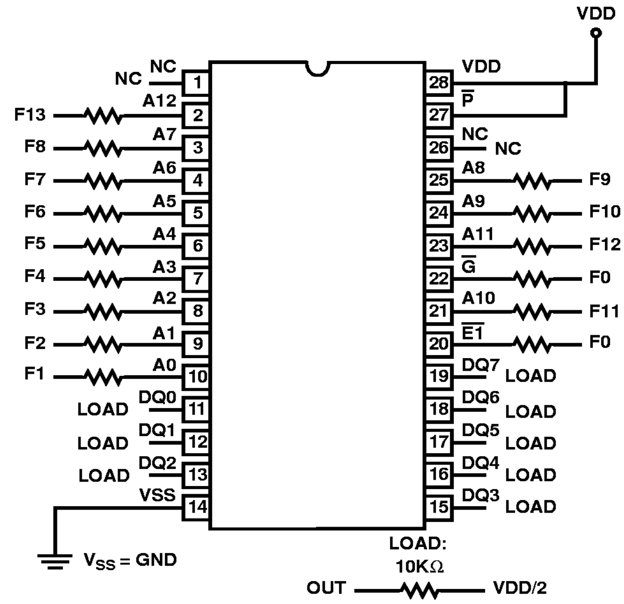


STATIC CONFIGURATION

NOTES:

1. Power Supply: VDD = 5.5V (Min)
2. Resistors = 10kΩ ± 10%

HS1-6664RH 28 LEAD (8K x 8 PROM DIP)
HS9-6664RH 28 LEAD (8K x 8 PROM FLATPACK)



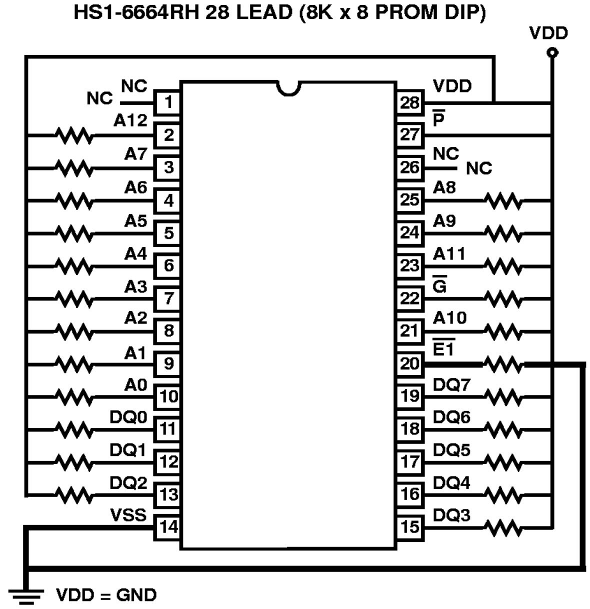
DYNAMIC CONFIGURATION

NOTES:

1. Power Supply: VDD = 5.5V (Min)
2. VIH = VDD to VDD-1.0V
3. VIL = 0.0V to 0.8V
4. Resistors = 10KΩ ± 10%
5. F0 = 100KHz ± 10%, 50% Duty Cycle
6. F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2; F5 = F4/2; . . . F13 = F12/2

Irradiation Circuit

HS1-6664RH 28 LEAD (8K x 8 PROM DIP)



NOTES:

1. Power Supply: VDD = 5.5V ±0.5V
2. All Resistors = 47KΩ ± 10%

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Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection Method 2010 Condition B Alternate
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group B Inspection Method 5005 (Notes 1, 2)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B, C and D data package contains Attributes Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

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Metallization Topology

DIE DIMENSIONS:
271 x 307 x 19 ±1mils

METALLIZATION:
M1: 6kÅ ±1kÅ Si/Al/Cu
2kÅ ±500Å TiW
M2: 10kÅ ± 2kÅSi/Al/Cu

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2

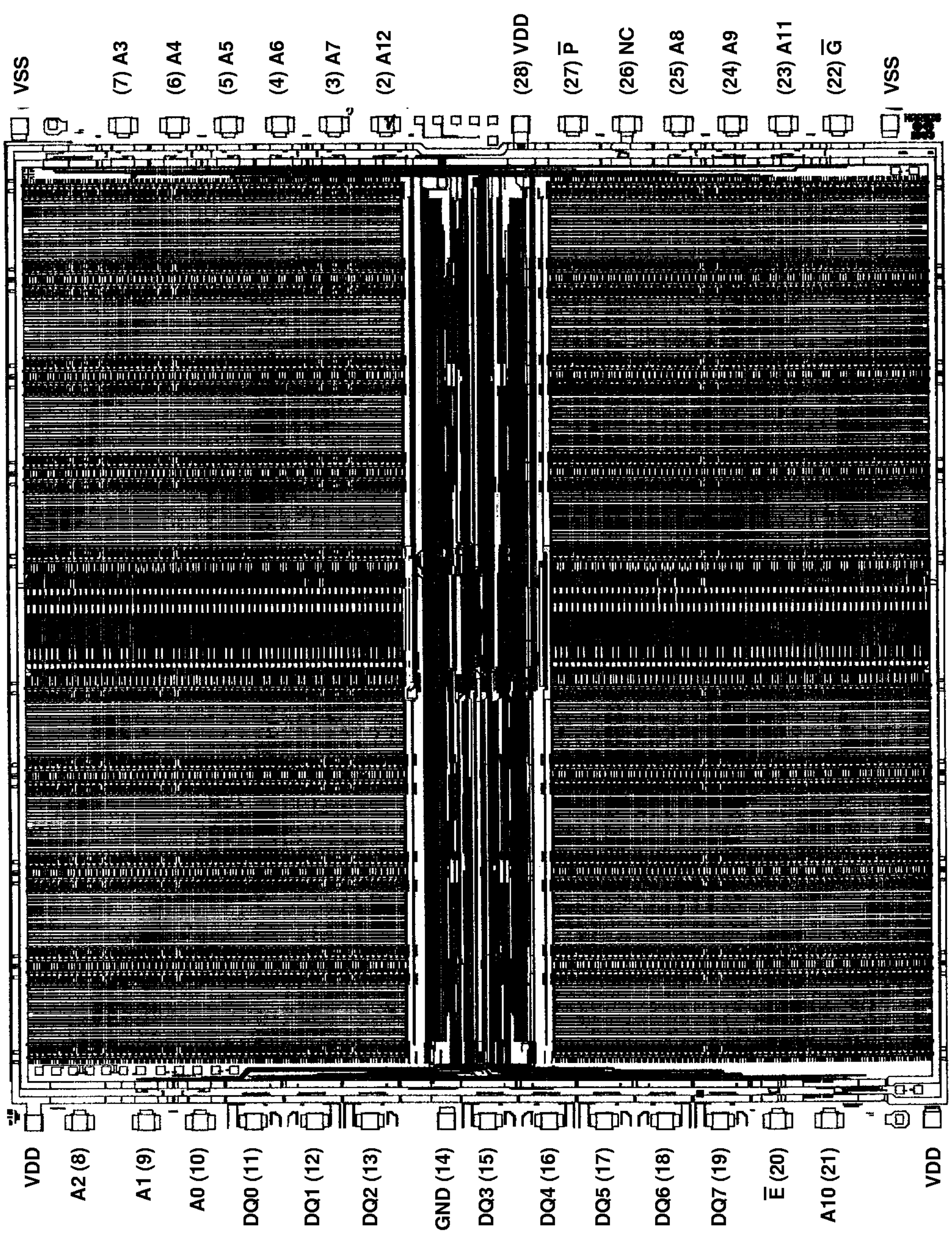
SUBSTRATE POTENTIAL: VDD

TRANSISTOR COUNT: 110, 874

GATE COUNT: 27, 719 (Based on 2-Input NAND)

Metallization Mask Layout

HS-6664RH



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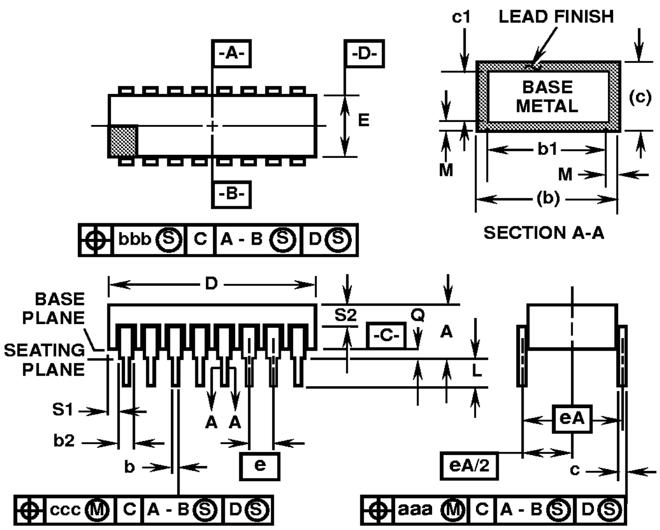
Packaging



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D28.6 **MIL-STD-1835 CDIP2-T28 (D-10, CONFIGURATION C)**
28 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

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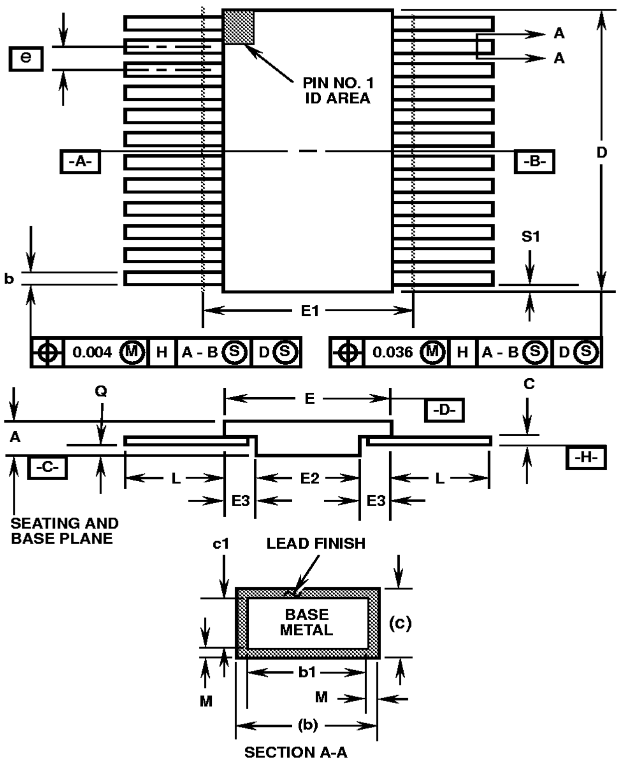
Packaging (Continued)



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B) 28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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HARRIS Semiconductor

HS-6664RH

DESIGN INFORMATION

September 1995

8K x 8 CMOS PROM

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Background Information HS-6664RH Programming

PROGRAMMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input "0"	VIL	0.0	0.2	0.8	V	
Voltage "1"	VIH	VDD-2	VDD	VDD+0.3	V	6
Programming VDD	VDDPROG	9.0	9.0	9.0	V	2
Operating VDD	VDD1	4.5	5.5	5.5	V	
Special Verify	VDD2	4.0	-	6.0	V	3
Delay Time	td	1.0	1.0	-	μs	
Rise Time	tr	1.0	10.0	10.0	μs	
Fall Time	tf	1.0	10.0	10.0	μs	
Chip Enable Pulse Width	TEHEL	20	-	-	ns	
Address Valid to Chip Enable Low Time	TAVEL	0	-	-	ns	
Chip Enable Low to Output Valid Time	TELQV	-	-	60	ns	
Programming Pulse Width	tpw	90	100	110	μs	4
Input Leakage at VDD = VDDPROG	tIP	-10	+1.0	10	μA	
Data Output Current at VDD = VDDPROG	IOP	-	-5.0	-10	mA	
Output Pull-Up Resistor	Rn	5	10	15	kΩ	5
Ambient Temperature	T_A	-	25	-	°C	

NOTES:

1. All inputs must track VDD (pin 28) within these limits.
2. VDDPROG must be capable of supplying 500mA. VDDPROG Power Supply tolerance ±3% (Max.)
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to VDD through a resistor of value Rn.
6. Except during programming (See Programming Cycle Waveforms).

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DESIGN INFORMATION (Continued)

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Background Information Programming

The HS-6664 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or use of an approved commercial programmer is recommended.

Programming Sequence of Events

1. Apply a voltage of VDD1 to VDD of the PROM.
2. Read all fuse locations to verify that the PROM is blank (output low).
3. Place the PROM in the initial state for programming: $\overline{E}$ = VIH, $\overline{P}$ = VIH, $\overline{G}$ = VIL.
4. Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5. After a delay of td, apply voltage of VIL to $\overline{E}$ (pin 20) to access the addressed word.
6. The address may be held through the cycle, but must be held valid at least for a time equal to td after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7. After a delay of td, disable the outputs by applying a voltage of VIH to $\overline{G}$ (pin 22).
8. After a delay of td, apply voltage of VIL to $\overline{P}$ (pin 27).
9. After delay of td, raise VDD (pin 28) to VDDPROG with a rise time of tr. All outputs at VIH should track VDD within VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resistors of value Rn.
10. After a delay of td, pull the output which corresponds to the bit to be programmed to VIL. Only one bit should be programmed at a time.
11. After a delay of tpw, allow the output to be pulled to VIH through pull-up resistor Rn.
12. After a delay of td, reduce VDD (pin 28) to VDD1 with a fall time of tf. All outputs at VIH should track VDD with VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resistors of value Rn.
13. Apply a voltage of VIH to $\overline{P}$ (pin 27).
14. After a delay of td, apply a voltage of VIL to $\overline{G}$ (pin 22).
15. After a delay of td, examine the outputs for correct data. If any location verifies incorrectly, it should be considered a programming reject.
16. Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

Post-Programming Verification

17. Place the PROM in the post-programming verification mode: $\overline{E}$ = VIH, $\overline{G}$ = VIL, $\overline{P}$ = VIH, VDD (pin 28) = VDD1.
18. Apply the correct binary address of the word to be verified to the PROM.
19. After a delay of td, apply a voltage of VIL to $\overline{E}$ (pin 20).
20. After a delay of td, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21. Repeat steps 17 through 20 for all possible programming locations.

Post-Programming Read

22. Apply a voltage of VDD2 = 4.0V to VDD (pin 28).
23. After a delay of td, apply a voltage of VIH to $\overline{E}$ (pin 20).
24. Apply the correct binary address of the word to be read.
25. After a delay of TAVEL, apply a voltage of VIL to $\overline{E}$ (pin 20).
26. After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27. Repeat steps 23 through 26 for all address locations.
28. Apply a voltage of VDD2 = 6.0V to VDD (pin 28).
29. Repeat steps 23 through 26 for all address locations.

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DESIGN INFORMATION (Continued)

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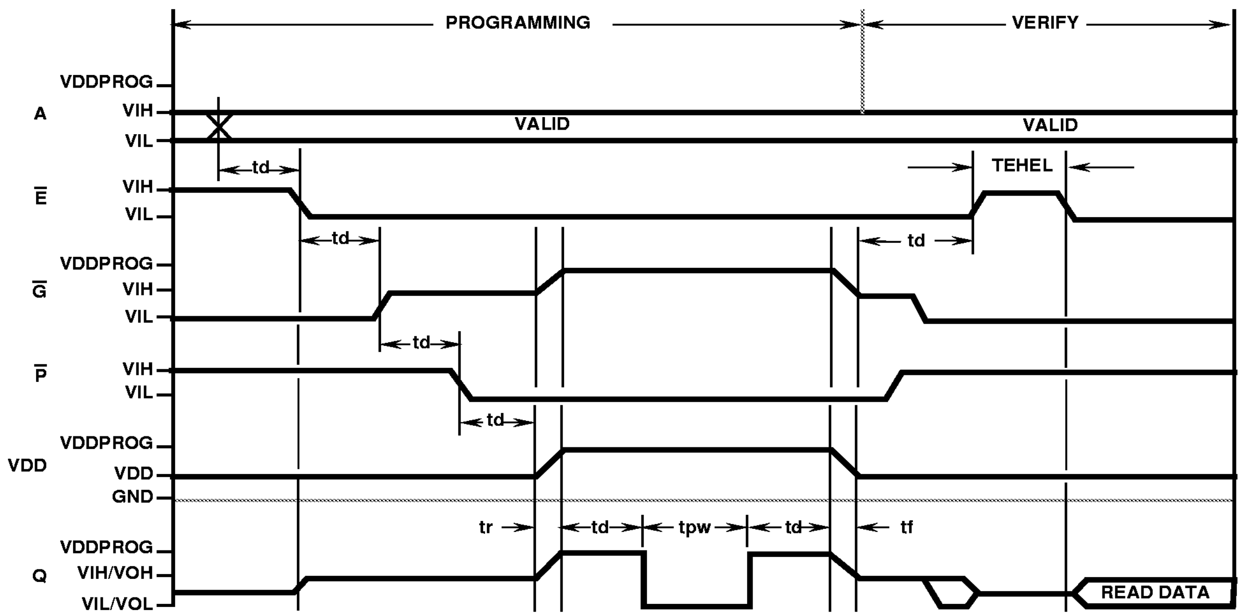
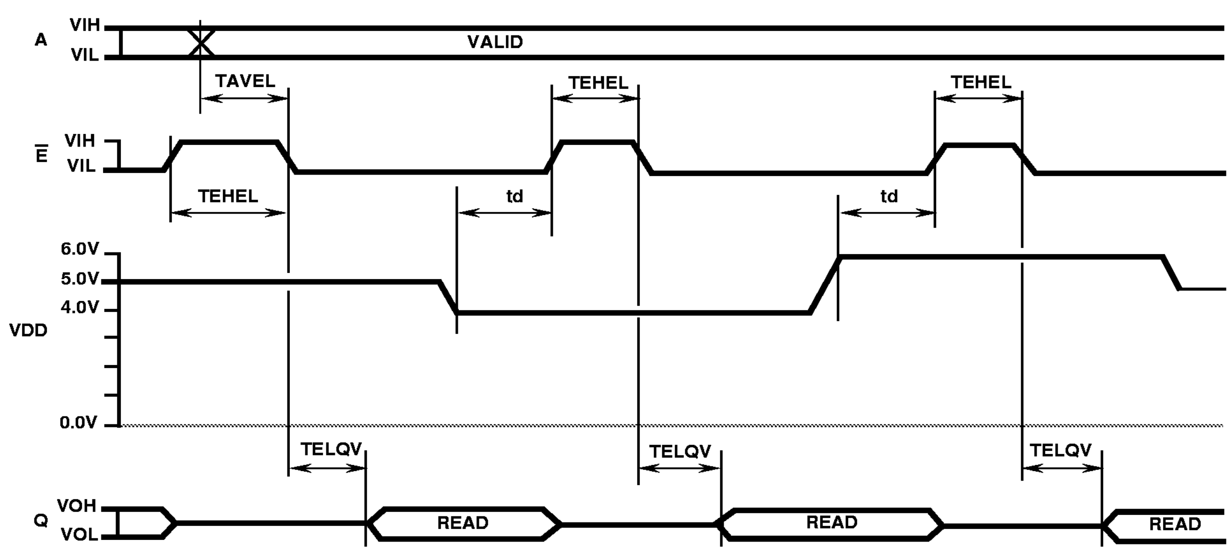
HS-6664RH PROGRAMMING CYCLE



HS-6664RH POST PROGRAMMING VERIFY CYCLE



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