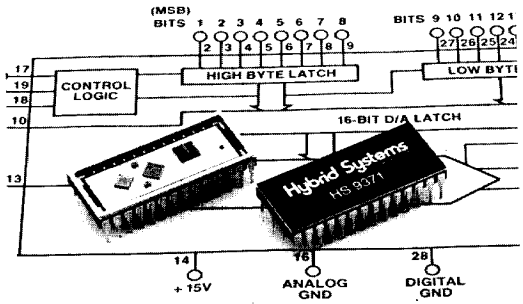
μP COMPATIBLE, CURRENT OUTPUT, 16-BIT MDAC

FEATURES

- Monotonic to 16-bits over the military and commercial temperature ranges
- Low power consumption, 45 mW max.
- Double buffered input
- Proprietary semicustom gate array signficantly reduces digital feedthrough
- Pinout permits 16 digital input lines to be connected to an 8-bit data bus without crossing bus lines



DESCRIPTION

The HS9371 is a current output, 16-bit multiplying D/A converter with 16-bit monotonicity guaranteed over the commercial and military temperature ranges. Complete with dual storage registers, the HS9371 Series easily interfaces with either 8-bit or 16-bit bus structures, eliminating the need for external latches.

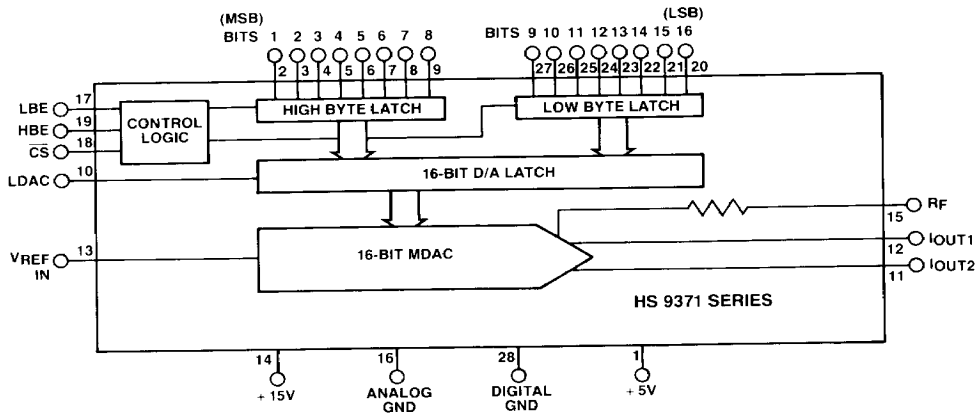
A proprietary semicustom gate array is used to significantly reduce digital feedthrough while internal decoupling capacitors reduce the effect of power supply perturbations.

The HS9371 has dual 8-bit input registers for direct interface to 8- or 16-bit bus structures. The pinout of the HS9371 allows the user with an 8-bit bus to run only 8 traces directly underneath the hybrid to connect to the 16-bit input register.

The HS9371 is available for either commercial (+0°C to +70°C) or military (−55°C to +125°C) applications. Screening to MIL-STD-883C is available.

7

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C unless otherwise specified)

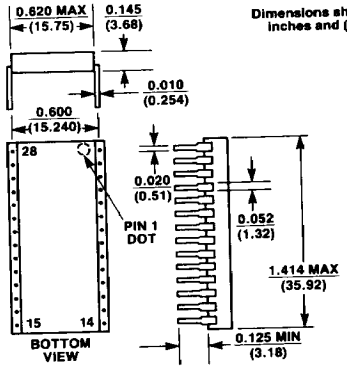
MODEL	HS 9371K	HS 9371J	HS 9371TB	HS 9371SB
DIGITAL INPUT				
Resolution	16-bits	*	*	*
Coding	Straight/Offset Binary	*	*	*
Logic Compatibility	TTL, LSTTL, CMOS			
V_{IL} (max)[5]	0.8V	*	*	*
V_{IH} (min)[5]	2.4V	*	*	*
Input Current	10 μ A max	*	*	*
Latch Control Minimum Pulse Width	100 nsec	*	*	*
Data Set-Up Time	100 nsec min[1]	*	*	*
Data Hold Time	0 nsec	*	*	*
ANALOG OUTPUT				
Gain Accuracy	±0.1% F.S.R. typ, ±0.2% max[2]	*	*	*
Initial Offset Error	±0.0005% max[2]	*	*	*
Current Range				
Unipolar	0 to +2 mA	*	*	*
Bipolar	±1 mA	*	*	*
Noise				
p-p noise (0.1 Hz to 100 Hz)	50 μ V	*	*	*
Output Capacitance	80 pF	*	*	*
REFERENCE INPUT				
Input Impedance	5K Ω	*	*	*
STATIC PERFORMANCE				
Integral Linearity Error[3]	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Differential Linearity Error[4]	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Monotonicity Guaranteed to:	16-bits	15-bits	16-bits	15-bits
DYNAMIC PERFORMANCE				
Major Carry Transition Settling to 0.0015% F.S.R.	1 μ sec[6]	*	*	*
Full Scale Transition Settling to 0.0015% F.S.R.	5 μ sec[6]	*	*	*
Reference Feedthrough Attenuation[8]	100 dB @ 100 Hz sine wave	*	*	*
	80 dB @ 1 kHz sine wave	*	*	*
Glitch Energy[8]	3 nV-sec	*	*	*
STABILITY				
Gain Drift	6 ppm/°C max	*	*	*
Offset Drift				
Unipolar	1 ppm/°C max	*	*	*
Bipolar	2 ppm/°C max	*	*	*
Linearity Drift	1 ppm/°C max	*	*	*
POWER SUPPLY				
Current		V_{LOGIC}, all bit inputs		
	0 or +5V		+2.5V	
+15V supply	1 mA typ, 3 mA max		1 mA typ, 3 mA max	
+5V supply	0.1 μ A typ, 1 μ A max		12 mA typ, 20 mA max	
Power Dissipation[7]	45 mW max, V_{LOGIC} = 0 or +5V, all bit inputs 150 mW max, V_{LOGIC} = +2.5V, all bit inputs			
Rejection Ratio	±0.0006% FS/% typ ±0.002% FS/% max	*	*	*
TEMPERATURE RANGE				
Operating	0°C to +70°C	0°C to +70°C	−55°C to +125°C	−55°C to +125°C
Storage	−25°C to +85°C	−25°C to +85°C	−65°C to +150°C	−65°C to +150°C
PACKAGE				
28-pin, double DIP				

NOTES:

1. −55°C to +125°C
2. Adjustable to zero.
3. Integral Linearity is measured per best straight line method.
4. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
5. Voltages at the digital inputs may not go below 0 volts or exceed +5V.
6. 50 Ω load.
7. To minimize power consumption, add 2KΩ pull-up resistors to the digital inputs when driving with TTL.
8. Lid of Case should be grounded to analog ground for optimum performance.

*Specifications same as 9371K

PACKAGE OUTLINE



PIN ASSIGNMENTS

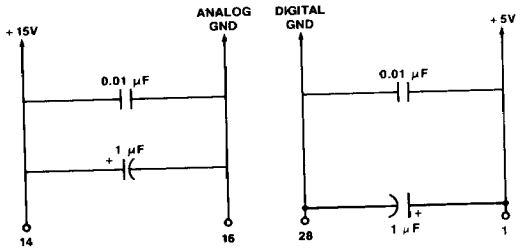
PIN	FUNCTION	PIN	FUNCTION
1	+5V	28	DIGITAL GND
2	BIT 1 (MSB)	27	BIT 9
3	BIT 2	26	BIT 10
4	BIT 3	25	BIT 11
5	BIT 4	24	BIT 12
6	BIT 5	23	BIT 13
7	BIT 6	22	BIT 14
8	BIT 7	21	BIT 15
9	BIT 8	20	BIT 16
10	LDAC	19	HBE
11	I_{OUT2}	18	$\overline{CS}$
12	I_{OUT1}	17	LBE
13	V_{REF}	16	ANALOG GND
14	+15V	15	R_F

ABSOLUTE MAXIMUM RATINGS (HS 9371)

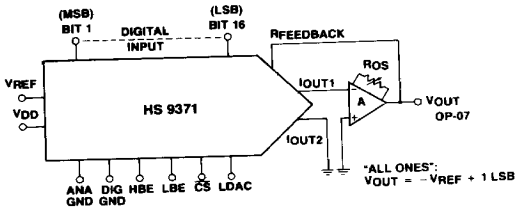
+15V Supply (+V_{DD}) to Analog GND	+17V
+5V Supply (+V_{CC}) to Digital GND	+7V
Analog GND to Digital GND	±0.5V
Digital Input Voltage to Digital GND	+V_{CC} + 0.3V max Digital GND −0.3V min
$V_{REF\,IN}$ to Analog GND	±25V
Output Voltage (Pins 11, 12)	Analog GND ±0.1V
Power Dissipation of Package (Case A) (Case B)	 1.4W @ +85°C 1.5W @ +125°C
Lead Temperature, Soldering (Case A) (Case B)	 300°C, 5 sec 300°C, 10 sec

APPLICATION INFORMATION

RECOMMENDED BYPASS CIRCUIT

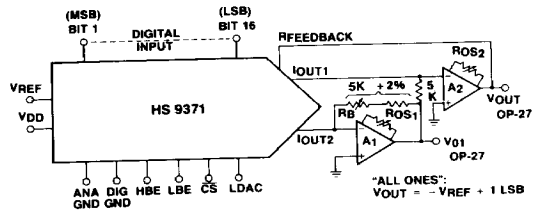


UNIPOLAR OPERATION *(2-Quadrant Multiplication)*



NOTE: To maintain specified HS 9371 linearity, the external amplifier (A) must be zeroed. Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ± 1 mV.

BIPOLAR OPERATION *(4-Quadrant Multiplication)*



NOTE: To maintain specified HS 9371 linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10...0 and V_{REF} set to zero:
a) Set R_{OS1} for V_{01} = 0 ± 1 mV
b) Set R_{OS2} for V_{OUT} = 0 ± 1 mV
c) Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0 volts.

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. −1 LSB
100...000	+F.S./2
011...111	+F.S./2 −1 LSB
000...000	0V

BIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. −1 LSB
100...000	0V
011...111	−1 LSB
000...000	−F.S.

MICROPROCESSOR INTERFACE CONSIDERATIONS

General

The HS 9371 is easily interfaced to either an 8-bit or 16-bit microprocessor. First, a signal to select (or address) the HS 9371 must be generated. Then the input data must be written (or latched) to the DAC and after settling, the analog output is valid.

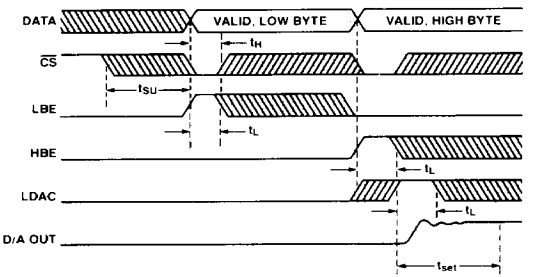
The bus interface logic consists of three independently addressable registers in two buffers. The first buffer consists of two 8-bit registers which can be loaded directly from an 8- or 16-bit microprocessor bus. Once the complete 16-bit word has been assembled in the first buffer, it can be loaded into the second buffer for conversion.

The required selection signal, $\overline{CS}$, is easily derived in most systems. Usually a base address is decoded and this active low signal is used for $\overline{CS}$. The active high signal for the low byte enable (LBE) and high byte enable (HBE) loads the two 8-bit registers into the first buffer while the LDAC signal loads the second buffer for conversion. The double-buffered input eliminates the generation of spurious analog output values.

MEMORY MAPPED INTERFACE TO 8-BIT μP

Figure 1 shows the timing sequence for operating the HS 9371 with an 8-bit μP bus and Figure 2 shows a general interface. Note that the pinout of the HS 9371 allows the user to run only 8 traces directly underneath the hybrid to connect to the two 8-bit input registers in the first buffer.

The HS 9371 is addressed by the chip select ($\overline{CS}$) signal going low for a minimum of 100 nsec. Since t_{SU}, the minimum time required for the input data to be valid before $\overline{CS}$, LBE, or HBE are active, is 0 ns minimum, the $\overline{CS}$ signal can go low simultaneously with data. The low byte enable (LBE) signal going high loads the 8 LSBs into the lower register of the first buffer. After a minimum latch time of 100 nsec, the LBE signal going low latches the data in the lower register. A similar control signal and timing sequence is used to load the 8 MSBs into the upper register of the first buffer (HBE). The load DAC (LDAC) signal going high loads the full 16-bits of data from the first buffer into the second buffer and the D/A for conversion. A minimum latch time of 100 nsec is required for the LDAC signal. The analog output then changes to the new value within the specified settling time. Table 1 is a truth table for the control inputs.



t_{SU}	Setup time required for input data to be valid before $\overline{CS}$, LBE or HBE going active	0 nsec min
t_H	Hold time for $\overline{CS}$ to stay low	100 nsec min
t_L	Latch time for LBE, HBE, and LDAC	100 nsec min
t_{SET}	Settling time from LDAC going active to valid output	
	– 0.0015% F.S.R., all zeros to all ones	5 μ sec typ
	– 0.0015% F.S.R., midscale LSB transition	1 μ sec typ

Figure 1. Timing Diagram for Interface to 8-Bit μP Bus

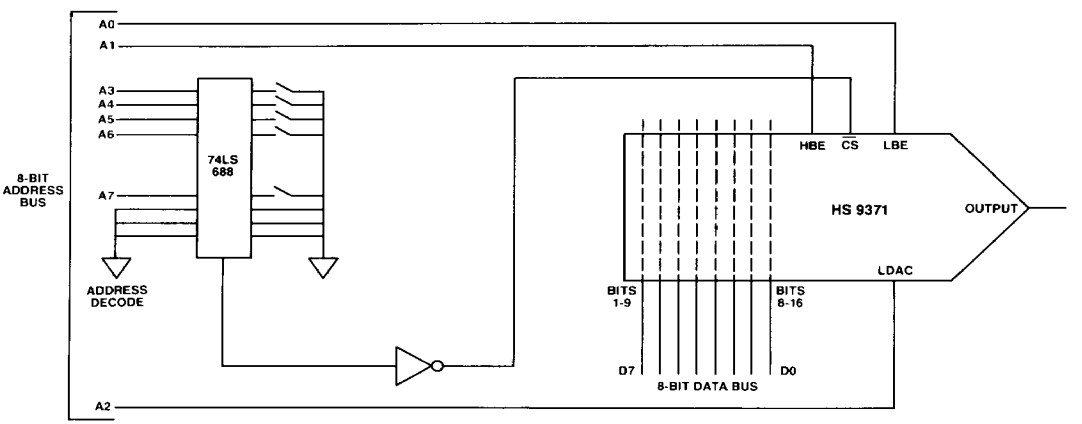


Figure 2. Block Diagram of HS 9371 Interfaced to 8-Bit μP

A_7-A_3 ($\overline{CS}$)	A_2 (LDAC)	A_1 (HBE)	A_0 (LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9371 is addressed	0	0	0	All data latched
	0	0	1	Data into low byte of 1st buffer, all others latched
	0	1	0	Data into high byte of 1st buffer, all others latched
	0	1	1	Invalid address
	1	0	0	Data into 2nd buffer (16 bits) and D/A, 1st buffer latched
	1	0	1	Invalid address
	1	1	0	Invalid address
	1	1	1	Data directly to D/A from bus, latches transparent

Table 1. Truth Table — Control Inputs (References Figure 2)

MEMORY MAPPED INTERFACE TO 16-BIT μP

Figure 3 shows the timing sequence for operating the HS 9371 with a 16-bit μP bus and Figure 4 shows a general interface. Table 2 is a truth table for the control inputs. Note that the control inputs are simplified since the HBE and LBE signals can be connected together.

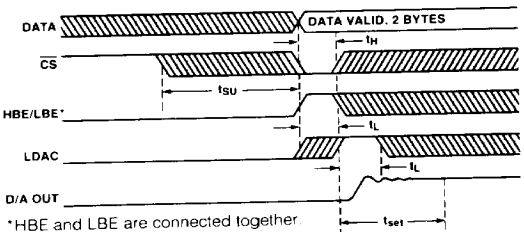


Figure 3. Timing Diagram for Interface to 16-Bit μP Bus

A_{15}-A_2 ($\overline{CS}$)	A_1 (LDAC)	A_0 (HBE, LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9371 is addressed	0	0	Data latched
	0	1	Data into 1st buffer, 2nd buffer latched
	1	0	Data into 2nd buffer, 1st buffer latched
	1	1	Data directly to D/A, latches transparent

Table 2. Truth Table — Control Inputs (References Figure 4)

POWER SUPPLY CONSIDERATIONS

Power supplies used for the HS 9371 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output voltage may result with noisy power sources. It is important to remember that 0.03 μA is 1 LSB for a 2 mA output. This translates to 156 μV for a 10 volt output range when converting to voltage.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.01 μF disc ceramic type.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, HS 9371 should be allowed sufficient warmup time (5 min.).
2. Due to the small bit weight (0.03 μA), noise becomes a noticeable factor; therefore, high quality sockets are recommended (if sockets are used) to minimize contact resistance.
3. No digital input should be left floating as the unit will draw excessive current. Unused digital inputs must be tied to a voltage potential between 0V and +5V.

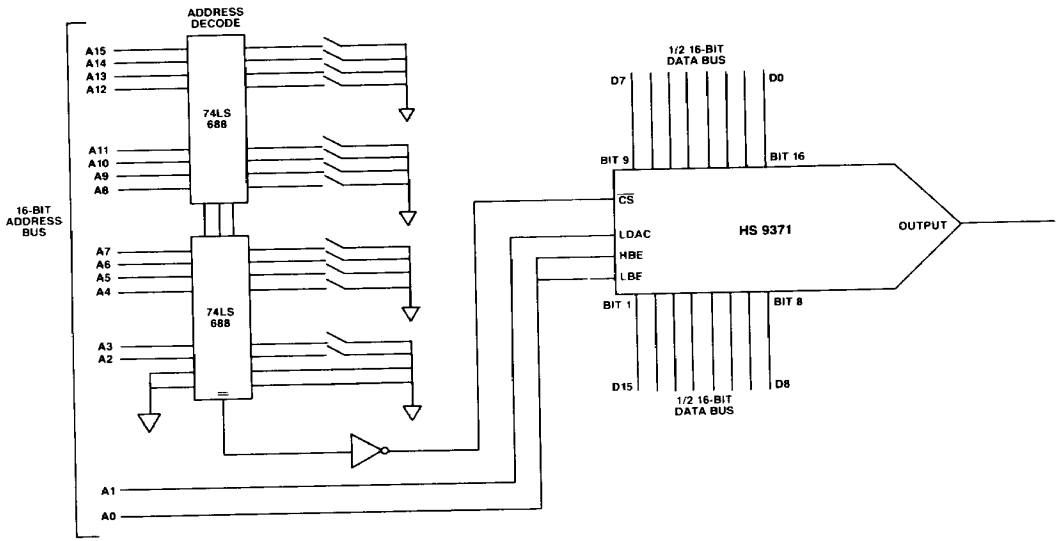


Figure 4. Block Diagram of HS 9371 Interfaced to 16-Bit μP

4. If optimum transient and glitch energy performance are required, electrically connect the lid (Case B) to pin 16.

5. If the D/A is driven from a non-buffered or heavily loaded bus, best linearity is obtained by adding 2KΩ pullups to the digital bit inputs.

CONTROL LOGIC

Figure 5 details the control logic function. Note that the LDAC signal is independent of the $\overline{CS}$ signal. All the latches are level controlled as opposed to edge triggered. This allows each of the latches to be operated in a transparent mode by tying the latch control input to a fixed logic "1" level. Since all 3 latches are independent of one another, the sequence of loading the 8 MSBs and the 8 LSBs is reversible.

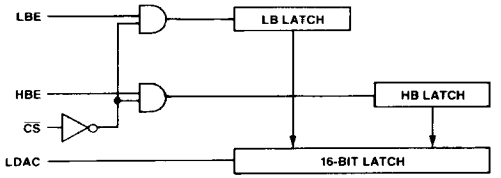


Figure 5. Control Logic Function

LAYOUT CONSIDERATIONS

Due to the small bit weight (0.03 μA for 1 LSB) special attention must be paid to the layout of the PC-board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground-plane can be directly connected to pin 16 of the HS 9371. All digital lines should run on the soldering side of the PC-board.

The pin assignment of the HS 9371 has been arranged so that the 16 digital inputs can be connected to an 8-bit data bus without crossing of bus lines (see Figure 2).

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package.

TERMINOLOGY

Major Carry Transition Settling: The total elapsed time between the application of a new input code and the point at which the analog output has settled to within a specified error band. The HS 9371 specifies settling to within 0.0015% FSR. For a major carry transition, the change is when the digital input goes from a "0" and all "1's" to a "1" and all "0's" or vice versa.

Full Scale Transition Settling: The same as major carry transition settling with the exception that the change is a full scale change. For the HS 9371, the change is from I_{OUT1} = 0 to I_{OUT1} = 2 mA or vice versa.

Monotonicity: A monotonic DAC means that the analog output does not decrease as the input is increased or vice versa. The relevant specification is over what temperature range and to what accuracy monotonicity is guaranteed.

A PRECISION SENSE-AND-CONTROL ROBOTICS SYSTEM

A counting A/D converter can be configured as a sense-and-control servo system for robotics applications. Figure 6 illustrates a bus-interfaced system which can:

1. Use the precision 16-Bit accurate HS 9371 as a D/A to provide a control voltage to a positioning device such as a motor or a speed controller such as a voltage to frequency converter.
2. Provide a tracking A/D function which allows a digital readout of position information.
3. Provide an infinite duration no-droop hold function for V_{SENSE}, under microprocessor control.

As shown, the system can traverse its entire output range of 0 to − 10V at approximately 10 Hz, which covers the entire 65,536 digital input (output) codes. This allows 1.5 μs for each successive count, or a clock rate to CCK of 667 kHz.

CIRCUIT OPERATION

A standard counting type A/D converter compares the output of a D/A converter to an external input signal and causes an N bit counter to move the N bit D/A inputs such that the D/A output converges to the external input signal. When the two signals are equal, the counter counts up and down on each successive clock, with the D/A output dithering on either side of the input by 1 LSB weight or less. The counter outputs are then a binary representation of the input (sense) voltage and the output (control) voltage.

This circuit has modified and expanded upon the basic configuration to provide a useable voltage output from the D/A (rather than the current output) and allow an easily scaled input voltage while being able to distinguish 16-Bit voltage difference levels (156 μV) at a 10V signal range).

ANALOG INS AND OUTS

The D/A-counter-comparator loop has been described. The HS OP-27 is used to convert the D/A output current to a 0 to − 10V signal. A comparator preamp is necessary at the 16-Bit level to ensure an adequate overdrive to a monolithic comparator because the response time of existing monolithic devices is inadequate for a 1.5 μs loop time. (Remember that all parts of the servo loop must settle to a 16-Bit level during each clock cycle; luckily the system moves by 1 LSB each cycle, so the voltage excursion is small.) A CA3127 monolithic transistor array is used for the differential pair and the output buffer devices.

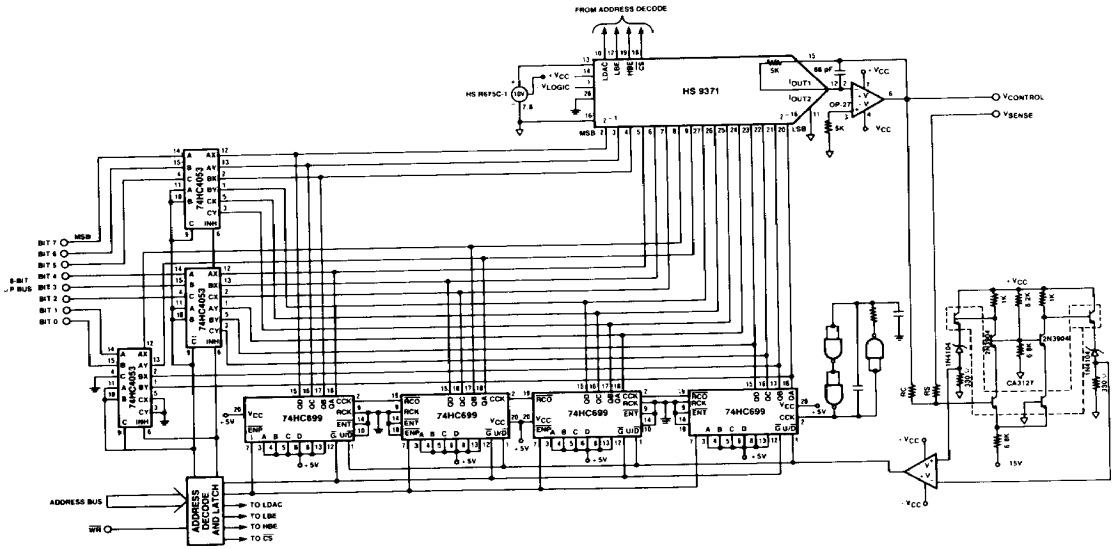


Figure 6. Bus Programmable Sense and Control Servo Loop for Precision Robotics Applications

The 1N4104 zener diodes provide a level shift of the preamp output to 3.3V to keep the signals within the common mode range of ±5V comparators such as the LT1016 and the LM360. The 2N3904 cascode devices may not be necessary in lower speed systems; a comparator such as the LM 319 or LM311 may also be used in less critical applications. The 1K gain setting resistors may be adjusted to trim offset voltage if the comparator has no such trim. The preamp is configured for a gain of 40, yielding an LSB output weight of (153 μV)*(40) = 6.1 mV to the comparator input.

Resistors RC and RS are used to compare $V_{CONTROL}$ and V_{SENSE}. With a positive 10V reference to the D/A converter (an HS R675C-1 is used for low noise and good transient response), a −10V full scale output is generated for $V_{CONTROL}$. This allows a 0V to positive V for V_{SENSE}, where

$$\frac{\max V_{CONTROL}}{RC} = \frac{\max V_{SENSE}}{RS}$$

is the constraint so that the input and output ranges match. If a 0V to negative V range is required, a negative reference such as the HS R675-3 can be used. A multiplexer (2:1 analog mux with low Ron) can be used to switch between negative and positive references at the V_{SENSE} zero crossing if a bipolar range is required.

DIGITAL UPS AND DOWNS

The comparator output must be a TTL or CMOS compatible signal which drives the UP/DOWN inputs of the counters. The four 4-Bit synchronous counters are cascaded to yield 16 binary outputs. Cascading results in a maximum rollover delay (for "HC" logic) of about 60-80 ns, which is small compared to the 1.5 μs minimum clock period. The $\overline{ENP}$ enable input is used to stop the count sequence for the "hold" function, while gate input $\overline{G}$ makes the outputs high impedance to allow the bus to load the D/A directly. If the system goes to the low or high end of the scale, the counter will roll over to the other end. If this is a problem (a linear versus rotary system), the ripple carry out $\overline{RCO}$ of the most significant counter can be exclusively NORed (XNOR) with the comparator output to cause the counter to toggle between its endpoint and 1 LSB away from the endpoint.

The bus interface uses 74HC4053s as a bidirectional 2:1 multiplexer with tri-state capability. The bus can load data into the D/A to force a specific control voltage. The bus interface in the HS 9371 can latch this data and act as a direct open-loop controller from the data bus with $\overline{ENP}$ high. If $\overline{ENP}$ is low, the 74HC4053s can be used to read the digital signal on the counter outputs in two 8-Bit bytes with the system in "track" mode. (If a two-byte read takes longer than one clock cycle, the tracking operation should be halted during READ to prevent erroneous data from being read.) To disconnect the bus from the servo system, make INH low. If both the counter and the bus can be tri-state, use pullup or pulldown resistors on the D/A inputs to prevent them from floating.

The address decode logic will be different for different processors and systems. It must be tailored to mate the address with the proper output signal polarity needed to drive the D/A interface signals and counter logic.

FINAL FEEDBACK

As with any highly sensitive analog circuit, care must be taken with circuit layout, power supply decoupling and ground paths. Keep clock signals away from analog signals, use analog ground plane underneath sensitive areas (especially the preamp and comparator) and minimize capacitive coupling between the comparator output and inputs. This coupling can cause oscillation which will preclude circuit operation. To prevent a linearity error due to ground resistance, route I_{OUT2} of the HS 9371 to the main analog ground via a separate trace from other low-level grounds. Connect analog and digital grounds at only one point, preferably near the D/A. Keep connections from the D/A to the preamp and comparator as short as possible. Follow decoupling procedures as described elsewhere in this data sheet.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for techincal assistance.

LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200 V for the first 1000 hrs; and 100 V per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

ORDERING INFORMATION

MODEL	MONOTONICITY (over temp.)	TEMPERATURE RANGE	SCREENING
HS 9371K	16 bits min	0°C to +70°C	—
HS 9371J	15 bits min	0°C to +70°C	—
HS 9371TB	16 bits min	−55°C to +125°C	MIL-STD-883C
HS 9371SB	15 bits min	−55°C to +125°C	MIL-STD-883C

Specifications subject to change without notice.