Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9476

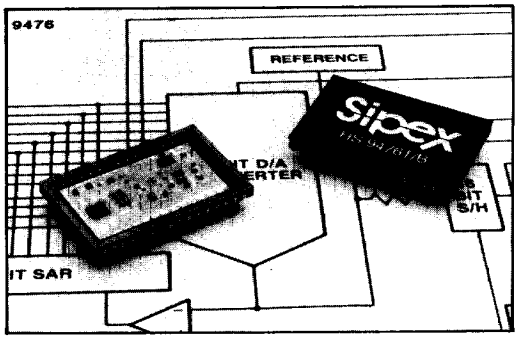
16-BIT SAMPLING A/D CONVERTER

FEATURES

- 16-bit ADC with internal 16-bit sample and hold amplifier
- 50kHz system throughput
- Pin for pin compatible with HS9576, BB ADC 76, AD 376

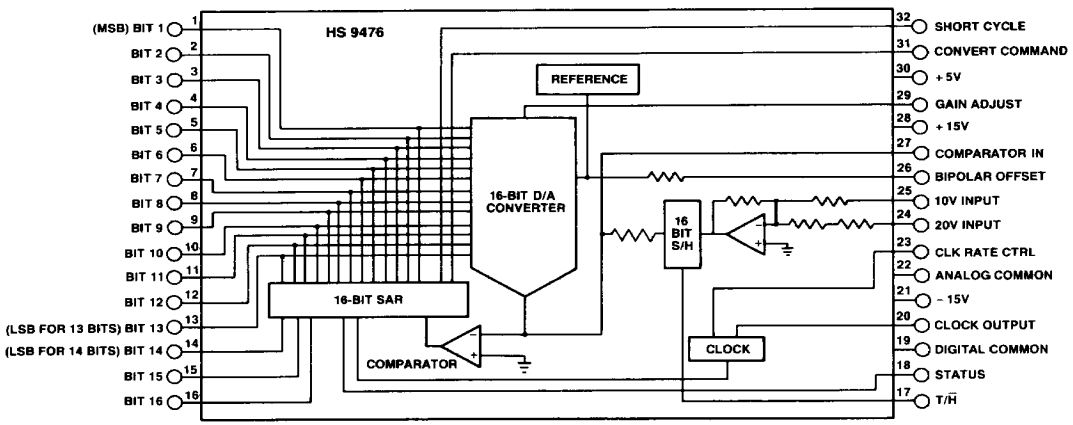
DESCRIPTION

Combining a 16-bit ADC and sample and hold amplifier (S/H) in a single 32 pin DIP, the HS9476 is a high accuracy sampling ADC capable of throughput rates up to 50kHz. Based on the HS9716, 16-bit 4μsec S/H and HS9576 16-bit 15μsec ADC the HS9476 is a pin compatible upgrade for the industry standard ADC 76/376 pin out. The S/H section has been specifically designed to match the requirements of the ADC for optimal performance. By integrating the S/H into the same package as the ADC, designers can avoid poor performance due to ground loops, signal coupling, and digital noise introduced when separate S/H and A/D converters are interconnected.



The HS9476 allows analog input ranges of ±5V, ±10V, 0 to +10V, and 0 to +20V. Integral nonlinearity is specified at ±0.003% of FSR maximum, while no missing codes is guaranteed for the full operating temperature range. The HS9476 is available for operation over the commercial (0°C to 70°C) temperature range or −55°C to +125°C with full MIL-STD-883C screening.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

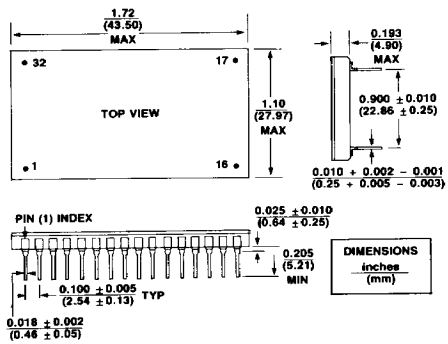
(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	HS 9476J	HS 9476K	HS 9476S/B	HS 9476T/B
RESOLUTION	16 bits	*	*	**
ANALOG INPUTS				
Voltage Range		*	*	**
Bipolar	±5V, ±10V	*	*	**
Unipolar	0 to +10V, 0 to +20V			
Overvoltage, No Damage		*	*	**
10V Range	±15V max	*	*	**
20V Range	±30V max			
Impedance		*	*	**
10V Range	10kΩ	*	*	**
20V Range	20kΩ			
DIGITAL INPUTS[1]		*	*	**
Convert Command (Pin 31)	Positive pulse 50 nsec wide, trailing edge initiates conversion	*	*	**
Logic Loading	1 LSTTL load	*	*	**
T/H Command (Pin 17)	TRACK MODE, Logic "1" HOLD MODE, Logic "0"	*	*	**
DIGITAL OUTPUTS[1] (All Codes Complementary)				
Output Codes[2]		*	*	**
Unipolar	CSB	*	*	**
Bipolar	COB, CTC	*	*	**
Output Drive	8 LSTTL loads	*	*	**
Status	Logic "1" during conversion	*	*	**
Status Output Drive	8 LSTTL loads			
Internal Clock[3]		*	*	**
Clock Output Drive	4 LSTTL loads	*	*	**
Frequency	933 kHz			
TRANSFER CHARACTERISTICS				
Integral Linearity Error	0.006% of FSR max	0.003% of FSR max	0.006% of FSR max	0.003% of FSR max
Differential Linearity Error	0.003% of FSR typ, 0.006% of FSR max	*	*	**
Gain Error[4]	±0.05% typ, ±0.2% max	*	*	**
Offset Error[4]		*	*	**
Unipolar	±0.05% of FSR typ, ±0.2% of FSR max	*	*	**
Bipolar	±0.05% of FSR typ, ±0.2% of FSR max	*	*	**
3σ Noise at Transitions (pk-pk)	0.003% of FSR max			
DRIFT		*	*	**
Gain	±20 ppm/°C max			
Offset		*	*	**
Unipolar	±5 ppm/°C of FSR max	*	*	**
Bipolar	±15 ppm/°C of FSR max			
Linearity	±3 ppm/°C of FSR max	±2 ppm/°C of FSR max	±3ppm/°C of FSR max	±2ppm/°C of FSR max
Guaranteed No Missing Codes[5]	13 bits (0°C to 70°C)	14 bits (0°C to 70°C)	13 bits (−55°C to 125°C)	14 bits (−55°C to 125°C)
THROUGHPUT[6]				
Sampling Rate		*	*	**
14-Bit Resolution	50 kHz typ, 47.6 kHz min	*	*	**
16-Bit Resolution	45.4 kHz typ, 43.4 kHz min			
ADC CHARACTERISTICS				
Conversion Time[3] (t_{CONV})		*	*	**
12-Bits	13μ sec max	*	*	**
14-Bits	15μ sec max	*	*	**
16-Bits	17μ sec max			
SAMPLE/HOLD CHARACTERISTICS				
Track (Sample) Mode Dynamics				
Frequency Response		*	*	**
Small Signal (−3 dB)	1 MHz	*	*	**
Full Signal Bandwidth	0.2 MHz	*	*	**
Slew Rate	6V/μsec	*	*	**
Noise in Track Mode, DC to 1.0 MHz	50μV rms			
Hold Mode Dynamics		*	*	**
Droop Rate	0.1μV/μsec max	*	*	**
Droop Rate at T_{max}	10μV/μsec max			
Feedthrough Rejection		*	*	**
(20Vp-p @ 20 kHz)	90 dB min	*	*	**
(20Vp-p @ 200 kHz)	86 dB min			
Track (Sample)-To-Hold Switching		*	*	**
Aperture Delay	30 nsec	*	*	**
Aperture Uncertainty	100 psec	*	*	**
Offset Step (Pedestal)	±2mV max			
Switching Transient		*	*	**
Amplitude	50mV	*	*	**
Settling to 1mV	0.5μsec	*	*	**
Settling to 0.3mV (t_{TH})	1μsec max			
Hold-To-Track (Sample) Dynamics Acquisition Time to ±0.003% (20V Step) (t_{ACQ})	4μsec typ, 5μsec max	*	*	**
POWER REQUIREMENTS				
Power Consumption	1520 mW max	*	*	**
Rated Voltage, Analog	±15V (±0.5V max)	*	*	**
Rated Voltage, Digital	+5V (±0.5V max)	*	*	**
Supply Current		*	*	**
+15V	+38 mA max	*	*	**
−15V	−51 mA max	*	*	**
+5V	+37 mA max	*	*	**
Power Supply Rejection	0.001%/% (all supplies)	*	*	**
Warm Up Time	1 minute			
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	**
Storage	−25°C to +85°C	*	−65°C to +150°C	**
PACKAGE				
32 Pin				

NOTES:

1. Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max, Logic "1" = 2.4V min. **2.** CSB — Complementary Straight Binary, COB — Complementary Offset Binary, CTC - Complementary Two's Complement. **3.** With CLK RATE CTRL (Pin 23) left open. **4.** Adjustable to zero. **5.** A missing code is defined as less than 0.2 LSB wide. **6.** Throughput Rate = $1/(t_{ACQ} + t_{TH} + t_{CONV})$. *Specifications same as HS 9476J. **Specifications same as HS 9476S.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	32	SHORT CYCLE
2	BIT 2	31	CONVERT COMMAND
3	BIT 3	30	+5V
4	BIT 4	29	GAIN ADJUST
5	BIT 5	28	+15V
6	BIT 6	27	COMPARATOR IN
7	BIT 7	26	BIPOLAR OFFSET
8	BIT 8	25	10V INPUT
9	BIT 9	24	20V INPUT
10	BIT 10	23	CLOCK RATE CONTROL
11	BIT 11	22	ANALOG GROUND
12	BIT 12	21	−15V
13	BIT 13 (LSB FOR 13 BITS)	20	CLOCK OUT
14	BIT 14 (LSB FOR 14 BITS)	19	DIGITAL GROUND
15	BIT 15	18	STATUS
16	BIT 16	17	T/$\overline{H}$

Analog Input Voltage Range	Defined As:	± 10V	± 5V	0 to + 10V	0 to + 20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR	20V	10V	10V	20V
	2^n	2^n	2^n	2^n	2^n
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
	n = 13	2.44mV	1.22mV	1.22mV	2.44mV
	n = 14	1.22mV	610μV	610μV	1.22mV
	n = 15	610μV	305μV	305μV	610μV
Transition Values					
MSB LSB					
000...000[4]	+ Full Scale	+ 10V − 3/2LSB	+ 5V − 3/2LSB	+ 10V − 3/2LSB	+ 20V − 3/2LSB
011...111	Mid Scale	0 − 1/2LSB	0 − 1/2LSB	+ 5V − 1/2LSB	+ 10V − 1/2LSB
111...110	− Full Scale	− 10V + 1/2LSB	− 5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

1. Complementary Offset Binary.
2. Complementary Two's Complement — obtained by inverting the most significant bit. MSB (pin 1).
3. Complementary Straight Binary.
4. Voltages given are the nominal value for transition to the code specified.

Table 1. Input Voltages, Transition Values, LSB Values, and Code Definitions

INSTALLATION

GROUNDING AND LAYOUT PRECAUTIONS

Due to the small bit weight (610 μV for 1 LSB, 14 bit, 10V range) special attention must be paid to the layout of the PC board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground plane can be directly connected to pin 22 of the HS 9476. All digital lines should run on the soldering side of the PC board.

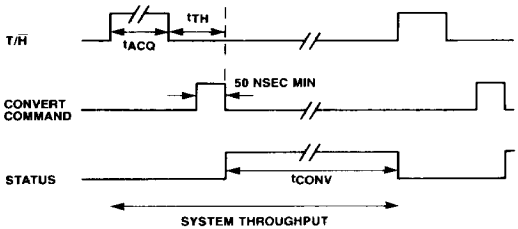
In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package. For the HS 9476, pin 19 (digital ground) and pin 22 (analog ground) should be tied together as close as possible to the converter.

POWER SUPPLY DECOUPLING

Internal 0.01 μF power supply bypass capacitors are included in the HS 9476 to maintain device stability. If the supply voltages contain excessive high frequency noise, additional external high frequency capacitors may be necessary to maintain low noise performance.

OPERATING INSTRUCTIONS

The HS 9476 tracks an analog input signal when the T/$\overline{H}$ command is high. When entering the hold mode (T/$\overline{H}$ goes low), time must be given to the sample-hold amplifier for settling in the hold mode. Hence, the A/D conversion, initiated by the falling edge of the CONVERT COMMAND cannot begin immediately after the T/$\overline{H}$ command is low: a 1 μsec delay must be added to account for the hold mode settling as shown in the system timing diagram of Figure 1.

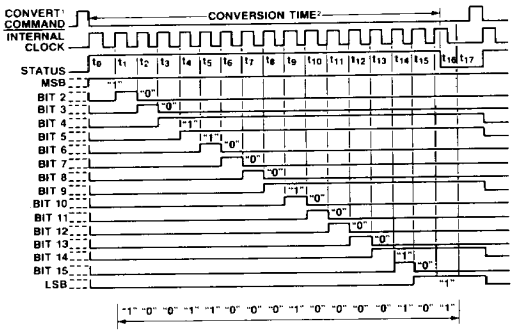


tACQ = SAMPLE-HOLD ACQUISITION TIME — 4μSEC TYP, 5μSEC MAX
tTH = SAMPLE-HOLD HOLD MODE SETTLING TIME — 1μSEC MAX
tCONV = A/D CONVERSION TIME — 14-BITS RESOLUTION — 15 SEC MAX
16 BITS RESOLUTION — 17μSEC MAX
SYSTEM THROUGHPUT = 14-BITS — 20μSEC TYP, 21μSEC MAX
16-BITS — 22μSEC TYP, 23μSEC MAX

Figure 1. System Timing Diagram

Simultaneous to a CONVERT COMMAND signal, the STATUS flag goes high indicating a conversion is in progress and removing the inhibit applied to the gated clock. The conversion is accomplished by successively comparing the analog input to the feedback DAC output, one bit at a time (MSB first, LSB last). After the LSB decision is made, there is a 30 nsec delay period before the STATUS flag goes low indicating that the conversion is complete and that the output data is valid. Incorporation of this 30 nsec delay guarantees that the digital data is valid at the logic "1" to "0" transition of the STATUS flag, allowing parallel data transfer to be initiated by the trailing edge of the STATUS signal. Resetting the STATUS flag to logic "0" restores the gated clock inhibit signal forcing the clock output to the logic "0" state. The clock remains low until the next conversion is initiated.

Figure 2 shows the detailed timing for the A/D converter of the HS 9476.



NOTES:
1. THE CONVERT COMMAND PULSE WIDTH IS 50nS MIN. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND. IF A NEW CONVERT COMMAND HAPPENS DURING CONVERSION, ALL THE LOGIC OF THE A/D IS RESET AND A NEW CONVERSION BEGINS.
2. 15μs FOR 14 BITS.

*Figure 2. A/D Timing Diagram (Output Code 1001100010000101)**

*All codes are complementary coded. Thus, the output code in Figure 2 represents an analog input whose positive true digital equivalent is 0110011101111010.

APPLICATIONS CIRCUIT

The purpose of this paragraph is to describe circuit examples for the implementation of the timing described earlier in Figure 1.

Figure 3 shows the circuit and the associated timing. The idea is to generate the T/$\overline{H}$ command from the CONVERT COMMAND signal and the STATUS flag.

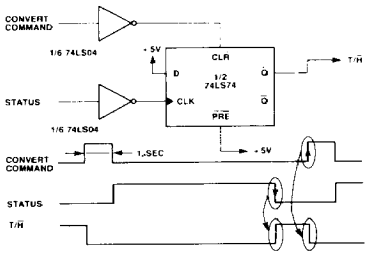


Figure 3. Generation of the T/$\overline{H}$ Command from CONVERT COMMAND and STATUS

The rising edge of the CONVERT COMMAND makes the T/$\overline{H}$ command going low (hold mode). The falling edge of the STATUS flag makes the sample-hold going back in track mode (T/$\overline{H}$ = "1").

To obtain the maximum throughput (HS 9476 short cycled to 14 bits), the CONVERT COMMAND should be a 50 kHz signal. Figure 4 shows how to obtain it from a 500 kHz clock. Slowing down this frequency reduces the throughput rate, which is given by fclock/10.

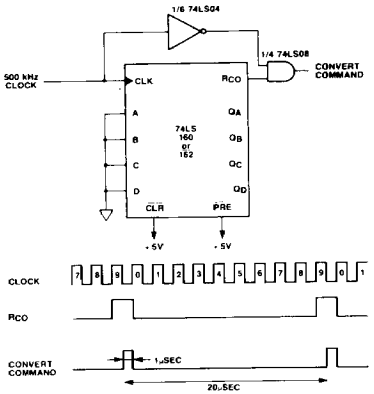


Figure 4. Generation of the CONVERT COMMAND

Using the schematics of Figure 3 and Figure 4 for applying the HS 9476 necessitates only 4 ICs: 74LS08, 74LS04, 74LS74 and 74LS160.

OPTIONAL UNIPOLAR OFFSET OR BIPOLAR ZERO ADJUST

The unipolar offset or bipolar zero error may be trimmed to zero (optional) using an external trim potentiometer connected to the HS 9476 as shown in Figures 5 or 6.

The adjustment circuit shown in Figure 5 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 1.8MΩresistor to pin 27. In this case a carbon composition resistor is adequate: if we assume that its tempco is − 1200 ppm/°C and that the adjustment range required is no more than 16 LSB_{14} (0.1% FS), it contributes for only 1.17 ppm/°C of tempco (0.001 x 1200). The low tempco adjustment circuit in Figure 6 contributes for negligible tempco if metal film resistors (tempco <100 ppm/°C) are used.

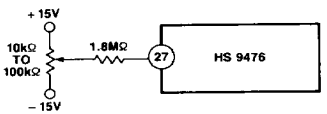


Figure 5. Unipolar Offset or Bipolar Zero Adjustment Circuit (± 0.4% FSR)

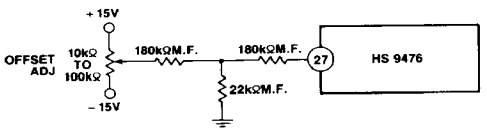


Figure 6. Low Tempco Adjustment Circuit

With both circuits the fixed resistor connected to pin 27 should be located close to the converter to keep the pin connection runs short. Offset or zero should be adjusted after warm-up and before gain (see below) to prevent interaction of the two adjustments. Offset or zero is adjusted with the analog input near zero volt. Refer to Table 1 for the appropriate values.

OPTIONAL GAIN ADJUST

The gain error may be trimmed to zero (optional) using an external offset trim potentiometer connected to the HS 9476 as shown in Figure 7.

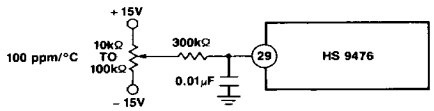


Figure 7. Gain Adjustment Circuit (± 0.2% FSR)

The gain adjustment circuit shown in Figure 7 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 300 K Ω resistor to pin 29. Gain should be adjusted after warm-up and after unipolar offset or bipolar zero (see above) to prevent interaction of the two adjustments. Gain is adjusted with the analog input near the most positive end of the analog range. Refer to Table 1 for the appropriate values.

OPTIONAL CONVERSION TIME ADJUST

Short Cycle: A SHORT CYCLE input, pin 32, permits the A/D timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted. For instance, when 14-bit resolution is desired, pin 32 is connected to bit 15 (output pin 15). The conversion cycle will then terminate and the STATUS flag reset after the bit 14 decision has been made. SHORT CYCLE connections and associated conversion times are summarized in Table 2 below for a 933 kHz clock.

Resolution Bits	(%FSR)	Max Conversion Time (μs)	Connect SHORT CYCLE Pin 32* to Pin:
16	0.0015	17.1	N/C (open)
15	0.003	16.1	16
14	0.006	15.0	15
13	0.012	13.9	14
12	0.024	12.9	13
10	0.100	10.7	11

*Pin 32 cannot be connected to +5V

Table 2. Short Cycle Connections

Clock Rate Adjust: The A/D of the HS 9476 may be operated at faster or slower conversion times by connecting the CLOCK RATE CONTROL, pin 23, to an external multiturn trim potentiometer with a TCR of ± 100 ppm/°C or less as shown in Figure 8. The conversion time is trimmed to 17μsec (16-bits) at the factory with CLK RATE CTRL open. The typical conversion time versus the clock rate control voltage is shown in Figure 9. The nonlinearity errors will vary with speed as shown in Figure 10.

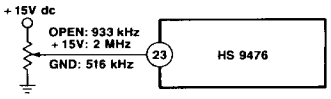


Figure 8. Optional Clock Rate Control Circuit

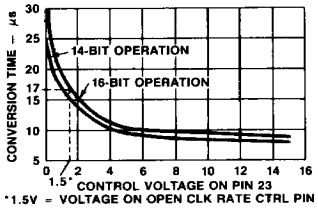


Figure 9. Conversion Time Vs. Clock Rate Control Voltage

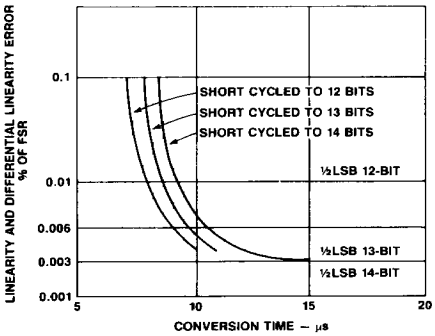


Figure 10. HS 9476 Nonlinearity Vs. Conversion Time

DIGITAL OUTPUT DATA

Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Complementary two's complement may be obtained by inverting MSB (pin 1). Table 1 shows the LSB, transition values and code definitions for each possible analog input signal range for 12-15 bits of resolution. The output data is CMOS compatible and the drive capability is 8 LSTTL loads. If long digital lines have to be driven, external output buffers are recommended.

INPUT SCALING

The HS 9476 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table 3.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Pin 25 To
± 10V	COB or CTC*	27	Input Sig.	Pin 22
± 5V	COB or CTC*	27	Pin 22	Input Sig.
0 to +10V	CSB	22	Pin 22	Input Sig.
0 to +20V	CSB	22	Input Sig.	Pin 22

*Obtained by inverting MSB (pin 1)
NOTE: The unused analog input is grounded to reduce noise pickup.

Table 3. HS 9476 Input Scaling Connections

CONNECTIONS AND CALIBRATION PROCEDURE

(14-Bit Resolution Example)

Figures 11a and 11b show the different analog and power connections required for unipolar 0 to 10V and bipolar − 10V to + 10V input range operation.

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figure 11, are used for device calibration. To prevent interaction of these two adjustments, unipolar offset or bipolar zero is always adjusted first and then gain.

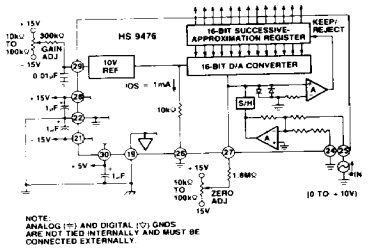


Figure 11a. Analog and Power Connections for Unipolar 0 to + 10V Input Range

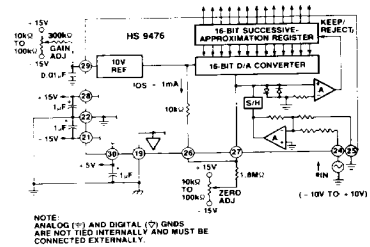


Figure 11b. Analog and Power Connections for Bipolar − 10V to + 10V Input Range

CALIBRATION FOR 0 TO + 10V RANGE

Set analog input to + 1 LSB_{14} = 0.00061V. Adjust ZERO for digital output = 11111111111110. ZERO is now adjusted. Set analog input to + FS − 2 LSB_{14} = 9.99878V. Adjust GAIN for 00000000000001 digital output code; GAIN is now calibrated. Half scale calibration check: set analog input to + 5V; digital output code should be 01111111111111.

CALIBRATION FOR − 10V TO + 10V RANGE

(Complementary Offset Binary Code)

Set analog input to 0.00000V; adjust ZERO for 01111111111111 digital output code. Set analog input to 9.99756V (+ FS − 2 LSB_{14}); adjust GAIN for 00000000000001 digital output code.

OTHER RANGES

Coding relationships and calibration points for 0 to + 20V and − 5V to + 5V ranges can be found by doubling and halving respectively the corresponding code equivalents listed for the 0 to + 10V and − 10V to + 10V ranges, as indicated in Table 1.

Unipolar offset or bipolar zero and full-scale calibrations can be accomplished to a precision of ± ½ LSB using the static adjustment procedure described above.

DISCUSSION OF SPECIFICATIONS

SYSTEM SPECIFICATIONS

The actual conversion errors that are associated with the HS 9476 are combinations of analog errors due to the sample-hold amplifier and the A/D.

Figure 12 shows the ideal HS 9476 transfer characteristics.

All the system specifications include the errors introduced by both the sample-hold amplifier and the A/D converter. The offset error is a shift (left or right) of the ideal transfer characteristics. Gain error is an error in the slope of the transfer function. Both these errors can be trimmed externally as explained earlier. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristics from a zero input voltage (which calls for an "all 1's" digital output) to a point which is defined as a full scale **(END POINT definition).** Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size. If the differential linearity is too negative, a code can be missing. The HS 9476K and T/B are specified as having no missing codes at the 14 bit level for the commercial and military temperature ranges.

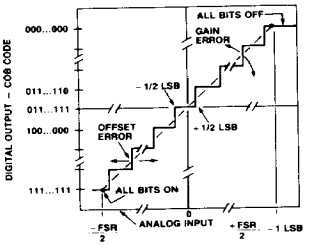


Figure 12. Ideal HS 9476 Transfer Characteristics (Bipolar Mode)

SAMPLE/HOLD SPECIFICATIONS

Acquisition Time is the time required by the sample/hold amplifier to "switch" from the hold mode to the track (sample) mode. This time is measured between the application of a "track" command and the point at which the output has settled to within a specified error band. This time includes the switch delay time, slewing time and settling time for a given output voltage change.

Switching Transient Settling (Hold Mode Settling) is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

Aperture Delay is the time lag between the application of the "hold" command and the instant the output stops tracking the input. It consists primarily of the propagation delay of the switch driver. Since it is a known quantity, the "hold" command can be advanced to account for this delay.

Offset Step (Pedestal) is a track (sample)-to-hold offset that results from unequal charge transfers when the device is switched into the hold mode.

Aperture Uncertainty (Jitter) is the variation in the aperture delay from sample to sample. This time uncertainty produces a voltage uncertainty proportional to the input slew rate.

Feedthrough is the amount of analog input signal that is coupled through to the analog output while the circuit is in the hold mode. It is usually expressed in dB's. Since feedthrough increases with frequency, it should be specified at a given frequency.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB. This, in turn, determines the maximum conversion time that an A/D converter can have to be used with a particular S/H.

Full Power Bandwidth is the frequency at which a full scale input/output sine wave becomes slew rate limited to – 3 dB.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

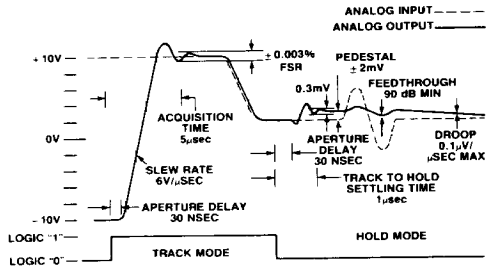


Figure 13. Illustration of the Main S/H Characteristics

DYNAMIC PERFORMANCE

The system specifications discussed earlier describe the DC performance of the HS 9476. For digital signal processing oriented applications, however, the response of the sampling A to D converter to AC signals must be known.

At Hybrid Systems, two different kinds of dynamic testing can be performed on the device:

1. Signal-to-Noise Ratio (SNR) test
2. Histogram test

These tests are discussed in the following paragraphs. They have been performed on devices **short cycled to 14 bits (in order to get a 50kHz throughput rate)** and configured in bipolar 10V mode.

The SNR test is the primary measurement of signal fidelity: distortion of an input sinewave due to Integral Linearity errors is quantified by this test. More precisely a finite time sequence of sampled data from a spectrally pure sine wave input is computed by the tester into a frequency spectrum using a Fast Fourier Transform algorithm. From this frequency domain representation of the output data, the effect of Integral Non-Linearity may be measured: harmonics of the input sine wave caused by Integral Linearity errors are aliased into the baseband spectrum. The magnitude of the fundamental's spectral lines (the signal) is summed, then divided by the sum of the remaining spectral lines (the noise). The logarithm of this number, multiplied by 20 provides the SNR expressed in decibels. For an ideal converter, it can be shown that:

$$SNR = 6.02 \times N + 1.76dB$$

(N = number of bits of the converter)

For a 14 bit converter, the SNR should be 86dB for all frequencies below the Nyquist rate (25kHz for the HS 9476). If the linearity error is $\pm$ ½LSB, a SNR of 3dB less is expected.

Figure 14 to 16 show the SNR results of the HS 9476 for full scale input frequency of 2.345, 12.345, 23.456kHz respectively. This shows the very slow degradation of the SNR with the input frequency.

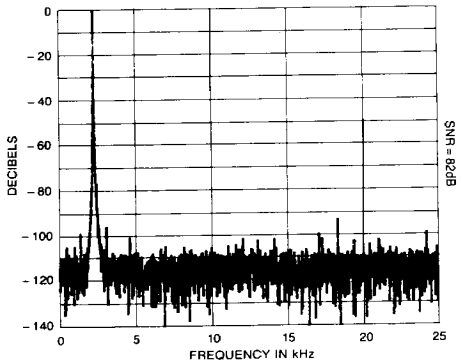


Figure 14. FFT of the HS 9476, Fin = 2.234kHz, Fsample = 50kHz

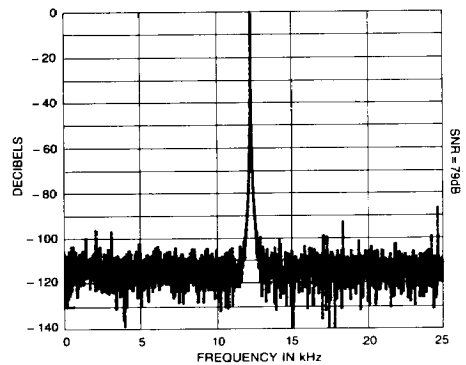


Figure 15. FFT of the HS 9476, Fin = 12.234kHz, Fsample = 50kHz

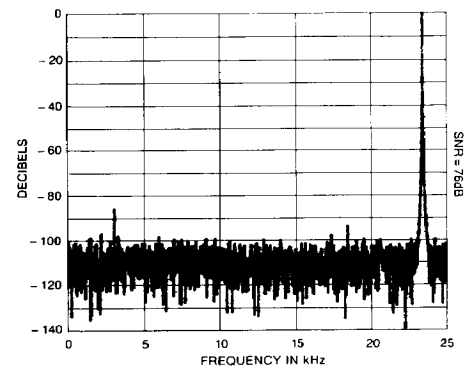


Figure 16. FFT of the HS 9476, Fin = 23.234kHz, Fsample = 50kHz

The HS 9476 will exhibit an improvement in SNR when less than full scale input signal is applied. Figure 17 illustrates that improvement.

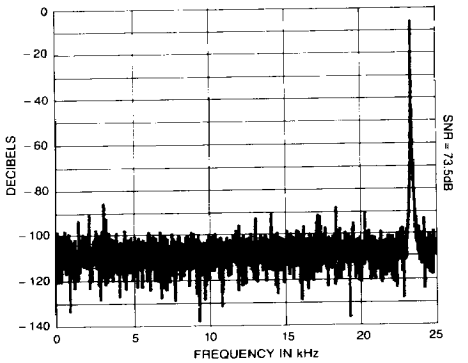


Figure 17. FFT of the HS 9476, Fin = 23.346kHz, Fsample = 50kHz, – 6dB input levels

Histogram testing is used to evaluate the dynamic differential linearity of a converter. A sine wave is applied to the converter and a finite number of sampled data is taken and stored by the tester. The number of occurences of each code is then determined, and this histogram is compared with an ideal quantized sine wave of same gain and offset. The ratio of the real number of occurences to the ideal number yields an effective code width for each code. Figure 18 shows the good dynamic differential linearity of the HS 9476 even when the input signal approaches the Nyquist bandlimit.

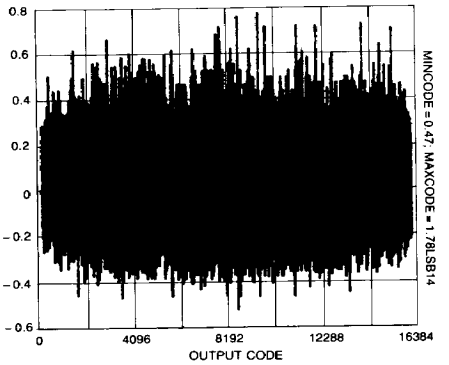


Figure 18. HS 9476 Dynamic Differential Linearity, Fin = 23.456kHz, Fsample = 50kHz

ORDERING INFORMATION

MODEL	MAX LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
HS 9476K	±0.003% FSR	0°C to +70°C	—
HS 9476J	±0.006% FSR	0°C to +70°C	—
HS 9476T/B	±0.003% FSR	–55°C to +125C	MIL-STD-883
HS 9476S/B	±0.006% FSR	–55°C to 125°C	MIL-STD-883