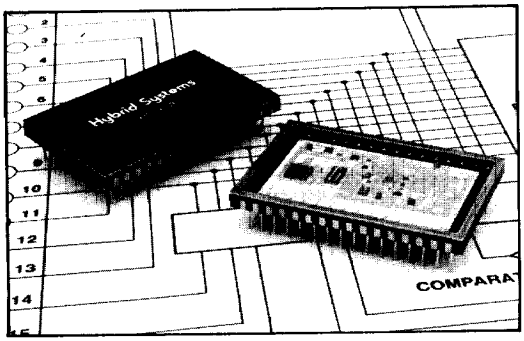
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9576

HIGH SPEED, LOW COST 16-BIT A/D

FEATURES

- Complete 16-bit ADC with internal reference and clock
- Linearity error ±0.003% max
- Fast conversion time: 15μSec max
- Pin for pin compatible with BB ADC 76 and AD 376

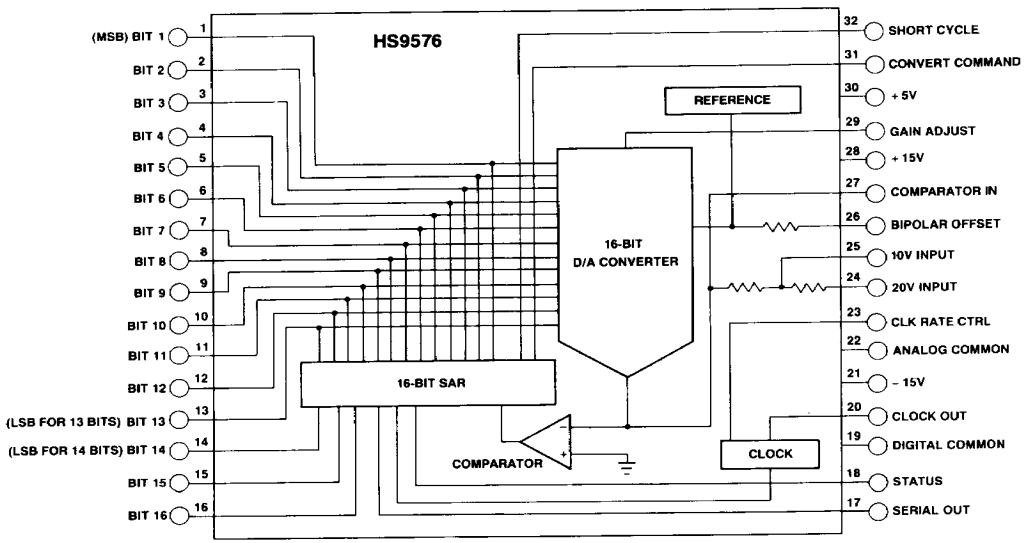


DESCRIPTION

The HS9576 is a low cost, 16-bit successive approximation A/D converter. The converter is complete with internal reference, short cycling capabilities and thin-film scaling resistors which allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V. Integral non-linearity is specified at ±0.003% of FSR maximum while no missing codes to 14 bits is guaranteed over the full operating temperature range. Conversion time is 15μsec maximum for 14 bits with the option for faster conversion times to resolutions less than 14 bits. Power consumption is specified at 1W typical.

The HS9576 is a versatile building block for high-accuracy, high-speed systems. When used with the HS9716 sample (track)/hold, a high-speed acquisition system is formed which can digitize signals at a rate of 50,000 conversions per second. The HS9576 is available for operation over the commercial (0°C to +70°C) temperature range or −55°C to +125°C with full MIL-STD-883C screening.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	HS 9576J	HS 9576K	HS 9576S/B	HS 9576T/B
RESOLUTION	16 bits	•	•	•
ANALOG INPUTS				
Voltage Range		•	•	•
Bipolar	±2.5, ±5, ±10V	•	•	•
Unipolar	0 to +5, +10, +20V	•	•	•
Impedance	2.5KΩ on 5V ranges	•	•	•
	5KΩ on 10V ranges	•	•	•
	10KΩ on 20V ranges	•	•	•
DIGITAL INPUTS[1]				
Convert Command	Positive pulse 50 nsec wide (min) trailing edge initiates conversion	•	•	•
Logic Loading	1 LSTTL load	•		
DIGITAL OUTPUTS[1]				
(All Codes Complementary)				
Output Codes[2]		•	•	•
Unipolar	CSB	•		
Bipolar	COB, CTC[3]	•	•	•
Output Drive	8 LSTTL loads			
Status	Logic "1" during conversion			
Status Output Drive	8 LSTTL loads max	•	•	•
Internal Clock[4]			•	•
Clock Output Drive	4 LSTTL loads max	•	•	•
Frequency	933 kHz	•		
TRANSFER CHARACTERISTICS				
Integral Linearity Error[5]	±0.006% of FSR max	±0.003% of FSR max	±0.006% of FSR max	±0.003% of FSR max
Differential Linearity Error	±0.003% of FSR typ	•	•	•
Gain Error[6]	±0.05% typ; ±0.2% max	•	•	•
Offset Error[6]				
Unipolar	±0.05% of FSR typ; ±0.1% of FSR max	•	•	•
Bipolar	±0.05% of FSR typ; ±0.2% of FSR max	•	•	•
3σNoise at Transitions (pk-pk)	0.001% of FSR typ; 0.003% of FSR max	•	•	•
CONVERSION TIME[4]				
12-Bits	13 μsec max	•	•	•
14-Bits	15 μsec max	•	•	•
16-Bits	17 μsec max	•	•	•
POWER REQUIREMENTS				
Power Consumption	1000 mW typ; 1100 mW max	•	•	•
Rated Voltage, Analog	±15V (±0.5V max)	•	•	•
Rated Voltage, Digital	+5V (±0.25V max)	•	•	•
Supply Drain		•	•	•
+15Vdc	+23 mA max	•	•	•
−15Vdc	−38 mA max	•	•	•
+5Vdc	+37 mA max	•	•	•
Power Supply Sensitivity	0.001% of FSR/%ΔV_S (all supplies)	•	•	•
WARM-UP TIME	3 minutes	•	•	•
DRIFT				
Gain	±15 ppm/°C max	•	•	•
Offset				
Unipolar	±4 ppm of FSR/°C max	±2 ppm of FSR/°C max	±4 ppm of FSR/°C max	±2 ppm of FSR/°C
Bipolar	±10 ppm of FSR/°C max	•	•	•
Linearity	±3 ppm of FSR/°C max	±2 ppm of FSR/°C max	±3 ppm of FSR/°C max	±2 ppm of FSR/°C
Guaranteed No Missing Codes[7]				
Temperature Range	13 Bits (0°C to +70°C)	14 Bits (0°C to +70°C)	13 Bits (−55°C to +125°C)	14 Bits (−55°C to +125°C)
TEMPERATURE RANGE				
Operating Temperature Range	0°C to +70°C	•	−55°C to +125°C	•
Storage Temperature Range	−55°C to +85°C	•	−65°C to +150°C	•

NOTES:

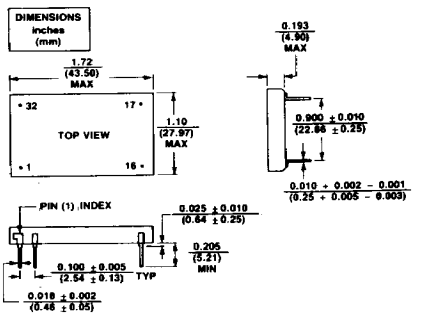
1. Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max, Logic "1" = 2.4V min. 2. CSB — Complementary Straight Binary. COB — Complementary Offset Binary. CTC — Complementary Two's Complement. 3. TCB coding obtained by inverting MSB (Pin 1). Valid for parallel output data only. 4. With CLK RATE CTRL (Pin 23) left open. 5. End Point Definition. 6. Adjustable to zero. 7. A missing code is defined as less than 0.2 LSB wide.

*Specifications same as HS 9576J.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	32	SHORT CYCLE
2	BIT 2	31	CONVERT COMMAND
3	BIT 3	30	+5V
4	BIT 4	29	GAIN ADJUST
5	BIT 5	28	+15V
6	BIT 6	27	COMPARATOR IN
7	BIT 7	26	BIPOLAR OFFSET
8	BIT 8	25	10V INPUT
9	BIT 9	24	20V INPUT
10	BIT 10	23	CLOCK RATE CONTROL
11	BIT 11	22	ANALOG GROUND
12	BIT 12	21	−15V
13	BIT 13 (LSB FOR 13 BITS)	20	CLOCK OUT
14	BIT 14 (LSB FOR 14 BITS)	19	DIGITAL GROUND
15	BIT 15	18	STATUS
16	BIT 16	17	SERIAL OUT

PACKAGE OUTLINE



Analog Input Voltage Range	Defined As:	± 10V	± 5V	± 2.5V	0 to + 10V	0 to + 5V	0 to + 20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR / 2^n n = 12 n = 13 n = 14 n = 15	20V / 2^n 4.88mV 2.44mV 1.22mV 610μV	10V / 2^n 2.44mV 1.22mV 610μV 305μV	5V / 2^n 1.22mV 610μV 305μV 152μV	10V / 2^n 2.44mV 1.22mV 610μV 305μV	5V / 2^n 1.22mV 610μV 305μV 152μV	20V / 2^n 4.88mV 2.44mV 1.22mV 610μV
Transition Values MSB LSB 000...000[4] 011...111 111...110	 + Full Scale Mid Scale – Full Scale	 + 10V – 3/2LSB 0 – 1/2LSB – 10V + 1/2LSB	 + 5V – 3/2LSB 0 – 1/2LSB – 5V + 1/2LSB	 + 2.5V – 3/2LSB 0 – 1/2LSB – 2.5V + 1/2LSB	 + 10V – 3/2LSB + 5V – 1/2LSB 0 + 1/2LSB	 + 5V – 3/2LSB + 2.5V – 1/2LSB 0 + 1/2LSB	 + 20V – 3/2LSB + 10V – 1/2LSB 0 + 1/2LSB

1. Complementary Offset Binary.
2. Complementary Two's Complement — obtained by inverting the most significant bit. MSB (pin 1).
3. Complementary Straight Binary.
4. Voltages given are the nominal value for transition to the code specified.

Table 1. Input Voltages, Transition Values, LSB Values, and Code Definitions

INSTALLATION

GROUNDING AND LAYOUT PRECAUTIONS

Due to the small bit weight (610 μV for 1 LSB, 14 bit, 10V range) special attention must be paid to the layout of the PC board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground plane can be directly connected to pin 22 of the HS 9576. All digital lines should run on the soldering side of the PC board.

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package. For the HS 9576, pin 19 (digital ground) and pin 22 (analog ground) should be tied together as close as possible to the converter.

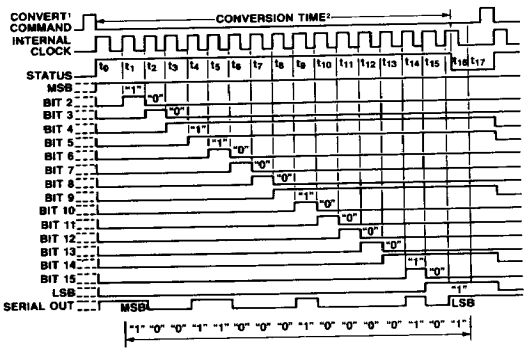
POWER SUPPLY DECOUPLING

Internal 0.01 μF power supply bypass capacitors are included in the HS 9576 to maintain device stability. If the supply voltages contain excessive high frequency noise, additional external high frequency capacitors may be necessary to maintain low noise performance.

OPERATING INSTRUCTIONS

TIMING

The timing diagram is shown in Figure 1. A conversion is initiated by the "trailing edge" of the CONVERT COMMAND. Simultaneous to a CONVERT COMMAND signal, the STATUS flag goes high indicating a conversion is in progress and removing the inhibit applied to the gated clock. The conversion is accomplished by successively comparing the analog input to the feedback DAC output, one bit at a time (MSB first, LSB last). After the LSB decision is made, there is a 30 nsec delay period before the STATUS flag goes low indicating that the conversion is complete and that the output data is valid. Incorporation of this 30 nsec delay guarantees that the digital data is valid at the logic "1" to "0" transition of the STATUS flag, allowing parallel data transfer to be initiated by the trailing edge of the STATUS signal. Resetting the STATUS flag to logic "0" restores the gated clock inhibit signal forcing the clock output to the logic "0" state. The clock remains low until the next conversion is initiated.



NOTES:
1. THE CONVERT COMMAND PULSE WIDTH IS 50ns MIN. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND. IF A NEW CONVERT COMMAND HAPPENS DURING CONVERSION, ALL THE LOGIC OF THE A/D IS RESET AND A NEW CONVERSION BEGINS.
2. 15μs FOR 14 BITS.

*Figure 1. Timing Diagram (Output Code 1001100010000101)**

*Note that all codes are complementary coded. Thus, the output code in Figure 1 represents an analog input whose positive true digital equivalent is 0110011101111010.

OPTIONAL OFFSET ADJUST

The unipolar offset or bipolar zero error may be trimmed to zero (optional) using an external trim potentiometer connected to the HS 9576 as shown in Figures 2 or 3.

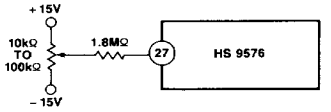


Figure 2. Unipolar Offset or Bipolar Zero Adjustment Circuit (± 0.4% FSR)

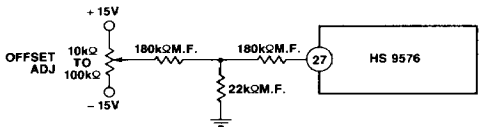


Figure 3. Low Tempco Adjustment Circuit

The adjustment circuit shown in Figure 2 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 1.8MΩ resistor to pin 27. In this case a carbon composition resistor is adequate: if we assume that its tempco is - 1200 ppm/°C and that the adjustment range required is no more than 16 LSB14 (0.1% of FS), it contributes only 1.17 ppm/°C of tempco (0.001 × 1200). The low tempco adjustment circuit in Figure 3 contributes negligible tempco if metal film resistors (tempco <100 ppm/°C) are used.

With both circuits the fixed resistor connected to pin 27 should be located close to the converter to keep the pin connection runs short. Offset or zero should be adjusted after warm-up and before gain (see below) to prevent interaction of the two adjustments. Offset or zero is adjusted with the analog input near zero volts. Refer to Table 1 for the appropriate values.

OPTIONAL GAIN ADJUST

The gain error may be trimmed to zero (optional) using an external offset trim potentiometer connected to the HS 9576 as shown in Figure 4.

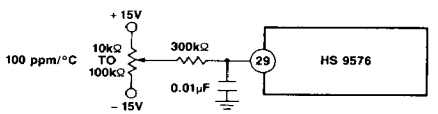


Figure 4. Gain Adjustment Circuit (± 0.2% FSR)

The gain adjustment circuit shown in Figure 4 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 300 KΩ resistor to pin 29. Gain should be adjusted after warm-up and after unipolar offset or bipolar zero (see above) to prevent interaction of the two adjustments. Gain is adjusted with the analog input near the most positive end of the analog range. Refer to Table 1 for the appropriate values.

OPTIONAL CONVERSION TIME ADJUST

Short Cycle: A SHORT CYCLE input, pin 32, permits the timing cycle shown in Figure 1 to be terminated after any number of desired bits has been converted. For instance, when 14-bit resolution is desired, pin 32 is connected to bit 15 (output pin 15). The conversion cycle will then terminate and the STATUS flag reset after the bit 14 decision has been made. SHORT CYCLE connections and associated conversion times are summarized in Table 2 below for a 933 kHz clock.

Resolution Bits	(%FSR)	Max Conversion Time (μs)	Connect SHORT CYCLE Pin 32* to Pin:
16	0.0015	17.1	N/C (open)
15	0.003	16.1	16
14	0.006	15.0	15
13	0.012	13.9	14
12	0.024	12.9	13
10	0.100	10.7	11

*Pin 32 cannot be connected to +5V.

Table 2. Short Cycle Connections

Clock Rate Adjust: The HS 9576 may be operated at faster or slower conversion times by connecting the CLOCK RATE CONTROL, pin 23, to an external multiturn trim potentiometer with a TCR of ± 100 ppm/°C or less as shown in Figure 5. The conversion time is trimmed to 17μsec (16-bits) at the factory with CLK RATE CTRL open. The typical conversion time versus the clock rate control voltage is shown in Figure 6. The nonlinearity errors will vary with speed as shown in Figure 7.

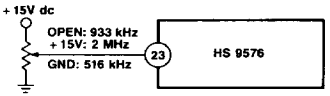


Figure 5. Optional Clock Rate Control Circuit

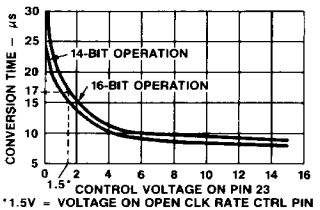


Figure 6. Conversion Time Vs. Clock Rate Control Voltage

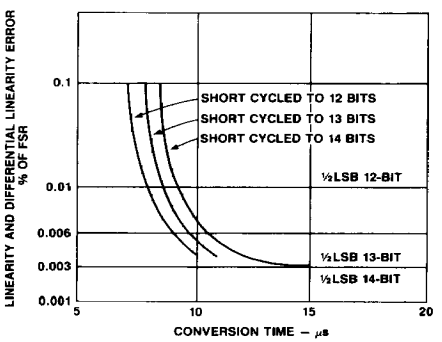


Figure 7. HS 9576 Nonlinearity Vs. Conversion Time

EXTERNAL CLOCK

An external clock may be connected to the CONVERT COMMAND input (pin 31); the CONVERT COMMAND of Figure 1 is not used in this case. The external clock must consist of negative going pulses 100 to 200 nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 16 clock cycles.

The converter begins to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after the STATUS output has gone low, signaling the end of the previous conversion. When continously converting in this manner, the STATUS output goes low for one external clock period following the completion of each conversion. Figure 8 shows continuous conversion using an external clock.

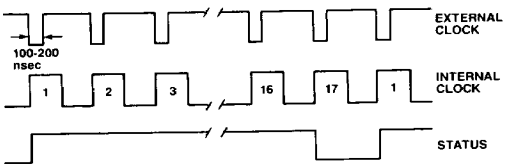


Figure 8. Continuous Conversion Using External Clock

PARALLEL DIGITAL OUTPUT DATA

Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Complementary two's complement may be obtained by inverting MSB (pin 1). Table 1 shows the LSB, transition values and code definitions for each possible analog input signal range for 12-15 bits of resolution. The output data is CMOS compatible and the drive capability is 8 LSTTL loads. If long digital lines have to be driven, external output buffers are recommended.

SERIAL DIGITAL OUTPUT DATA

Serial data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. It is CMOS compatible and has a drive capability of 8 LSTTL loads. At the first low to high transition of the A/D clock, serial out is set to "1" (See Figure 1). The digital word becomes available (bit by bit MSB first) 30nS maximum after the low to high transitions of the clock (Figure 9).

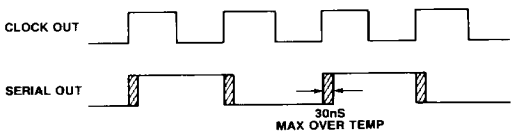


Figure 9. Serial Data to Clock Relationship

INPUT SCALING

The HS 9576 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table 3.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
± 10V	COB or CTC*	27	Input Sig.	24
± 5V	COB or CTC*	27	Open	25
± 2.5V	COB or CTC*	27	Pin 27	25
0 to + 5V	CSB	22	Pin 27	25
0 to + 10V	CSB	22	Open	25
0 to + 20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1). Parallel output data only.

Table 3. HS 9576 Input Scaling Connections

CONNECTIONS AND CALIBRATION PROCEDURE

(14-Bit Resolution Example)

Figures 10 and 11 show the different analog and power connections required for unipolar 0 to 10V and bipolar − 10V to + 10V input range operation.

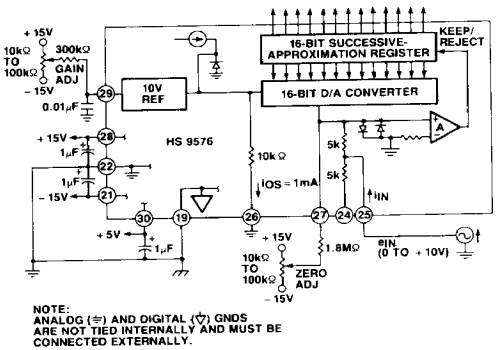


Figure 10. Analog and Power Connections for Unipolar 0 to + 10V Input Range

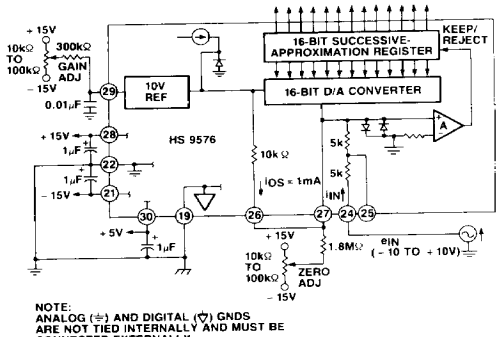


Figure 11. Analog and Power Connections for Bipolar + 10V to + 10V Input Range

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 10 & 11, are used for device calibration. To prevent interaction of these two adjustments, unipolar offset or bipolar zero is always adjusted first and then gain.

CALIBRATION FOR 0 TO +10V RANGE

Set analog input to +1 LSB_{14} = 0.00061V. Adjust ZERO for digital output = 11111111111110. ZERO is now adjusted. Set analog input to +FS − 2 LSB_{14} = 9.99878V. Adjust GAIN for 00000000000001 digital output code; GAIN is now calibrated. Half scale calibration check: set analog input to +5V; digital output code should be 011111111111111.

CALIBRATION FOR −10V TO +10V RANGE

(Complementary Offset Binary Code)

Set analog input to 0.00000V; adjust ZERO for 01111111111111 digital output code. Set analog input to 9.99756V (+FS − 2 LSB_{14}); adjust GAIN for 00000000000001 digital output code.

OTHER RANGES

Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5 V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table 1.

Unipolar offset or bipolar zero and full-scale calibrations can be accomplished to a precision of ± ½ LSB using the static adjustment procedure described above.

SAMPLE/HOLD REQUIREMENTS FOR THE HS 9576

Sample/hold amplifiers are normally used in front of A/D converters to hold the input voltage constant during conversion. Digitizing errors will result if the analog input signal varies by more than ½ LSB during conversion. In the case of the HS 9576, a 16-Bit A/D with a conversion time of 15 μsec to 14 bits, this results in a low input frequency which can be accurately digitized as explained below:

For a sine wave input, its maximum rate of change is calculated as $2\pi Af$ where f = frequency and A = amplitude. If one allows a ½ LSB change (0.6mV) during conversion for a ± 10V input swing to the A/D converter, the maximum rate of change limit would be 0.6mV/15 μsec, or 0.04mV/ μsec. Thus, the maximum sine wave input frequency that can be accurately digitized is calculated as:

$$0.04\text{mV}/\ \mu\text{sec} = 2\pi Af$$

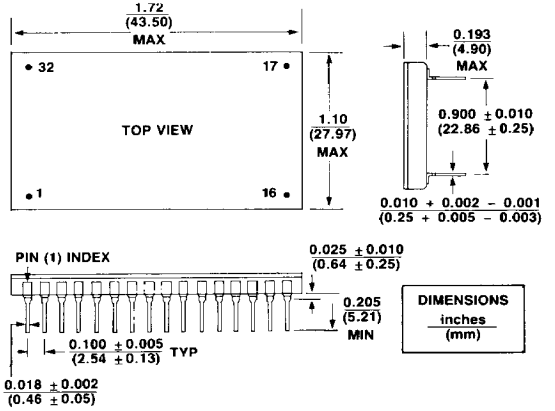
For a ± 10V input sine wave, this frequency limit is 0.63 Hz.

Expressed differently, the full scale bandwidth of the HS 9576 is slew rate limited to 0.63 Hz. By using a S/H, such as the HS 9716/9714 in front of the A/D this bandwidth can be significantly increased. The S/H will "freeze" an input signal that is changing too rapidly for the A/D alone to handle and hold it constant while the A/D performs a conversion. A S/H can accurately "freeze" signals moving as fast as ½ LSB during its aperture uncertainty (100 psec for the HS 9716/9714). Thus, for use with the HS 9576 to 14-Bit accuracy, the maximum rate of change limit would be 0.6mV (½ LSB, 14 bits, ± 10V swing) during 100 psec, or 6V/ μsec, which is the slew rate of the HS 9716/9714. Thus, the maximum full scale input frequency that can be accurately digitized is calculated as:

$$6\text{V}/\ \mu\text{sec} = 2\pi Af$$

For a ± 10V full scale input, this frequency limit is 95 kHz. Expressed differently, the full scale bandwidth of the HS 9576 has now been increased to 95 kHz with the use of the HS 9716/9714 S/H.

Throughput and the Nyquist criteria are other factors which will determine the highest input signal frequency that can be sampled. For the combination of the HS 9576 and the HS 9716/9714, the throughput is related to the sum of the conversion time of the A/D (15 μsec), the acquisition time of the S/H (5 μsec) and the hold mode (switching transient) settling time of the S/H (1 μsec). The total of 21 μsec represents a throughput of 47.6 kHz. Based on the Nyquist criteria of sampling more than twice per cycle, the highest input signal frequency that can be accurately digitized is slightly less than 23.8 kHz.



ORDERING INFORMATION

MODEL	MAX LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
HS 9576J	±0.006% FSR	0°C to +70°C	—
HS 9576K	±0.003% FSR	0°C to +70°C	—
HS 9576S/B	±0.006% FSR	−55°C to +125°C	MIL-STD-883C
HS 9576T/B	±0.003% FSR	−55°C to +125°C	MIL-STD-883C