Headland
Technology Inc

PRELIMINARY

GC113
Advanced Memory Manager

T-52-33-25

FEATURES

- **Page Mode and 2 or 4-Way Interleave support**
- **0 effective (0.4 to 0.6) Wait States using 100ns DRAM's**
- **EMS Page Write Protect**
- **EMS Dual Context Support**
- **EMS Auto Increment**
- **2 Sets of 32 EMS Registers**
- **Supports up to 8MB of on-board system memory**
- **Supports Shadow RAM for Video and System BIOS**
- **Supports 256K or 1M DRAMs**
- **Operates with the 286 or 386SX chip set.**
- **Pin Compatible with GC103 EMS Controller**
- **HCMOS Technology**

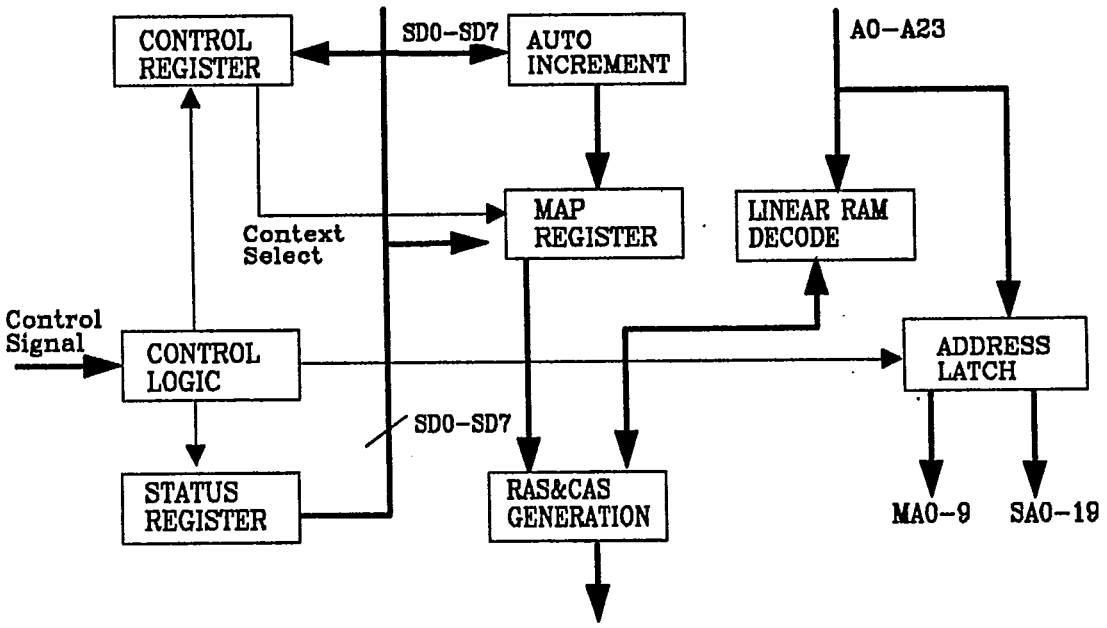
DESCRIPTION

The GC113 is an advanced highly integrated page interleave memory controller that operates with the 386SX or 286 chip sets. The use of high performance CMOS technology and advanced packaging techniques provide the highest performance possible. This device, when used with the GC101SX and GC102 (386SX) or GC101 and GC102 (286) forms a complete high performance chip set. EMS 4.0 support and memory interleave functions operate with minimal critical timing delays, features not possible with other low cost solutions.

The GC113 provides hardware support for EMS 4.0 and both 2-Way and 4-Way memory interleave. The EMS 4.0 hardware support has dual sets of 32 registers and full context support for the highest possible performance local memory accesses. Advanced EMS hardware write-protect has been added for maximum EMS 4.0 compatibility. The GC113, with the GC101SX/GC102 and GC101/GC102 chip sets, support up to 8MB of on-board memory as well as Shadow RAM for System and Video BIOS. Minimal support logic is required for a complete high performance AT compatible system.

The GC113 also provides address buffering for the expansion bus, local I/O bus, and on-board DRAM memory. Control logic for DMA, Address, and Refresh control are provided for a complete hardware solution for your needs. This device is packaged in a 160 pin quad flat pack.

Chip Block Diagram



Headland Technology is changing part number designations from GC to HT. Printed materials and schematics may not be updated concurrently; in the interim chips may be referenced as either GC or HT.

The EMS Auto-Increment capability provides your application with the capability to emulate multiple contexts for use with advanced multi-tasking requirements. This capability provides a high performance solution for those applications that require high speed block move capability.

Advanced Memory Management

The hardware design of the GC113 utilizes advanced main frame techniques such as two or four way interleaving along with high speed page mode capability. The hardware has been optimized to allow mixing of DRAM types to give your end user the maximum flexibility in choosing the correct DRAM capacity for their application. The GC113 supports 64K, 256K and 1Meg DRAM's in the configurations shown in the Table Below.

Extensive Hardware support has been integrated into this device to support multiple Shadow RAM address relocation. When the split feature is active all memory is relocated upward by 384K. As an example when the system memory capacity is 1MB the 384K would be found between the address range of 1Meg to 1.384MByte.

Interleave

Interleave is enabled when an even number of Banks are installed and the DRAM Bank pairs are of the same type. If bit 1 of Control Register is set to 0 (default), word interleave will be selected. Page interleave will be selected if bit 1 is set to 1.

Refresh

A refresh cycle starts by performing a RAS precharge cycle for all banks of RAM. This is followed by staggered RAS-only refresh cycles. The page registers are reset. The first memory cycle to any bank following a refresh is always a page miss.

DMA or Bus Master

The RAS and CAS timing for the DRAM are generated from the delay lines and the page mode sequencers are reset. The first memory cycle to any bank following a DMA or Bus Master cycle is a page miss.

PIN NAME				TYPES OF DRAMS INSTALLED				TOTAL	
RAM1M	1MMIX	RAMSW2	RAMSW1	BANK0	BANK1	BANK2	BANK3	Interleave	MB
Off	Off	Off	Off	256K	None	None	None	0	512K
Off	Off	Off	0n	256K	256K	None	None	2	1M
Off	Off	On	Off	256K	256K	256K	None	0	1.5M
Off	Off	On	On	256K	256K	256K	256K	4	2M
Off	On	Off	Off *	256K	64K	None	None	0	640K
Off	On	Off	On	256K	256K	None	None	2	1M
Off	On	On	Off	256K	256K	1M	None	0	3M
Off	On	On	On	256K	256K	1M	1M	2	5M
On	Off	Off	Off	1M	None	None	None	0	2M
On	Off	Off	On	1M	1M	None	None	2	4M
On	Off	On	Off	1M	1M	1M	None	0	6M
On	Off	On	On	1M	1M	1M	1M	4	8M
On	On	Off	Off	1M	None	None	None	0	2M
On	On	Off	On	1M	1M	None	None	2	4M
On	On	On	Off	1M	1M	256K	None	0	4.5M
On	On	On	On	1M	1M	256K	256K	2	5M

*SPLSW must be On.
On - pin grounded
Off - pin not grounded

EMS and Address Buffering

The GC113 EMS Controller provides the necessary control to buffer the addresses of the A, SA, XA, LA, and MA buses (see figure on Page 5). It also includes all the logic necessary for a hardware implementation of the Expanded Memory Specification. The DMAAEN and CPUHLDA signals control direction of the Address bus (A) flow; between the CPU, the Slot expansion (SA) bus and XA Bus. The Memory Address (MA) bus is generated by multiplexing the expansion (SA) bus with the ADRSEL and /REFRESH.

EMS Address Translation

On power up the EMS function is disabled, all the DRAM addresses are left as flat linear addresses; ie without any EMS translations. An internal Linear Address Decoder accessses the lower 0-640K and 1 Meg and above -- to the upper limit of the system's memory. The top of the linear address space is defined by 5 switch settings. These switches (RAMSW1, RAMSW2, 1MMIX, SPLIT and RAM1M) determine the number of RAM banks connected to the GC113. When the switches are left floating, bank selection can be controlled in software; where bits D5 and D6 of the Map Register (1EC) determine the number of banks.

A second I/O register selects the EMS pages; with the address space from 256K(40000) to 640K(A0000) and from 768K(C0000) to 896K(E0000) being decoded as 32 pages. To get 64K of program memory, four contiguous pages are required. The EMS pages are accessed through the Map Address Register located at I/O address 1EE (hex); which is a read/write register.

Register Summary

The GC113 contains three internal EMS registers, all accessed via I/O operations, all read/writable. They are the Map Address Register (MAR) at 1EE, the Control Register (CR) at 1EF, and the Map Register (MR) at 1EC. The first two registers are 8 bits wide (I/O byte operations); the Map Register is 10 bits wide and thus requires I/O word accesses.

During I/O cycles, the MAR (1EE) provides a 6-bit address to the Map Register (a 64x10 Static RAM). This selects the register for programming or reading the maps. Writing data to the MR (1EC) programs the RAM, and that data becomes the upper most address bits (translated A14-A19) when addressing DRAM in EMS operation. By selecting the auto-increment operation of the MAR, you can write once to MAR, and follow that with 64 writes to MR and fully program the RAM pages with the address translations. This programs both the standard and alternate context maps.

During memory cycles, address pins and a single bit from the CR (1EF) provide the 6-bit address to the Map Register (1EC). The MR then puts its programmed data onto the system's external DRAM address lines. After this summary concludes, there is a bit-by-bit description of these three registers.

The Map Register contains two sets of 32 registers; used as standard context maps and alternate context maps. This allows two programs to maintain separate and simultaneous register mappings, so switching between two programs is practically instantaneous. In systems with only a single set of 32 registers, when a second program needs to perform EMS operations, it must save the current mapping and then write it's own maps before starting. This requires time, and data may be lost in fast-moving communications programs. The two sets of 32 registers in the GC113 alleviate this problem.

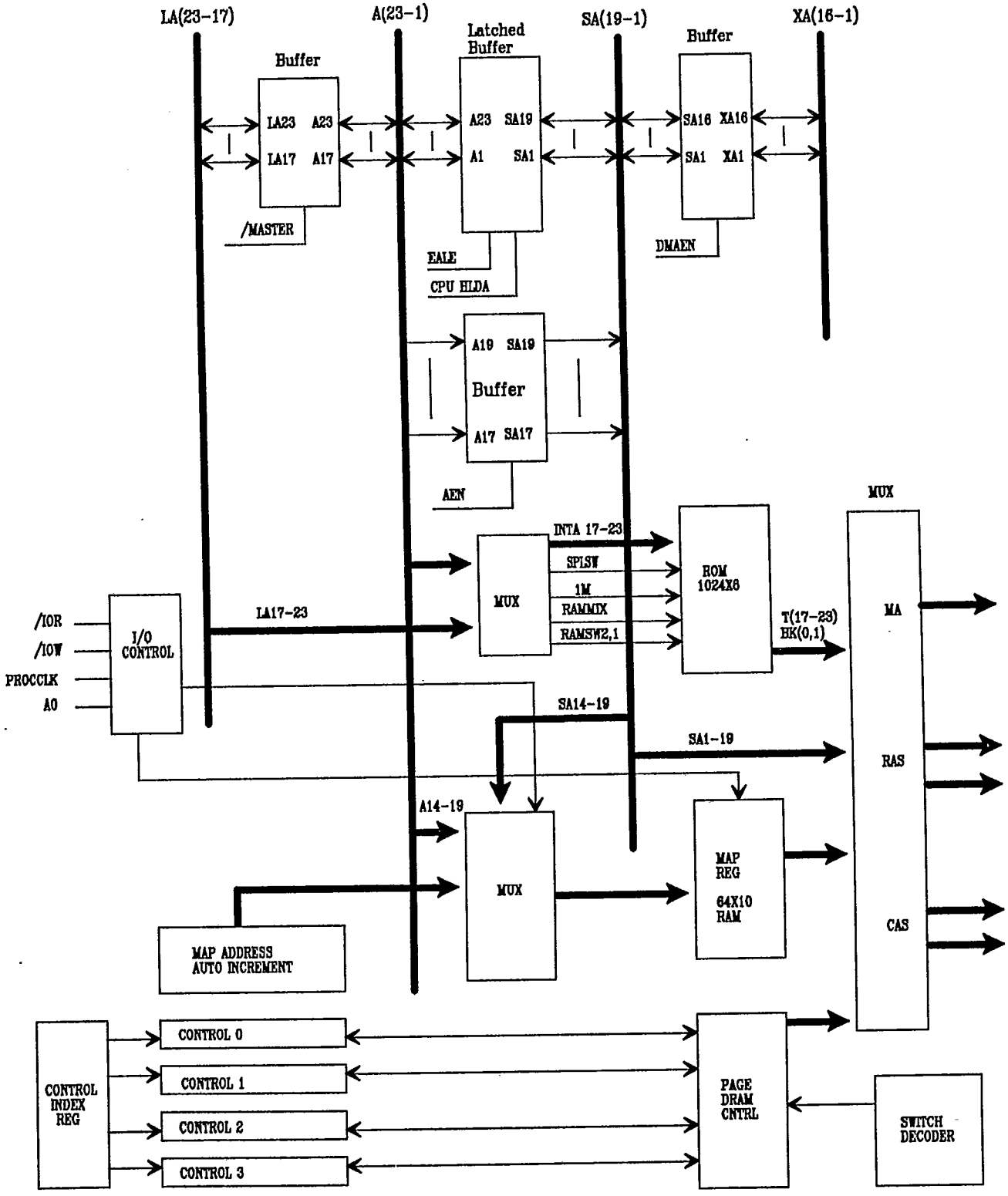
For I/O cycles, the MAR (1EE) page bits (D0-D4) select 1 of 32 registers, and its Context bit (D5) selects between the two pairs of 32 registers. 0 selects the standard context maps, and 1 selects the alternate context maps. These six bits drive the address lines of the 64x10 RAM, or Map Register. An additional bit determines whether auto-incrementing is enabled (D7). If enabled, when a count of all ones is reached on D0-D6, D7 is cleared and auto-incrementing ceases.

For the memory cycles, 6 address pins select pages among the 32 registers. The address pins are either A14-A19 or SA14-SA19, depending upon whether the CPU has control of the system or not. As with I/O cycles, there is a Context bit to select between the 2 sets of 32 registers. D0 of the Control Register (1EF) provides context information; a 0 selects the standard context maps.

The MR outputs 10 lines, the 7 least significant provide DRAM addresses, the next two perform bank selection and thus generate RAS0-RAS3, and D9 is for bank enable. When EMS memory accesses occur, A0 to A13 are passed unfiltered to the DRAM. A14 to A19 are redirected to the MR as addresses, and the Map Register outputs the translated addresses on its D0-D6 lines. (The smaller 256k DRAM uses only D0-D4 outputs.)

Four other bits within the CR, D7-D5 and D2, are software switches to select DRAM type (1M vs 256k DRAM), bank count, and extra 384K disable. The same functions can be controlled by grounding four pins on the GC113, respectively: 1MRAM, RAMSW2 and RAMSW1 and SPLIT. The full EMS register descriptions follow.

GC113
Block Diagram



GC113
Page Size

Page Size

4 Way Interleave

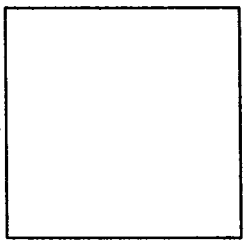
256K	256K	256K	256K	Device Type
4 X 1024 Bytes				
4096 Bytes				

1Meg	1Meg	1Meg	1Meg	Device Type
4 X 2048 Bytes				
8192 Bytes				

Typical DRAM Organization

CAS 1024

RAS 1024

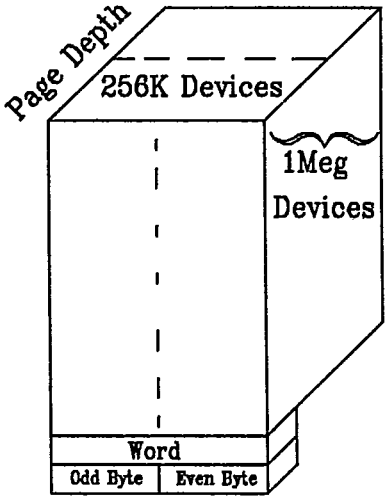


1 Meg DRAM

Page Size

1024 X 16 Bits
= 1024 Word's
= 2048 Bytes

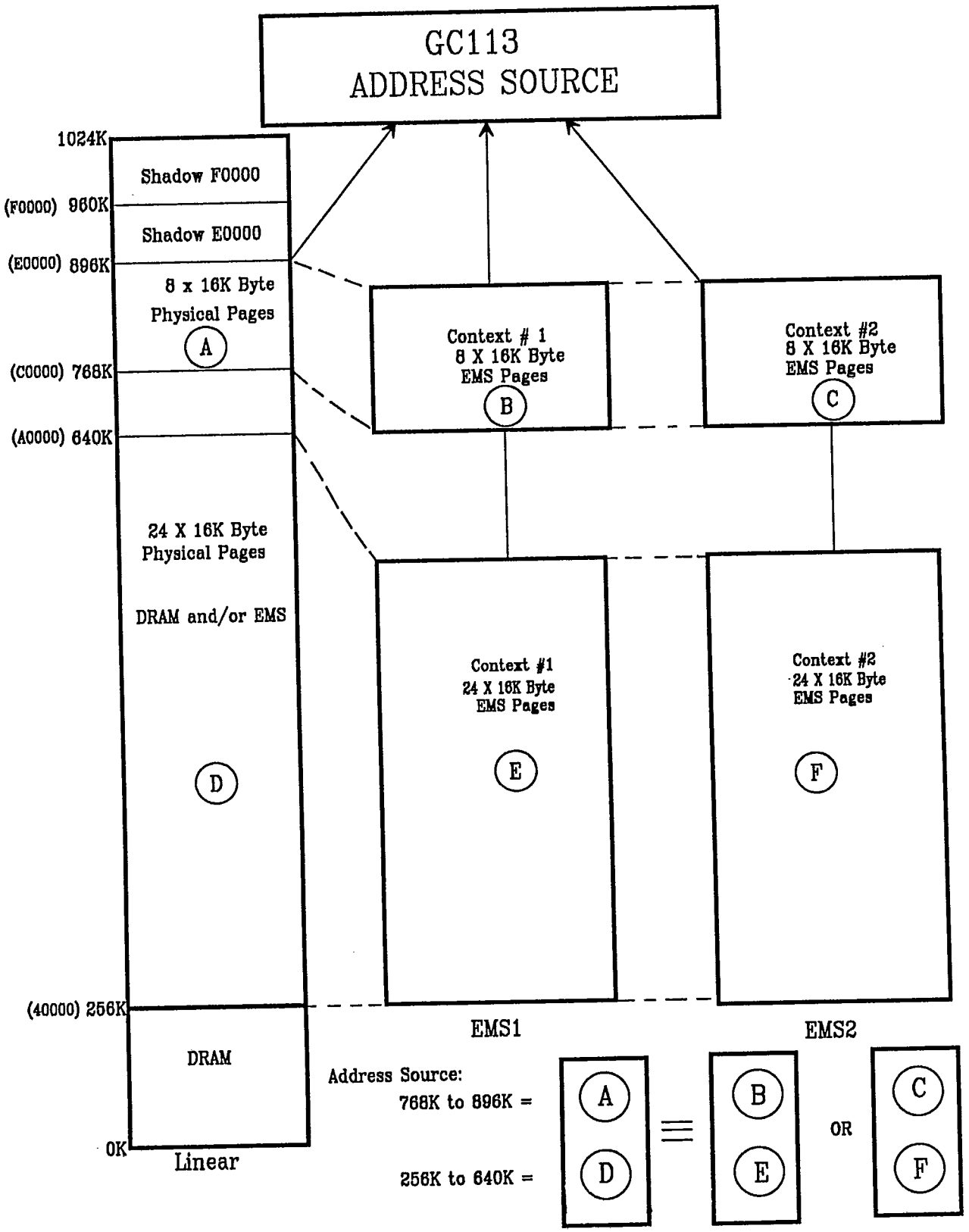
Page Description



256K DRAM

Page Size

GC113
Memory Map



MAP ADDRESS REGISTER 8 R/W bits, at I/O address 1EE (hex) Reset State: 0	
D7	Auto-increment Enable Bit
D6	EMS Page Write Protect
D5	Context Selection
D4-D0	Page Selection 1 page (or more) of 32

D7: Auto-increment, Enable

When 1, each read or write of the Map Register (1EC) increments the count on D7-D0. These bits can be treated as a 8-bit counter, which auto-increment under D7 control. The counter consists of Auto-increment Enable (D7), Carry (D6), Context Selection (D5), and Page Address bits (D4-D0). When the count reaches all 1's (FF), the Enable bit is set to zero and auto-incrementing is turned off until another 1 is written to D7.

By initializing the counter to 80 hex (auto-incrementing on, carry off, standard context, and page 40,000 hex) the maximum number of automatic accesses is available. 32 standard-context writes are followed by 32 alternate-context write s; bringing the count to C0. Then, 32 reads in each context would increment the counter to 00. The 64th read clears the auto-incrementing enable (D7), and prevents further increments until D7 is manually set back to 1.

D6: EMS Page Write Protect

With D6 = 0, Do not write protect the selected page when data is written to the Map Register to select the physical memory to map into this EMS page.

With D6 = 1, Write protect the selected page when data is written to the map register to select the physical memory to map.

D5: Context Selection

When 0, standard context is the default
When 1, alternate context

The GC113 contains two sets of 32 registers, each maps to different available pages. Bit D5 switches between the two sets of registers during I/O cycles. (CR's D0 is context selection during memory cycles.) This allows one program to access its 32 mapping registers (standard context), and a second program has an alternate set of register maps (alternate context). With two pairs of registers available, changing between two programs is almost instantaneous, and data integrity is maintained. D5 selects the active set of map registers during I/O EMS cycles.

D4-D0: Page Selection

Page selection is determined by these 5 bits. Once latched in the MAR, with incrementing enabled, they generate the address lines to the Map Register for I/O cycles. Select the appropriate page(s) by setting D4-D0 according to Table 1 below. A minimum of 4 contiguous 16k pages must be selected for EMS operation. (EMS requires a Page Frame size of 64K or more, thus four 16K pages.) Note that page addresses are presented in the table below as both hexadecimal and decimal numbers.

Hexadecimal Page Address	Decimal Page Address	Register 1EE Bits D 4	DDDD 3210
DC000-DFFFF	880 - 896K	1	1111
D8000 -	864 -	1	1110
D4000 -	848 -	1	1101
D0000 -	832 -	1	1100
CC000-CFFFF	816 - 832K	1	1011
C8000 -	800 -	1	1010
C4000 -	784 -	1	1001
C0000-C3FFF	768 -	1	1000
....	....	...	....
9C000-9FFFF	624 - 640K	1	0111
98000 -	608 -	1	0110
94000 -	592 -	1	0101
9000 -	576 -	1	0100
8C000-8FFFF	560 - 576K	1	0011
88000 -	544 -	1	0010
84000 -	528 -	1	0001
80000 -	512 -	1	0000
7C000-7FFFF	496 - 512K	0	1111
78000 -	480 -	0	1110
74000 -	464 -	0	1101
74000 -	464 -	0	1101
70000 -	448 -	0	1100
6C000-6FFFF	432 - 448K	0	1011
68000 -	416 -	0	1010
64000 -	400 -	0	1001
60000 -	384 -	0	1000
5C000-5FFFF	368 - 384K	0	0111
58000 -	352 -	0	0110
54000 -	336 -	0	0101
50000 -	320 -	0	0100
4C000-4FFFF	304 - 320K	0	0011
48000 -	288 -	0	0010
44000 -	272 -	0	0001
40000-43FFF	256 - 272K	0	0000
(4000 increments hex	16K increments) decimal		

MAP REGISTER 10 R/W bits, at I/O address 1EC (hex) Reset State: 0	
D9	Map Enable
D8-D7	Bank Select
D6-D5	1M DRAM Address Bits
D4-D0	1M/256k DRAM Address Bits

D9: Map Enable

When the Global EMS Enable bit in Control Register 0 is a 1, the Map Enable bit associated with each 16K page acts as an individual page mapping enable. If Map Enable is a 1, then its corresponding page is remapped by the GC113. If the Map Enable bit is 0, the CPU address lines are passed through untranslated. If the Global EMS Enable bit is a 0, all address remapping is turned off regardless of the state of the individual Map Enable bits.

D8-D7: Bank Select

For 1M/256K, selection as follows:

D8	D7	
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

D6-D5: Translated address 1M DRAM types

D4-D0: Translated address bits for 256K/1M DRAM type

CONTROL REGISTER INDEX 8 R/W bits, at I/O 1ED (hex) Reset State: 0	
D7-D3	Reserved
D2-D0	Control Register Select at 1EF (hex)

D7-D3: Reserved:

Write as zero.

D2-D0: Control Register Select

D2	D1	D0	
0	0	0	Control Register 0
0	0	1	Control Register 1
0	1	0	Control Register 2
0	1	1	Control Register 3
1	0	0	Control Register 4

Control Register 0 8 R/W bits, at I/O address 1EF (hex) Reset state: all 0's	
D7	RAM-type Override
D6-D5	Bank-count Override
D4	Shadow Enable F0000 and FF0000
D3	Shadow Enable E0000 and FE0000
D2	Extra 384k Disable
D1	Global EMS Enable
D0	Context Selection

D7: RAM-type Override

If RAM1M (input pin 36) is not connected to ground, then this register can be written to select the RAM type. If a switch is connected to this pin, then this setting can be read back (sense inverted) on this bit.

Type of RAM

0 off 256K (default)
1 on 1M

off - pin not grounded
on - pin grounded

D6-D5: DRAM Bank-count Override

If pins RAMSW1 and RAMSW2 are not used, then this register can be used to program the number of banks installed under BIOS control. The READ back of these bits is the register value or'd with the switches attached to the pins RAMSW1 and RAMSW2.

D6	D5	RAMSW1	RAMSW2	default # of RAM Banks enabled	Interleave Mode
0	0	Off	Off	1	0
0	1	On	Off	2	2
1	0	Off	On	3	0
1	1	On	On	4	4

D4: Shadow Enable Page F0000 and FF0000

64K page of RAM that would have been located from F0000 to FFFFF in ROM is now enabled in RAM between F0000 to FFFFF and is duplicated at FF0000 to FFFFFF. The ROM chip select will now be disabled. Data should be written to this RAM before enabling this bit. Access to this memory requires the following EMS pages be reserved for shadow ram use:

256K RAMs Installed Hi/Low Byte	1M RAMs Installed Hi/Low Byte
02 9C	02 3C
02 9D	02 3D
02 9E	02 3E
02 9F	02 3F

Note: RAM is write protected in this RANGE and is READ only.

D3: Shadow Enable page E0000 and FE0000

The 64K page of RAM that would have been located from E0000 to EFFFF in ROM is now enabled in RAM between E0000 and EFFFF and is duplicated at FE0000 to FEFFFF. The ROM chip select will now be disabled. Data should be written to this RAM before e nabling this bit. Access to this memory requires the following EMS pages be reserved for shadow ram use:

256K RAMs Installed Hi/Low Byte	1M RAMs Installed Hi/Low Byte
02 98	02 38
02 99	02 39
02 9A	02 3A
02 9B	02 3B

Note: RAM is write protected in this RANGE and is READ only.

D2: Extra 384K Disable.

If the SPLSW (input pin 19) is floating, this register bit disables/enables the 384k. A 1 written to D2 disables the extra 384K, a 0 enables it. If the SPLSW IS grounded, the extra 384K is disabled.

Normally the 384K address range, located between A0000 and 1 Meg, is relocated above the 1M border. This preserves the lower addresses for system use. With the SPLSW floating and D2=1, the relocated 384K is disabled and usable as shadow RAM or as EMS. When this bit is read back, the result is D2 OR'D with the inverse of SPLSW.

D1: Global EMS Enable

If D1 = 1, EMS memory is enabled. You must initialize the EMS registers before D1 is set high.

D0: Context Selection

If D0 = 0, the standard context is selected; if 1, the alternate context. This bit operates in the same manner as bit D5 of Register 1EE, except this determination of context is used during Memory cycles.

CONTROL REGISTER 1 8 R/W bits, at I/O address 1EF (Hex) Reset State: 0	
D7	Page Mode Enable
D6	Mix DRAM Type
D5-D3	RAS Precharge timing
D2-D0	RAS Active Timeout

D7: Page Mode Enable

0	Page mode disabled, uses delay line timing for normal memory access.
1	Page mode enabled, uses synchronous memory timing except during DMA and bus master.

D6: Mix Dram type Mode Register

D6	Pin	Mix	Memory Type
0	1	open	Same type all four banks
1	0	grounded	Selected type first 2 banks, other type last two banks. Special CASE when 256K DRAMs, selected and only 1 bank is selected allows the use of 256K DRAMs in the first bank and 64K DRAMs in the second bank for a total of 640K RAM.

D5-D3: RAS Precharge Timing

D5	D4	D3	PROCCLK Cycles
0	0	0	16
0	0	1	14
0	1	0	12
0	1	1	10
1	0	0	8
1	0	1	6
1	1	0	4
1	1	1	2

D2-D0: RAS Active Timeout

D2	D1	D0	PROCCLK Cycles
0	0	0	1080
0	0	1	960
0	1	0	840
0	1	1	720
1	0	0	600
1	0	1	480
1	1	0	360
1	1	1	240

Values can be adjusted to provide nominal values near 10 usec for any speed system configuration. A speed timing routine or preset system speeds are required to determine the correct value. All timing is based on a fixed PROCCLK signal. If changes are made to PROCCLK, then register value changes may be required to compensate.

CONTROL REGISTER 2 8R/W bits, at I/O address 1EF (Hex) Reset State: 0	
D7-D6	Reserved
D5-D4	Page Mode
D3-D2	CAS Precharge Time
D1-D0	CAS Active Time

Values are adjustable to provide values for most all DRAMs at any speed and configuration. All timing is based on a fixed PROCCLK signal. If changes are made to the PROCCLK signal, adjustments may be required to this register to compensate. DD Hex is the recommended value for 80386SX or 80286 0-wait state operation. C8 Hex should be used for 1-wait state 386SX systems while CC Hex should be used for 1-wait state 286 systems.

D7-D6: Reserved

These 2 Bits must be set to 1 in order to execute operations properly.

D5-D4: Page Mode

D5	Non-page mode zero wait state enable (valid when D7 of Control Register 1 is set to 0)
0	1 Wait state memory operation
1	Assert zero wait state all non-page mode memory cycles
D4	Page mode zero wait state enable (valid when D7 of Control Register 1 is set to 1)
0	Page mode operation with 1 wait state
1	Page mode operation with zero wait state when page hit

D3-D2: CAS Precharge Time

D3	D2	PROCCLK cycles
0	0	4
0	1	3
1	0	2
1	1	1

D1-D0: CAS Active Time

D1	D0	PROCCLK cycles
0	0	4
0	1	3
1	0	2
1	1	1

CONTROL REGISTER 3 8 R/W bits, at I/O Address 1EF (Hex) Default Memory Size (A23-A16)	
D7-D0	External Expansion RAM

D7-D0: External Expansion RAM

Top of Memory from 0 to 255 number of 64K segments before expansion memory should be decoded. For example 0 would indicate that all system board RAM should be disabled for all but EMS and shadow. After reset, GC113 checks the 5 switches set up (RAM1M, 1MMIX, SPLSW, RAMSW2 and RAMSW1) to determine the on board memory size and load the maximum on board address (A23-A16) to (D7-D0) on this register.

Control Register 4 8 R/W bits, at I/O Address 1EF (Hex) Reset State: 0	
D7-D2	Reserved
D1	Interleave
D0	Reserved

D1: Interleave Mode

0	Word Interleave
1	Page Interleave

D0: Reserved

This Bit must be set to 0.

GC113
Interleave Addressing

The memory address multiplexers provide the proper address for the memory array. There are two types of interleaving available, word and page interleaving. When Control Register 4 is selected, bit D1=0 will select Word Interleave, bit D1=1 will select Page Interleave. Note: Interleaving can only occur when an even number of banks of memory have been installed on the system board.

Word 2-Way and 4-Way Interleaving selects the proper bank of memory by applying the proper /RAS and /CAS signal as selected by the RASA and RASB bits defined in the chart.

BK=Bank A=Address T=Translated Address (Bank and Translated Address are from A14-A23.

WORD INTERLEAVE												
		RASA	RASB	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9
Memory Type 256K				(Mixed with 1M or Not)									
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A1	BK1	A10	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			BK0	A11	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A1	A2	A10	A11	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			BK0	BK1	A12	A13	T14	T15	T16	T17	T18	T20
Memory Type 1M				(Only)									
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A1	BK1	A11	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			BKO	T19	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A1	A2	A11	A12	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			BK0	BK1	T19	A13	T14	T15	T16	T17	T18	T20
256K with 64K				(Maximum Memory 640K)									
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	T17	T19
	RAS			A10	A11	A12	A13	T14	T15	T16	A9	T18	T20
Refresh													
N/C	RAS			A1	A2	A3	A4	A5	A6	A7	A0	A8	-

GC113
Interleave Addressing

Page Interleave is accomplished in a similar manner to previously shown inteleaving. The Page interleave chart showing the RASA and RASB signals and address translation is shown below. In Page Interleave mode, only 256K and 1Meg devices are supported. 256K devices will result in a 4K Page Size and 1Meg devices will result in a 8K page size.

PAGE INTERLEAVE

		RASA	RASB	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9
Memory Type 256K				(Mixed with 1M or Not									
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A11	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	BK0	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A11	A12	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS			A10	BK0	BK1	A13	T14	T15	T16	T17	T18	T20
Memory Type 1 M				Only									
0	CAS	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	A11	A12	A13	T14	T15	T16	T17	T18	T20
2	CAS	A11	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	BK0	A12	A13	T14	T15	T16	T17	T18	T20
4	CAS	A11	A12	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS			T19	BK0	BK1	A13	T14	T15	T16	T17	T18	T20

4 BANKS 1M Devices

4 Way Interleave

DRAM 1 MWord (16 1M devices + 2 Parity)	DRAM 1 MWord (16 1M devices + 2 Parity)	DRAM 1 MWord (16 1M devices + 2 Parity)	DRAM 1 MWord (16 1M devices + 2 Parity)

— 8 MByte

— 4 MByte

— OK

4 BANKS 256K Devices
4 Way Interleave

BANK 3	BANK 2	BANK 1	BANK 0
DRAM 512K Word (16 256K Devices +2 Parity)	DRAM 512K Word (16 256K Devices +2 Parity)	DRAM 512K Word (16 256K Devices +2 Parity)	DRAM 512K Word (16 256K Devices +2 Parity)
A2 = 1 = DBLWRD1		A2 = 0 = DBLWRD0	
16 Bit Word 3	16 Bit Word 2	16 Bit Word 1	16 Bit Word 0
Byte 7 | Byte 6	Byte 5 | Byte 4	Byte 3 | Byte 2	Byte 1 | Byte 0

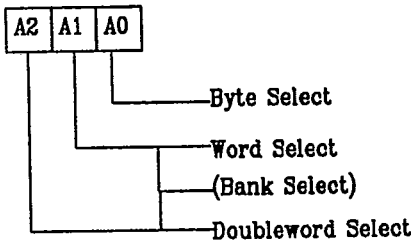
— 2 MByte

— 1 MByte

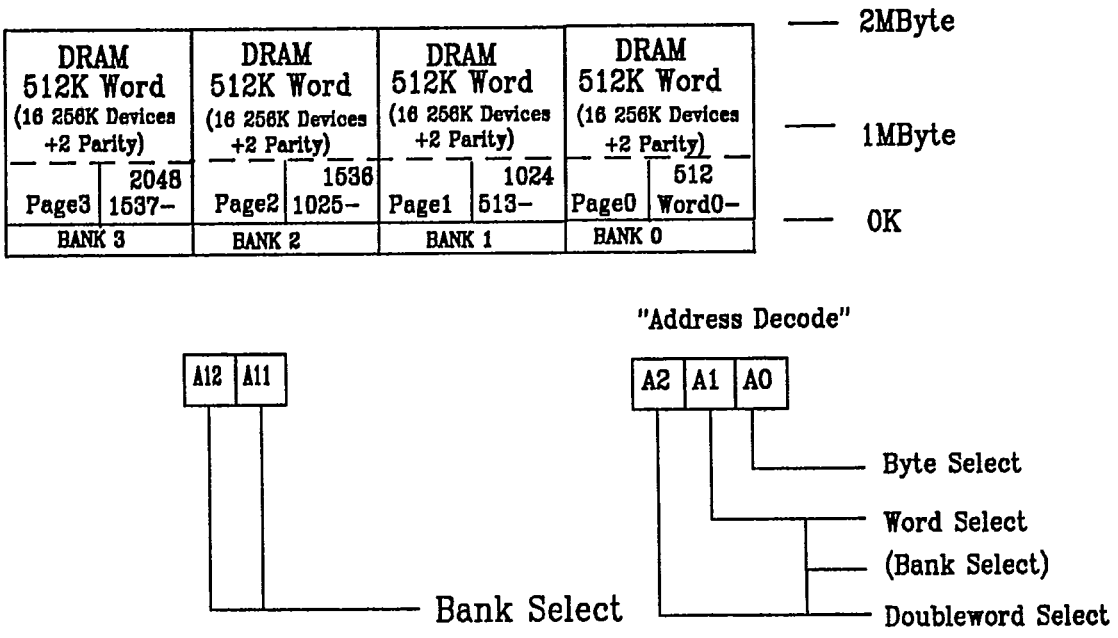
— OK

A1=Low=Even Word;A1=High=Odd Word
A0=Low=Even Byte;A0=High=Odd Byte

"Address Decode"

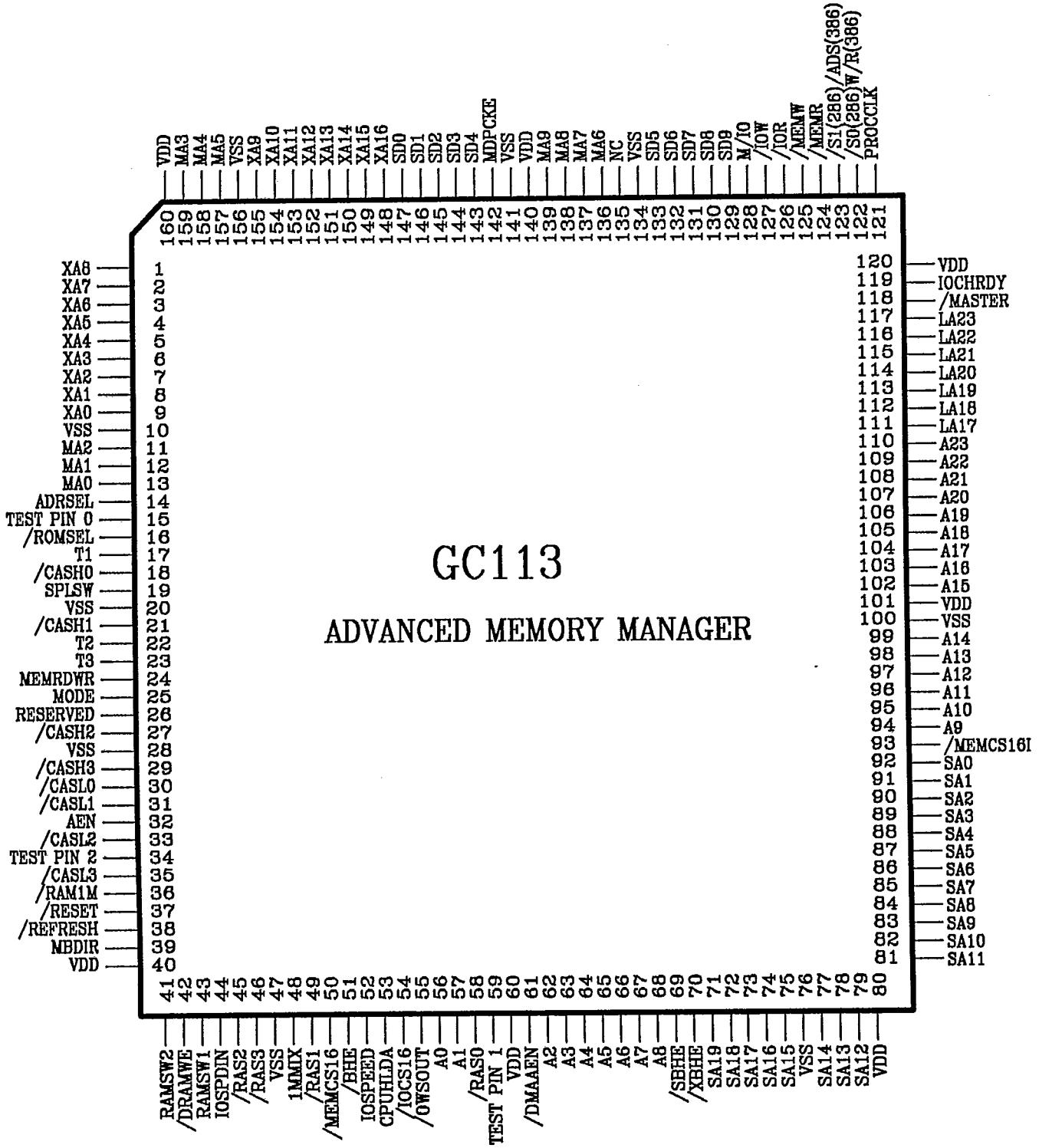


4 Way Word Interleave Addressing



4 Way Page Interleave Addressing

GC113
Pin Diagram



GC113
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
A0-A16	56,57,62-68,94-99,102-103	I	Address bits 0-16: Inputs from 80286 CPU or 80386SX. The GC113 takes the address bus inputs and generates SA bus for I/O slots, the XA bus for peripherals, and the MA bus for the system DRAM.
A17-A23	104-110	I/O	Address bits 17-23: Input lines from 80286 CPU or 80386SX CPU. During Bus Master operation from LA (17-23). See above.
ADRSEL	14	I	ADdrRss SELection: This input from off chip delay line determines when the RAS or CAS address of the Memory Address bus is output.
AEN	32	I	DMA Address ENable: When high, the DMA controller inside the GC101 controls the address and data buses, I/O read/write lines, and memory read/write signals.
/BHE	51	I	Byte High Enable: A low at this input enables the high-order byte of the D bus, D15-8.
/CASH0- /CASH3	18, 21, 27, 29	O	Column Address Strobe, High order byte: these control up to four banks of DRAMs. These signals can be connected directly to DRAM CAS input through a 22 Ohm series resister.
/CASL0- /CASL3	30, 31, 33, 35	O	Column Address Strobe, Low order byte: these control the four banks of DRAMs. These signals can be connected directly to DRAM CAS inputs through a 22 Ohm series resister.
CPUHLDA	53	I	CPU HoLD Acknowledge: The 80286 drives this input high to indicate that it has released control of its buses.
/DMAAEN	61	I	DMA Address ENable:. A low input indicates a DMA operation is in progress.
/DRAMWE	42	O	DRAM Write Enable: Generates the write strobe to DRAMs controlled by GC113. This is a gated signal derived from the /MEMW input.

GC113
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
IOCHRDY	119	O	I/O CHannel ReaDY: Held low by the GC113 to lengthen the cycles by an integral number of clock cycles. The GC113 will add more wait states for a page miss by pulling this signal low.
/IOCS16	54	O	IO Chip Select, 16 bits: Open drain output to indicate that the current I/O operation is a 16 bit operation. Input to the GC101.
IOSPDIN	44	I	I/O SPeeD INput: A low at this input indicates the system should run at lower speed at I/O cycles and off board memory.
IOSPEED	52	O	I/O SPEED: This output drives the GC101 IOSPEED pin. It indicates that the system clock is to be slowed down (1/2 speed) to accomodate off-board memory and peripherals. A high signal indicates half speed, a low - full speed.
/IOR	126	I	I/O Read: Input from the GC101.
/IOW	127	I	I/O Write: Input from the GC101.
LA17-23	111-117	I/O	Latched Address bits, 17-23: I/O addresses available on the AT expansion slots. Direction is controlled by the /MASTER input.
1MMIX	48	I	1M MIX: When low, indicates the system consists of mixed 256K and 1M DRAM.
MA0-MA9	13-11,159-157,136-139	O	Multiplexed Address bus: to DRAMs These signals should connect to the memory address of the DRAMs through 22 Ohm resisters.
/MASTER	118	I	Bus Master: Control signal from the AT expansion bus. When low, allows a peripheral on the expansion bus to have system control.

GC113
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
MBDIR	39	O	Memory Bus DIRection control: When high, data flows from the MD0-15 bus to the SD0-15 bus. When low, the data flow is reversed. RAM and ROM data is transmitted on the MD bus.
MDPCKE	142	O	Memory Data Parity Check Enable: A high on the pin enables the parity checking logic of the GC102 data buffer and indicates on-board memory is being accessed. The memory range in which this signal is active depends on the RAM select switches and register contents.
/MEMCS16	50	I	MEMory Chip Select, 16 wide: External devices drive this input low for 16-bit data transfers. In turn, the GC113 sets it's output pin /MEMCS16I low, alerting the GC101 of the 16-bit transfer. Connects to the system expansion bus.
/MEMCS16I	93	O	MEMory Chip Select Internal, 16-bits: A low on this output alerts the GC101 that the current memory access is 16 bits wide. The polarity of this output is controlled by the level on the input pin /MEMCS16 and the memory range selected in the GC113. A low at that input, forces this output low.
/MEMR	124	I	MEMory Read: A low from GC101 indicates a read is in progress.
MEMRDWR	24	O	MEMory ReaD or WRite cycle: to delay line input
/MEMW	125	I	MEMory Write: A low from GC101 indicates a write cycle.
M/IO	128	I	Memory or I/O status from 80286/80386SX CPU
MODE	25	I	"0" = 386SX, "1" = 286 Used to select 286 or 386SX operation.
PROCCLK	121	I	PROCcessor CLocK: Internal system clock. Driven by GC101.

GC113
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
/RAM1M	36	I	RAM 1 Megabyte: Tie this input to Ground, for 1 Megabyte DRAM. Connect the input to VCC for 256K byte DRAM.
RAMSW1, RAMSW2	43, 41	I	RAMSW1 / RAMSW2 / DEFAULT # OF BANKS INSTALLED VCC / VCC / 1 ground / VCC / 2 VCC / ground / 3 ground / ground / 4 If these pins are floating, Register 1EC, bits D6 and D5 define the number of banks installed. See the register description section for more details.
/RAS0-/RAS3	58,49,45,46	O	Row Address Strobe: RAS selection for 4 banks of DRAM
/REFRESH	38	I	Refresh: Input from the GC101 is low when the current cycle is a memory refresh.
/RESET	37	I	RESET: A low from the GC101 resets internal logic.
/ROMSEL	16	O	ROM SELect: A low enables signals to the BIOS ROMS or EPROMS
SA0	92	I	System Address bit 0: Address input from GC101
SA1-SA19	91-81, 79-77, 75-71	I/O	System Address bus: Bi-direction bus to/from the PC expansion slot.
/SBHE	69	I/O	System Byte High Enable: Low when peripherals are performing a transfer on the upper byte.
SD0-SD9	147-143, 133-129	I/O	System Data bus: to/from PC bus

GC113
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
SPLSW	19	I	Enable last 384K section of RAM SPLIT = 0 Extra 384K section disable SPLIT = 1 Extra 384K section enable If this pin is floating, Register 1EF, bit D2 determines whether the additional 384K of RAM is enabled. See register description section..
/S0-W/R, /S1-/ADS	122,123	I	Inputs /S0, /S1 from the 80286 CPU (MODE=1). Inputs W/R , /ADS from the 80386 CPU (MODE=0)
T1,T3	17, 23	I	Time Delays: MEMRDWR is the input to a delay counter. The counter generating successively longer delays called ADRSEL, T1, T2 and T3 respectively. Used for CAS input timing.
T2	22	I	Connects to ground to select external delay line.
XA0	9	I	External Address 0: This input from the GC101 enables low byte transfers between the SD and MD buses.
XA1-XA16	8-1, 155-148	I/O	External Address: bus to/from the GC101
/XBHE	70	I/O	EXternal Byte High Enable: Low when peripherals are performing a transfer on the upper byte.
/0WSOUT	55	O	Zero Wait State OUTput to the GC101 indicates the current memory access should not have any wait states inserted.

GC113
Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
VDD	40, 60, 80, 101, 120, 140,160		Power pins
VSS	10,20,28,47,76,100, 134,141,156		Ground Power Pins
NC	26, 135		No Connection
TEST PIN 0,2	15,34	O	Test Pins
TEST PIN 1	59	I	Test Pin for disabling all tri-state outputs. This pin should be connected to ground for normal operation.

GC113
DC Characteristics

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC Input Current	IIN	+10	mA
Storage Temperature Range (Plastic)	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	unit
DC Sypply Voltage	VDD	+3 to +6	V
Operating Ambient Temperature Range Commercial	TA	0 to +70	C

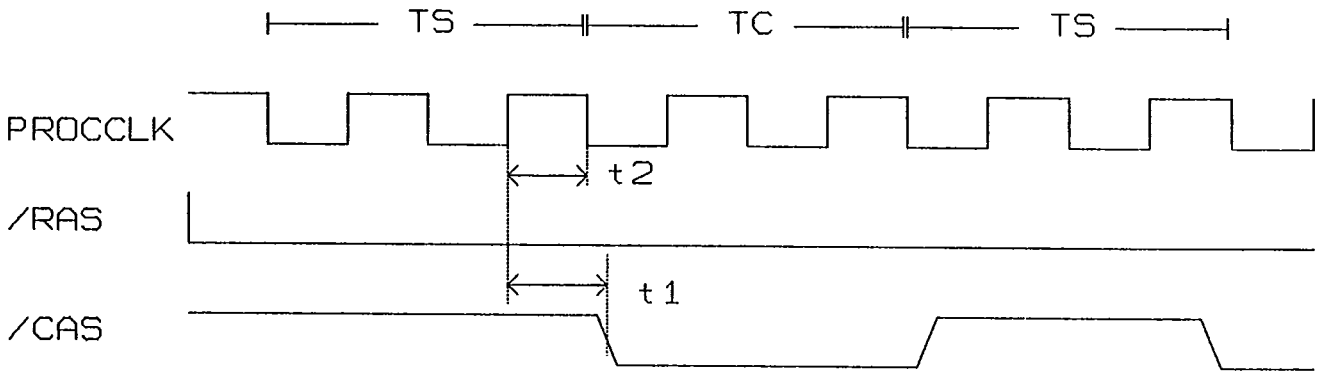
DC Characteristics: VDD = 5V +/- 5%, TA = 0 C to 70 C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input LOW	VIL				0.8	V
Voltage Input HIGH	VIH		2			V
Input Current	IIN	VIN = VDD or VSS	-10	+1	+10	uA
w/internal pulldown		VIN = VDD	10	35	120	uA
w/internal pullup		VIN = VSS	-100	-30	-8	uA
Voltage Output High /RAS0-3,//DRAMWE,MA0-9 /MEMCS16I, /CASL0-3, /CASH0-3, SD0-9, SA1-19, A17-23,/XBHE,/SBHE XA1-18,LA17-23,MEMRDWR /ROMSEL,MDPCKE,MBDIR, IODEC0,IOSPEED	VOH	IOH=12mA IOH=8mA IOH=6mA IOH=4mA IOH=2mA	2.4	4.5		V
Voltage Output LOW /RAS0-3,/DRAMWE,MA0-9 /MEMCS16I,/CASL0-3,SA1-19 /CASH0-3, SD0-9, /IOCS16, /0WSOUT,IOCHRDY A17-23,/XBHE,/SBHE XA1-18,LA17-23,MEMRDWR /ROMSEL,MDPCKE,MBDIR, IODEC0,IOSPEED	VOL	IOL=24mA IOL=16mA IOL=12mA IOL=8mA IOL=4mA		0.4	0.8	V
3-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	+1	10	uA
Output Short Circuit Current	IOS	VDD=Max,VO=VDD VDD=Max,VO=0V	20 -10	110 -90	220 -190	mA mA
Supply Current	IDD	CLK=16MHz,CL=50pf		150		mA

Note: Not more than one output may be shorted at a time for a maximum duration of one second.

DRAM CAS ACCESS TIME

286 Mode



t1 = CAS delay from PROCCLK 16 ns (max)

t2 = 20ns @ 12.5 MHz, 15.6ns @ 16 MHz, 12.5ns @ 20 MHz

t3 = 12 ns (GC102 Data buffer delay)

t4 = data setup time for 80286 CPU
5ns @ 12.5 MHz, 5ns @ 16 MHz, 3ns @ 20 MHz

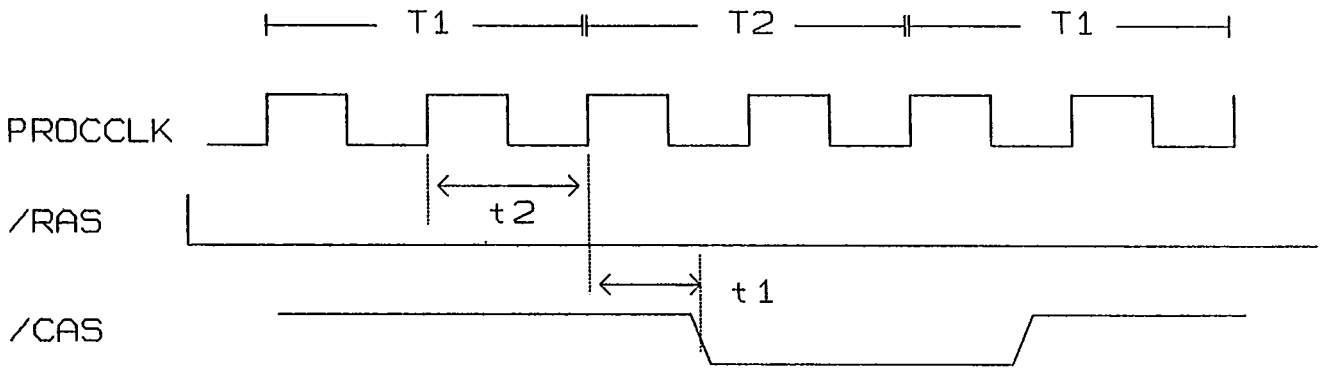
DRAM CAS access time required = 5 x t2 - (t1 + t3 + t4)
= 67ns @ 12.5 MHz 45ns @ 16 MHz 31.5ns @ 20 MHz

Figure 1

DRAM CAS ACCESS TIME

SX MODE

Inactive MD bus



t1 = CAS delay from PROCCLK 16 nS (max)

t2 = 15.625nS @ 16MHz

t3 = data setup time for 80386SX CPU = 9 nS

t_{SR} = 2nS (for series resistor, value 22 ohm)

DRAM CAS access time required = 4 x t2 - (t1 + t3 + t_{SR})
= 35.5 nS

Figure 2

DRAM
True Page Mode or 2-Way Word Interleave
286 and SX Modes

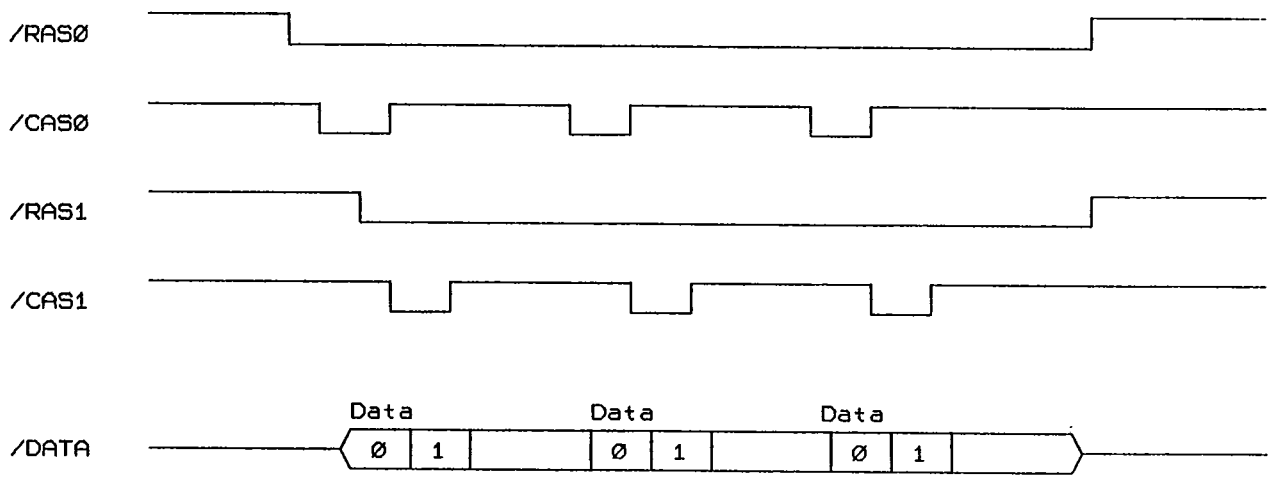


Figure 3

DRAM
True Page Mode or 4-Way Word Interleave
286 and SX Modes

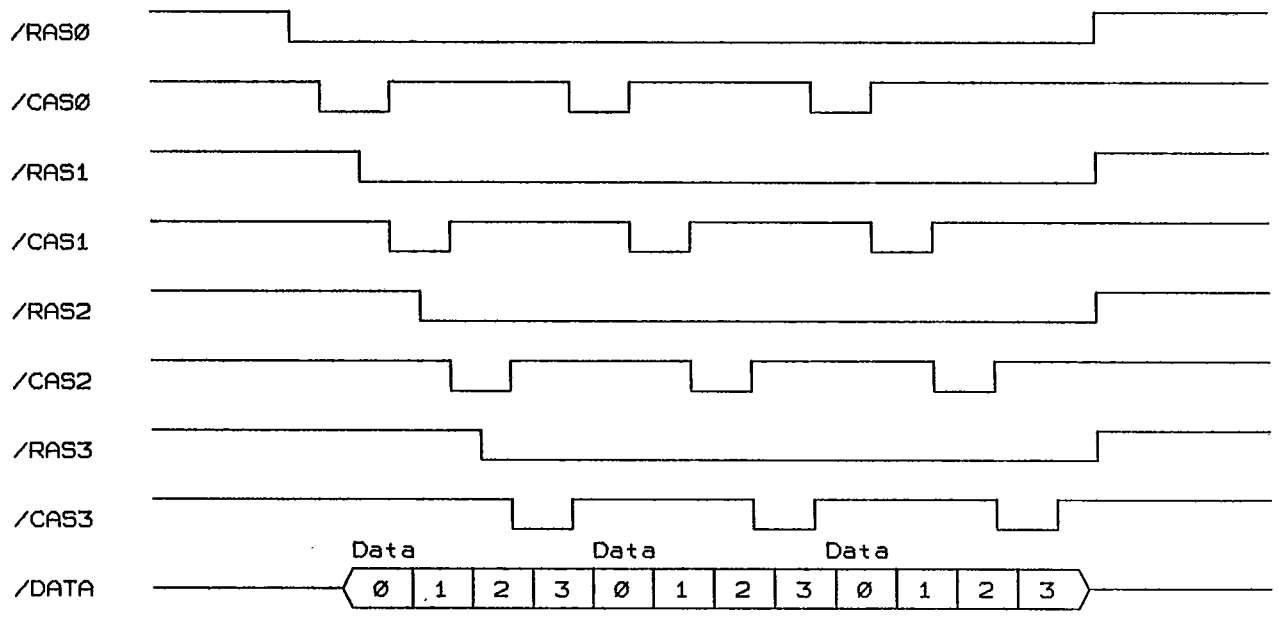
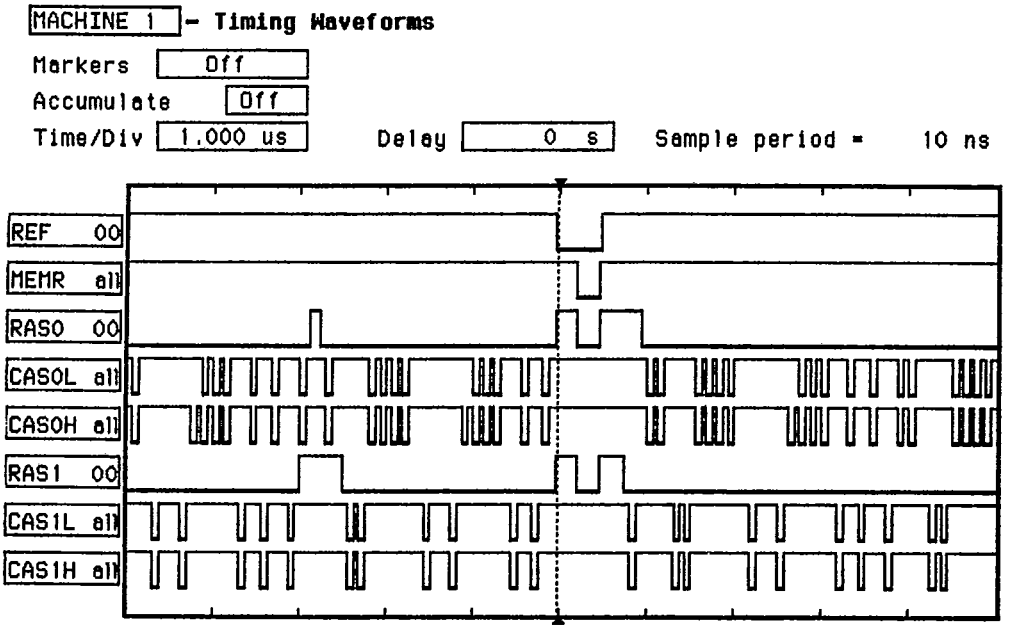


Figure 4

2 Banks of 256K Page Mode with Interleave - 16 MHz - 0 WS



2 Banks of 256K Page Mode with Interleave - 12 MHz - 0 WS

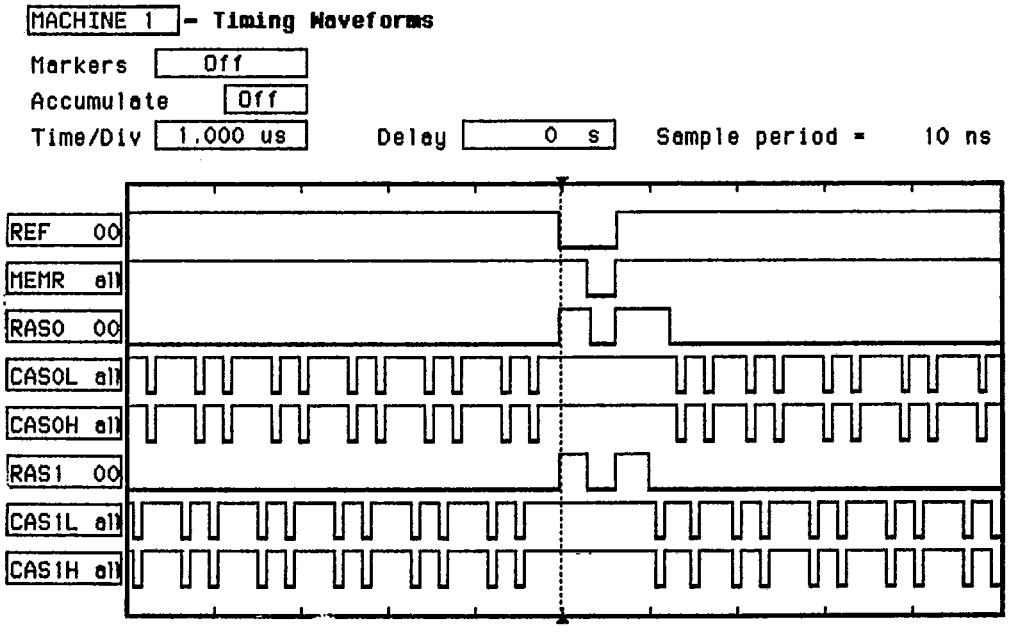
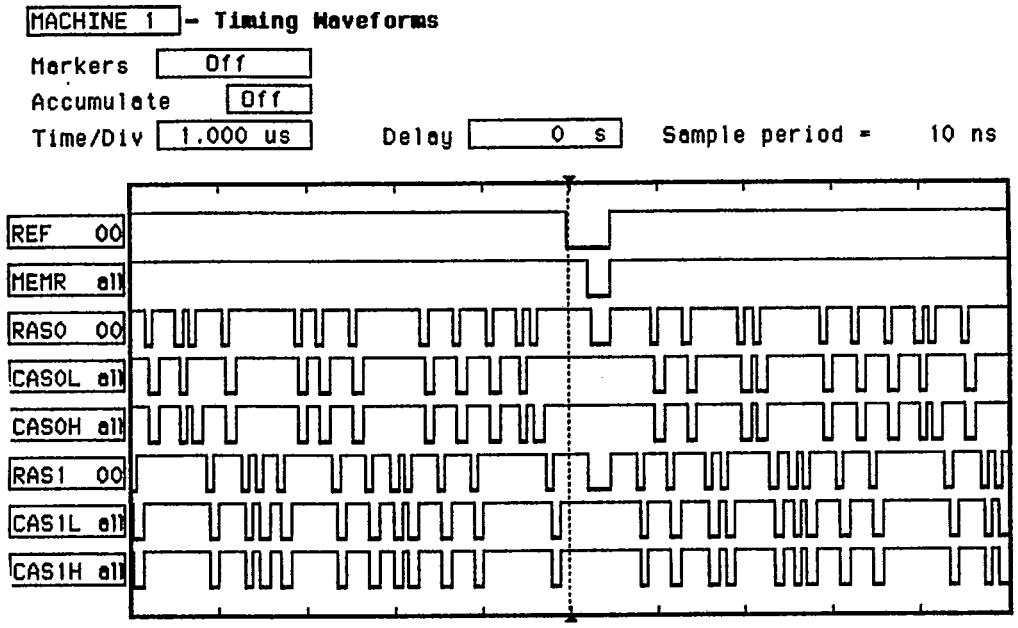


Figure 5

2 Banks of 256K Non-Page Mode
SPLSW = 1 - 16 MHz - 1 WS



2 Banks of 256K Non-Page Mode
SPLSW = 1 - 12 MHz - 0 WS

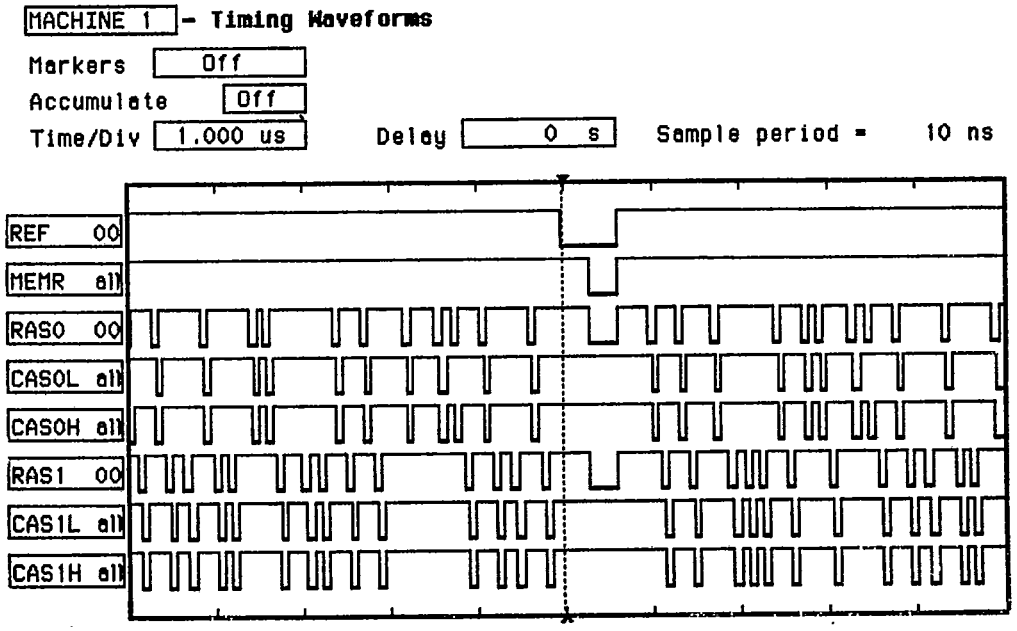
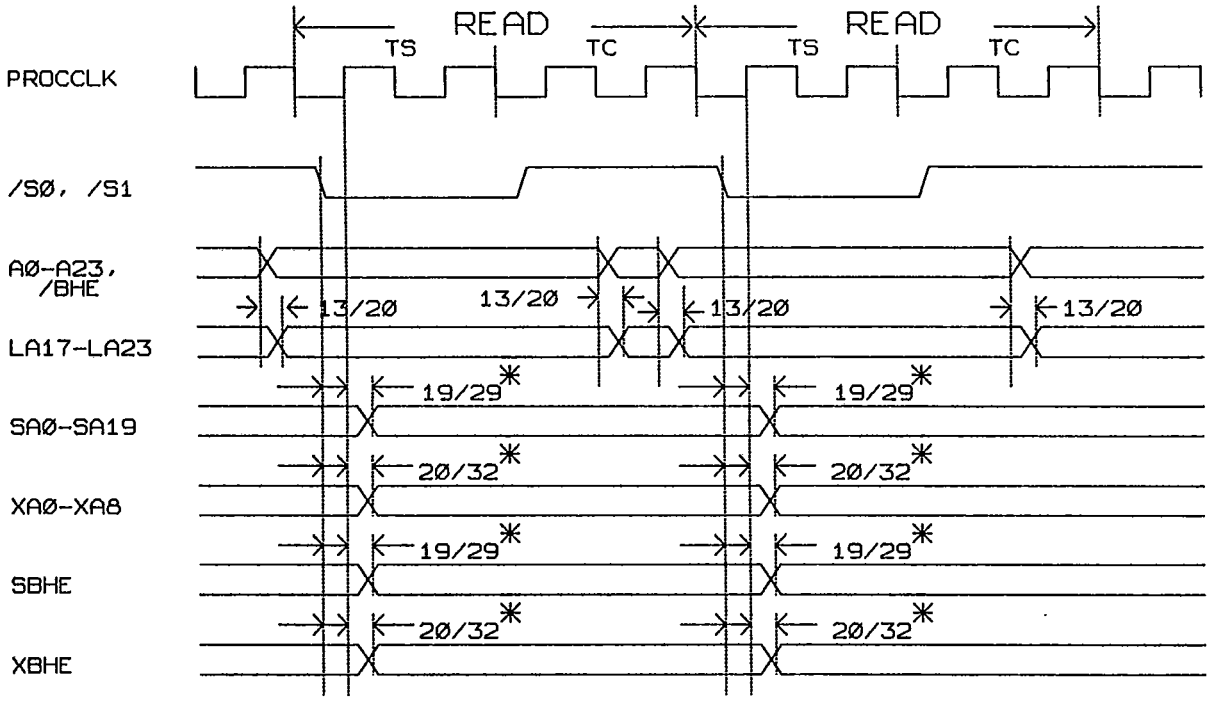


Figure 5

NORMAL OPERATION, ADDRESS OUTPUT

286 Mode



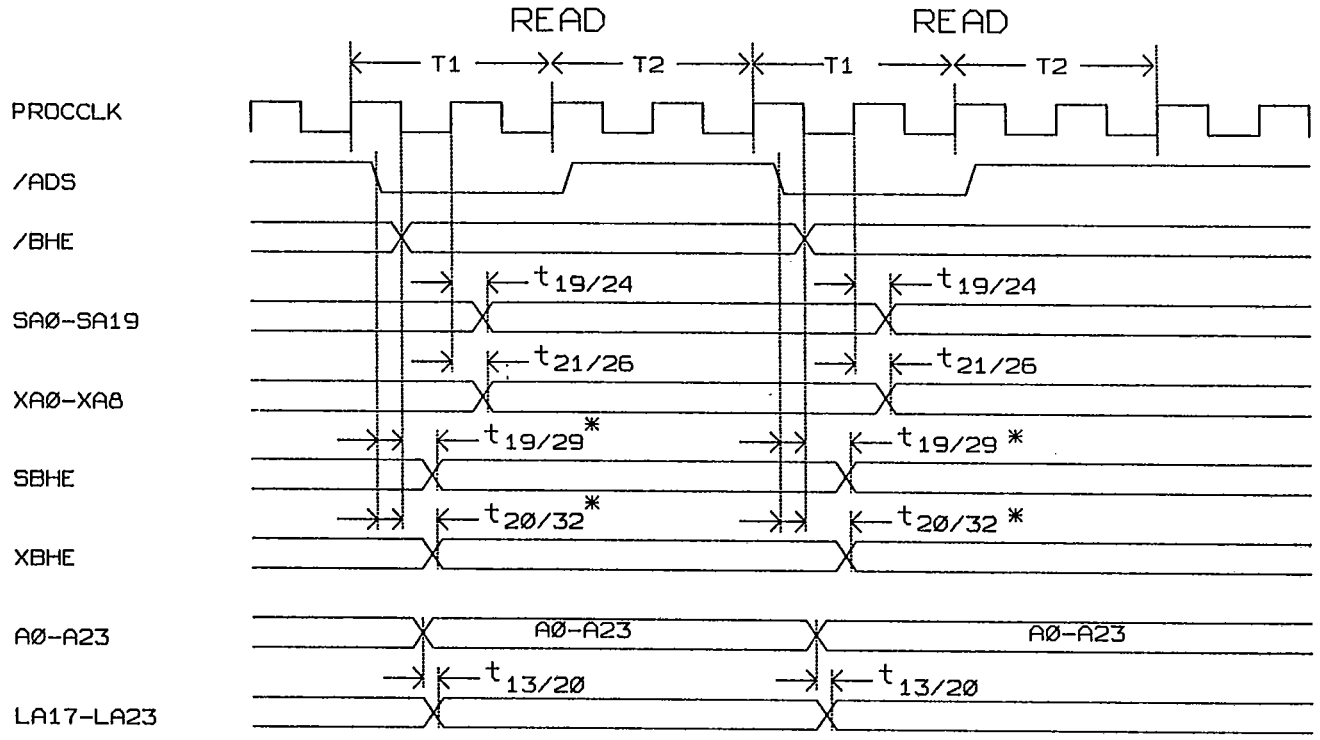
NOTE:

TYPICAL/MAX DELAY
RELATIVE TO LATER OF 2 EDGES
* = (PROCCLK RISING & SØ*/S1*)

Figure 6

NORMAL OPERATION, ADDRESS OUTPUT

SX Mode

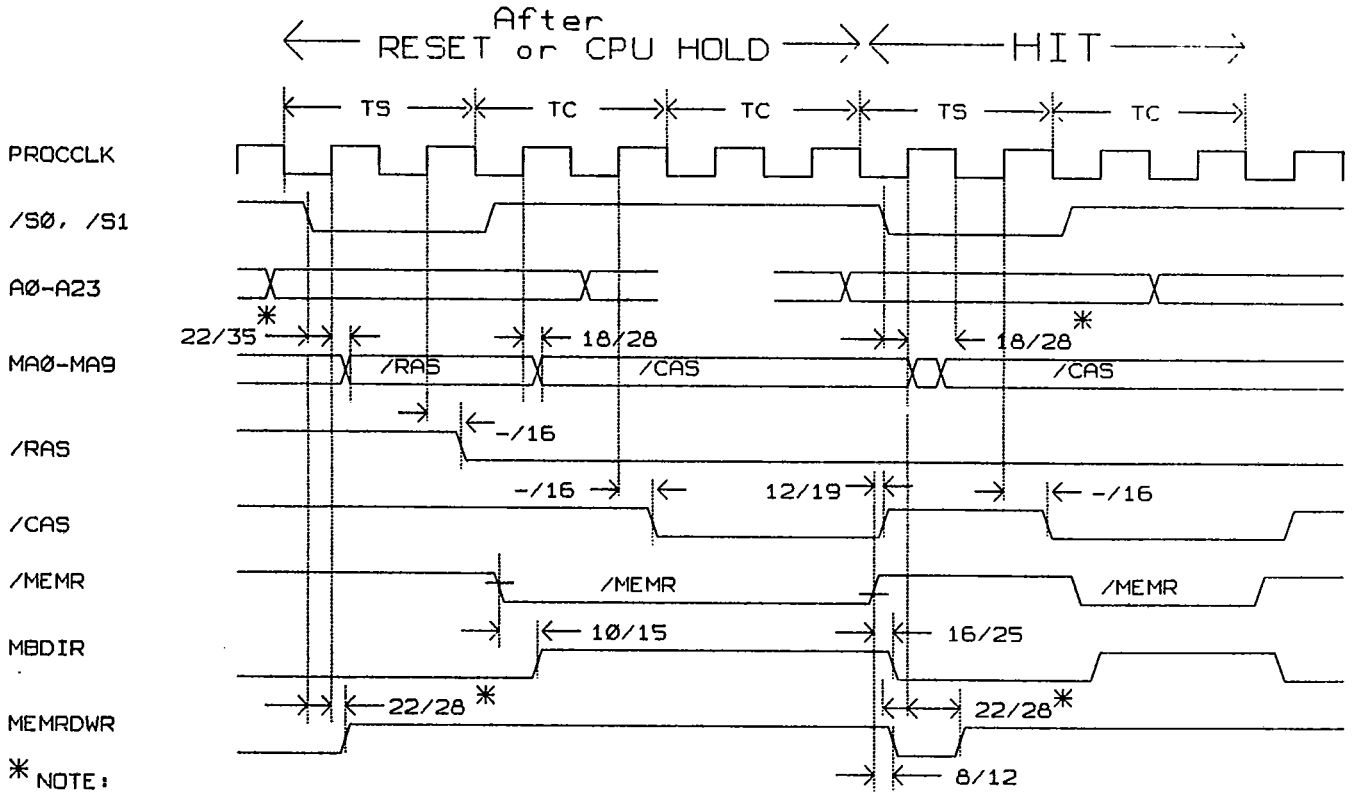


NOTE: TYPICAL/MAX DELAY
RELATIVE TO LATER OF 3 EDGES
*(PROCCLK FALLING, /ADS, or /BHE)

Figure 7

PAGE MODE, READ CYCLES 0 WAIT STATE

286 Mode
Top

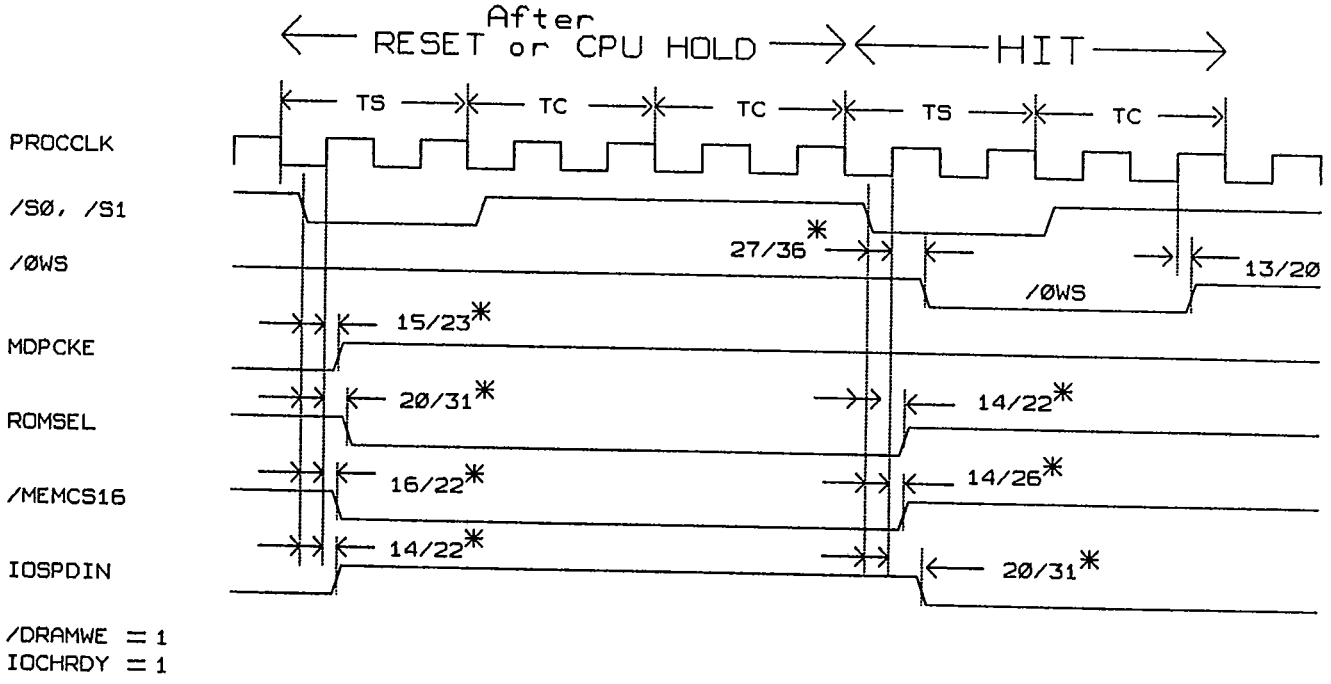


* NOTE:
TYP/MAX DELAY TIMING,
RELATIVE TO LATER OF 2 EDGES
(PROCCLK RISING or S0*/S1*)

Figure 8

PAGE MODE, READ CYCLES 0 WAIT STATE

286 Mode
Bottom

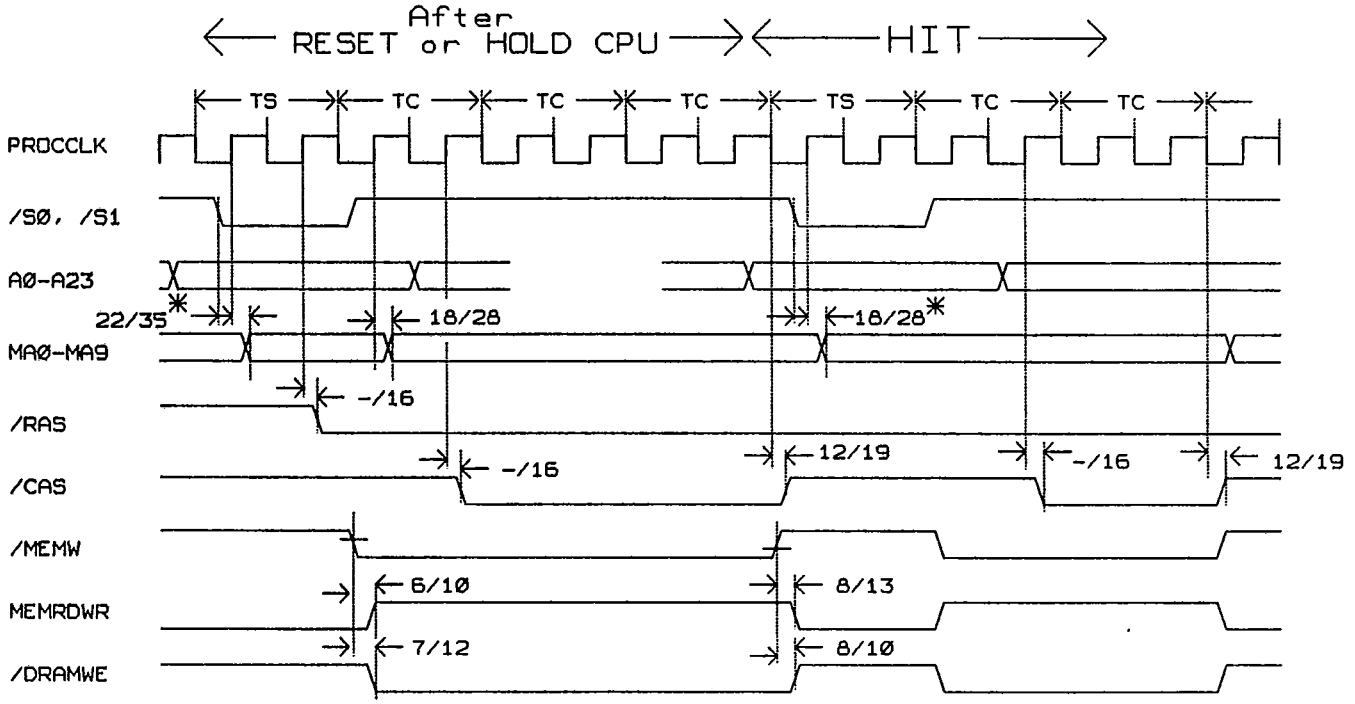


NOTE: TYP/MAX DELAY TIMING, RELATIVE TO LATER OF 2 EDGES (PROCCLK RISING or S0/S1*)

Figure 8

PAGE MODE, WRITE CYCLE 1 WAIT STATE

286 Mode
Top

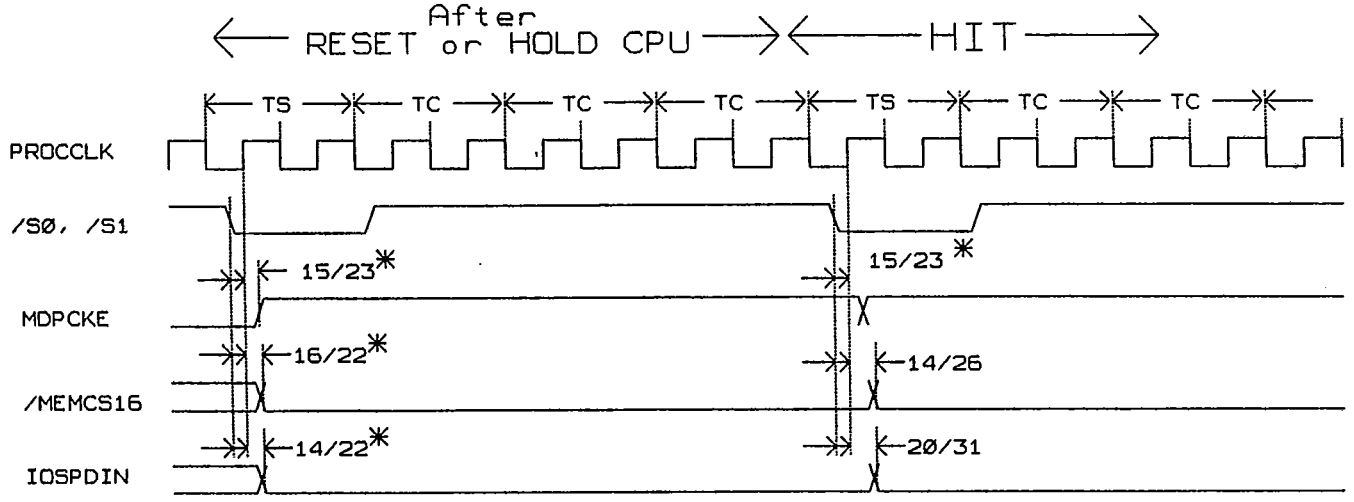


* NOTE: TYP/MAX TIMINGS
RELATIVE TO LATER OF 2 EDGES
(PROCCLK RISING or S0*/S1*)

Figure 9

PAGE MODE, WRITE CYCLE 1 WAIT STATE

286 Mode
Bottom



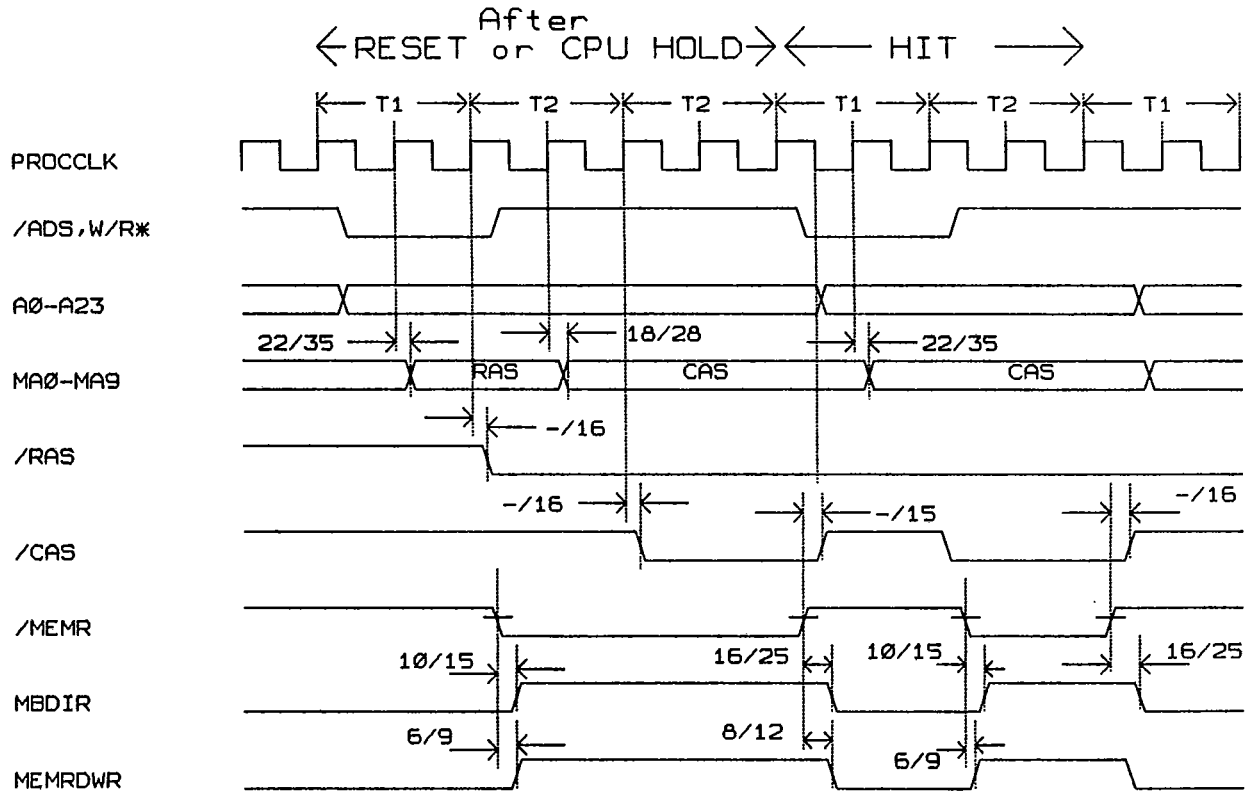
IOCHRDY =1
/0WS =1
ROMSEL =1
MBDIR =0

Figure 9

* NOTE: TYP/MAX TIMINGS
RELATIVE TO LATER OF 2 EDGES
(PROCCLK RISING or S0*/S1*)

PAGE MODE, READ CYCLES 0 WAIT STATE

SX Mode
Top



NOTE:
TYP/MAX DELAY TIMING

Figure 10

PAGE MODE, READ CYCLES 0 WAIT STATE

SX Mode
Bottom

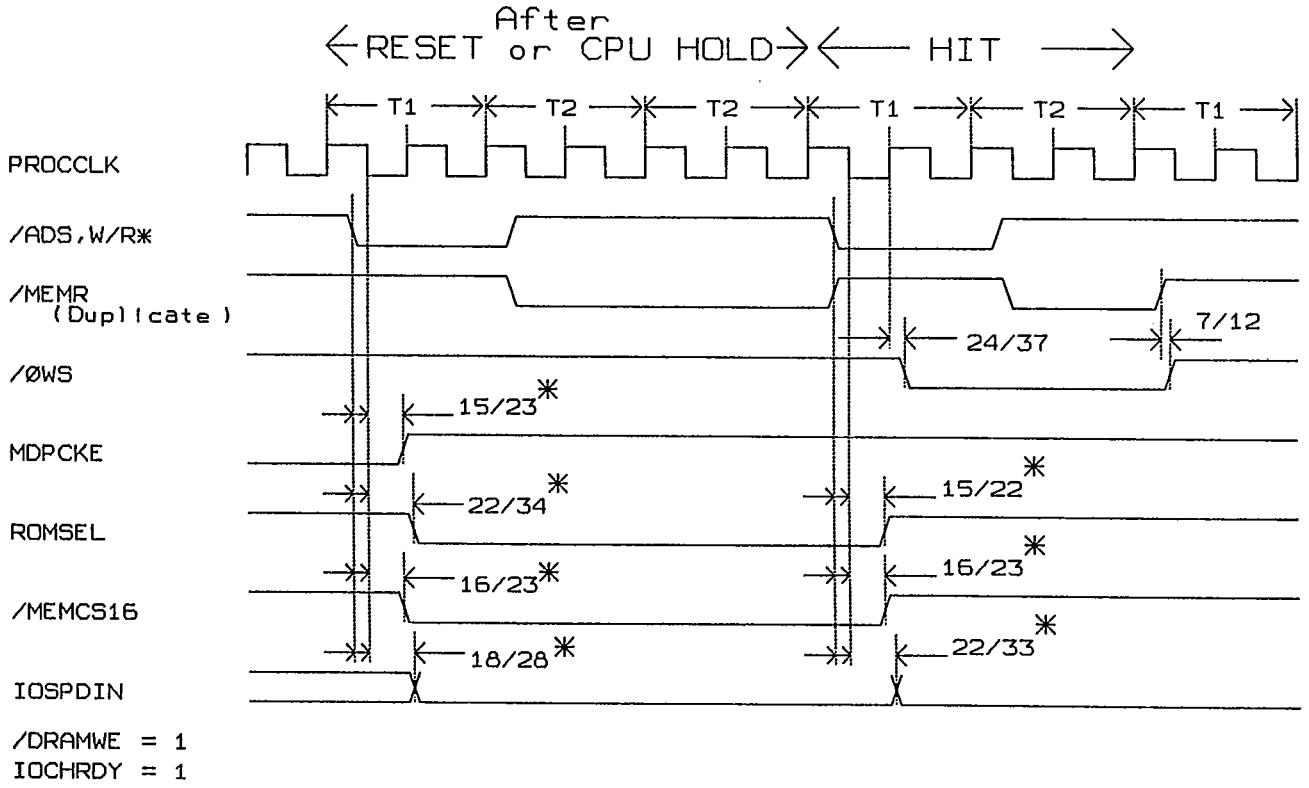


Figure 10

NOTE: TYP/MAX DELAY TIMING,
RELATIVE TO LATER OF 2 EDGES
* = (PROCCLK FALLING OR ADS*)

PAGE MODE, WRITE CYCLE 1 WAIT STATE

SX Mode
Top

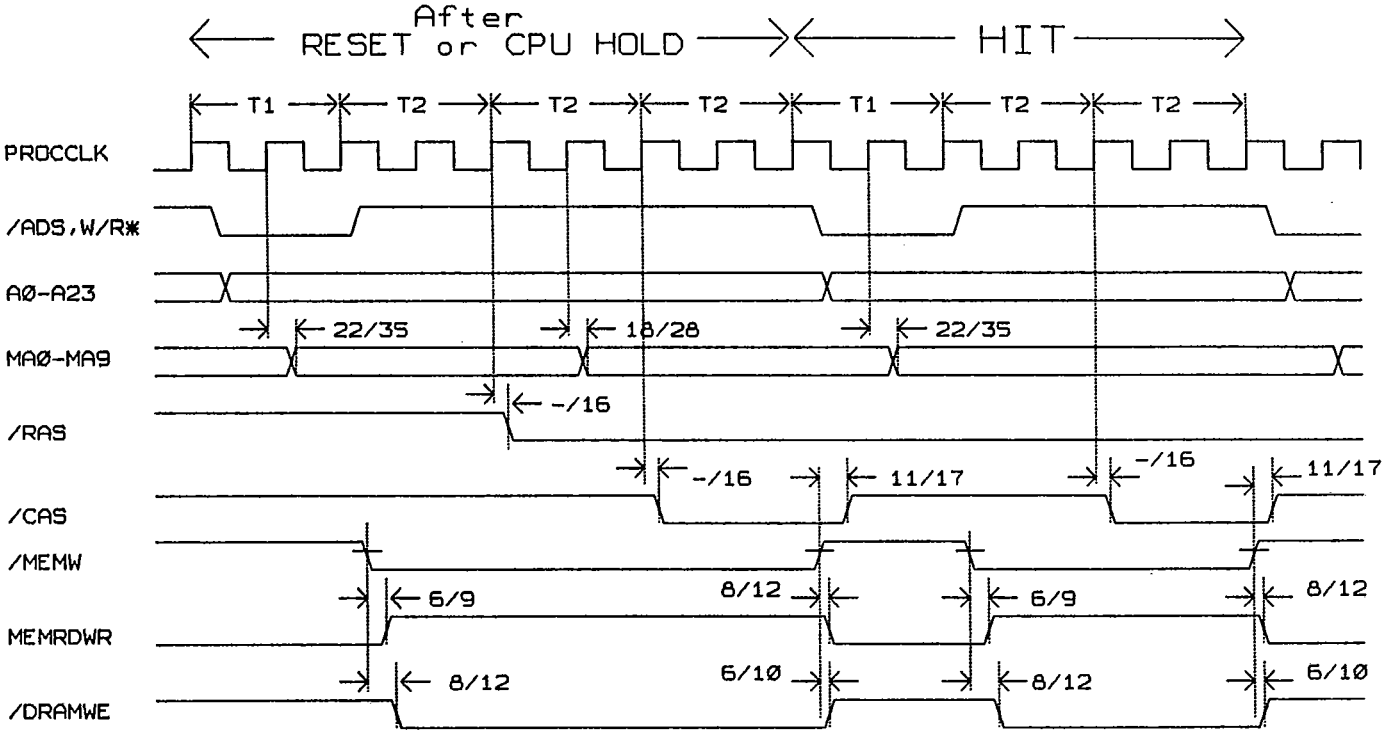
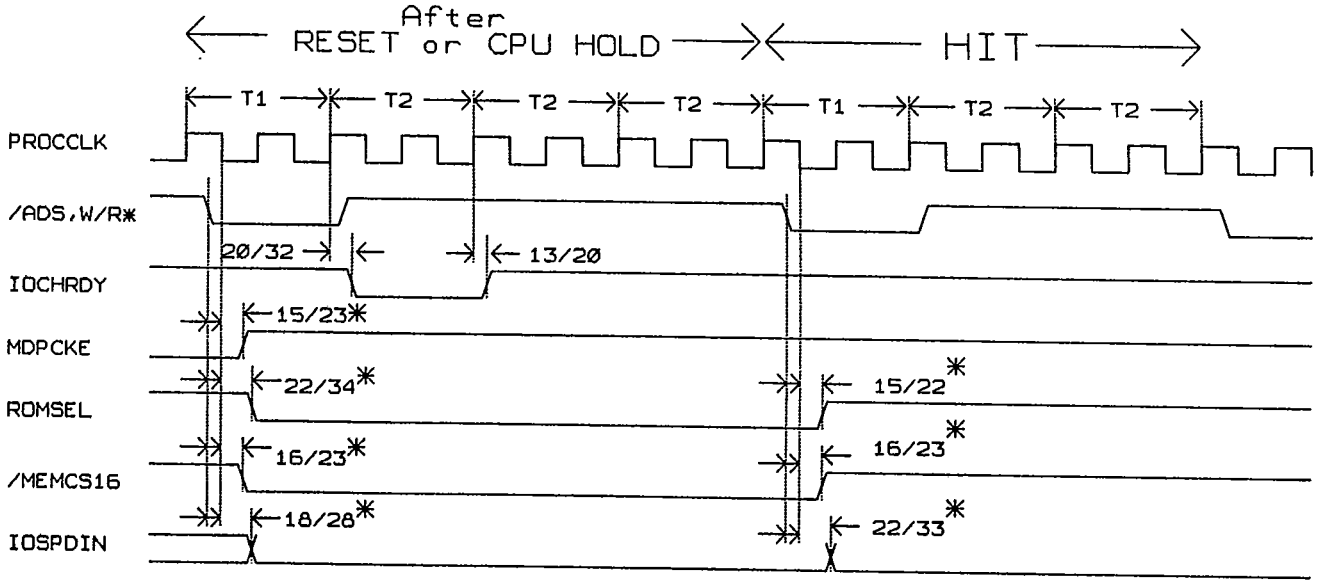


Figure 11

NOTE: TYP/MAX TIMINGS

PAGE MODE, WRITE CYCLE 1 WAIT STATE

SX Mode
Bottom



/ØWS = 1
MBDIR = Ø

Figure 11

*NOTE: TYP/MAX TIMINGS
RELATIVE TO LATER OF 2 EDGES
(PROCCLK FALLING OR /ADS)

EXTERNAL DELAY TIMING 0 WAIT STATE

286 Mode

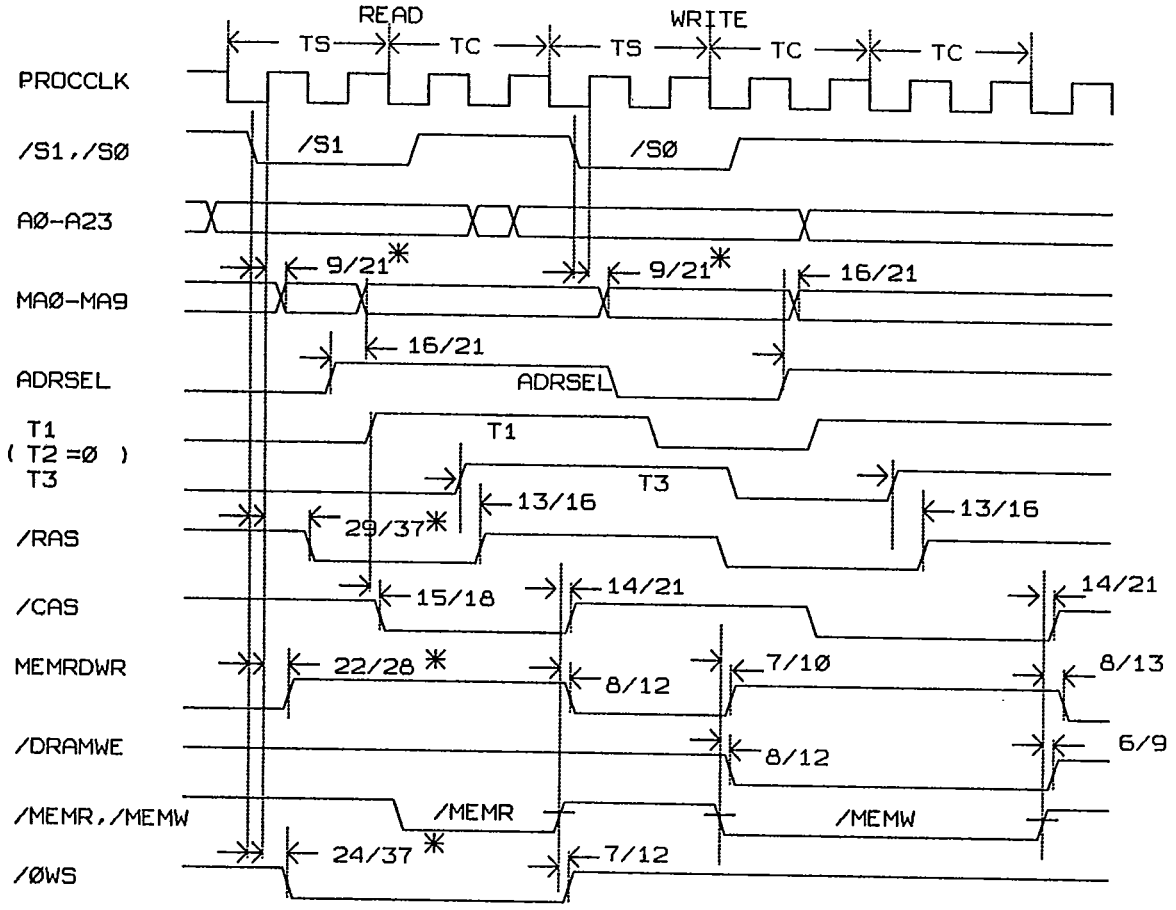


Figure 12

TYP/MAX
TIMINGS

EXTERNAL DELAY TIMING 1 WAIT STATE

SX Mode

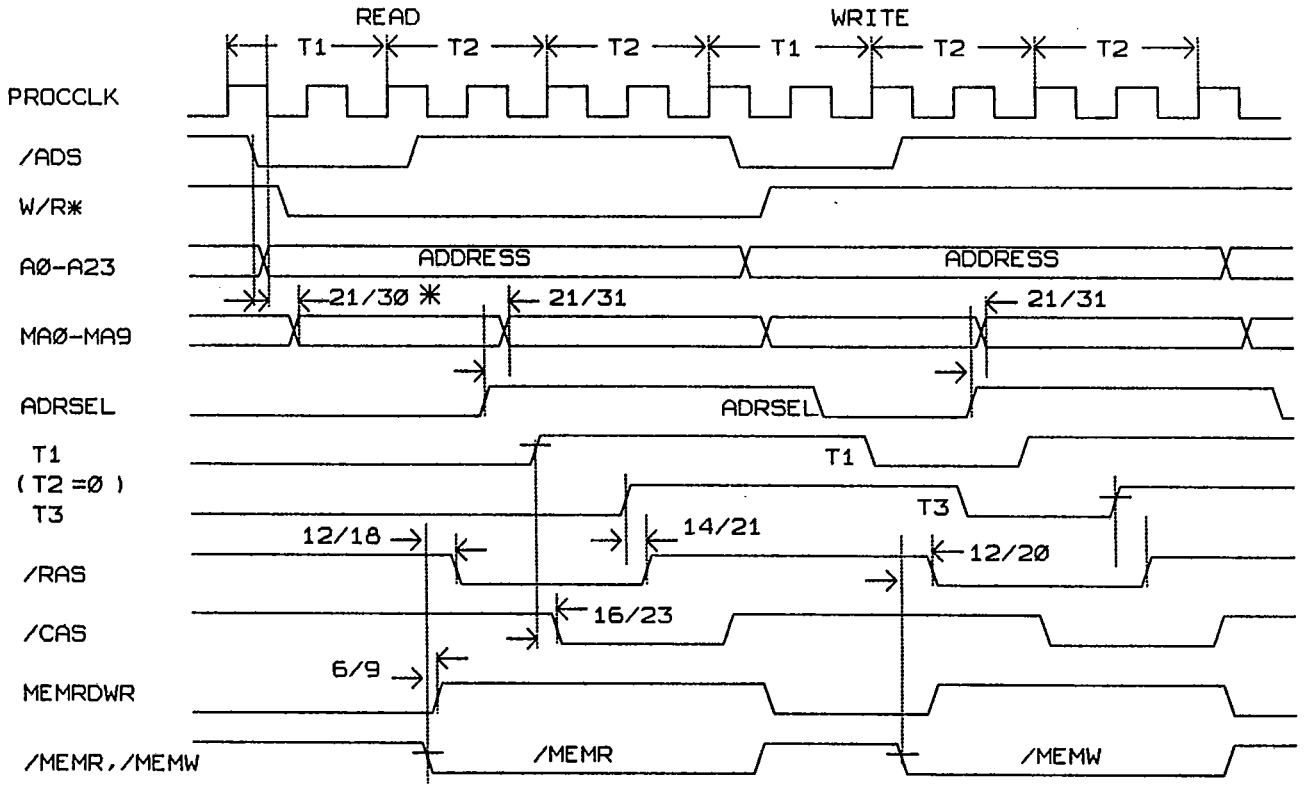


Figure 13

* TYP/MAX,
RELATIVE TO LATER
(PROCCLK RISING or /ADS)

INTERNAL DELAY TIMING 0 WAIT STATES

286 Mode

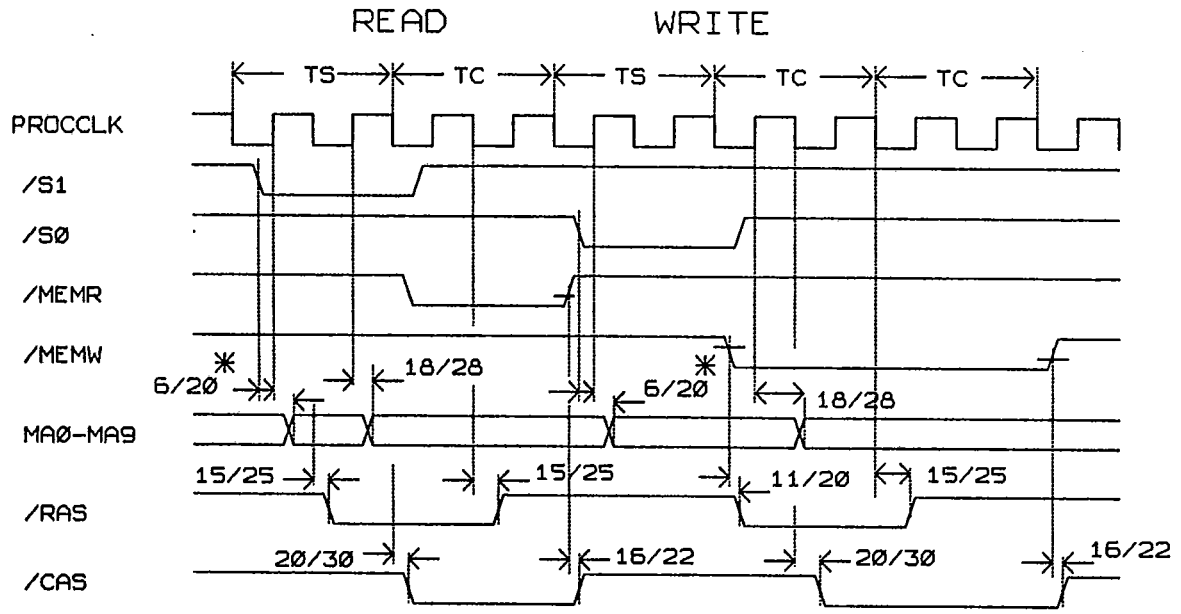


Figure 14

TYP/MAX
TIMINGS

INTERNAL DELAY TIMING 1 WAIT STATES

SX Mode

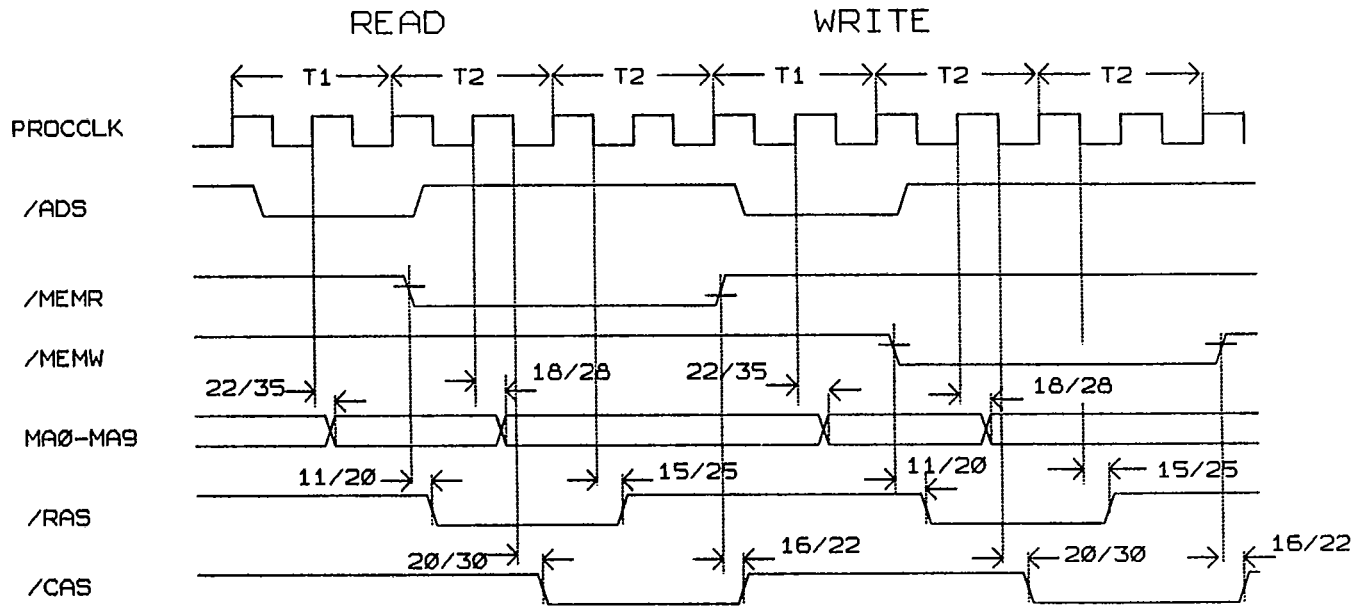
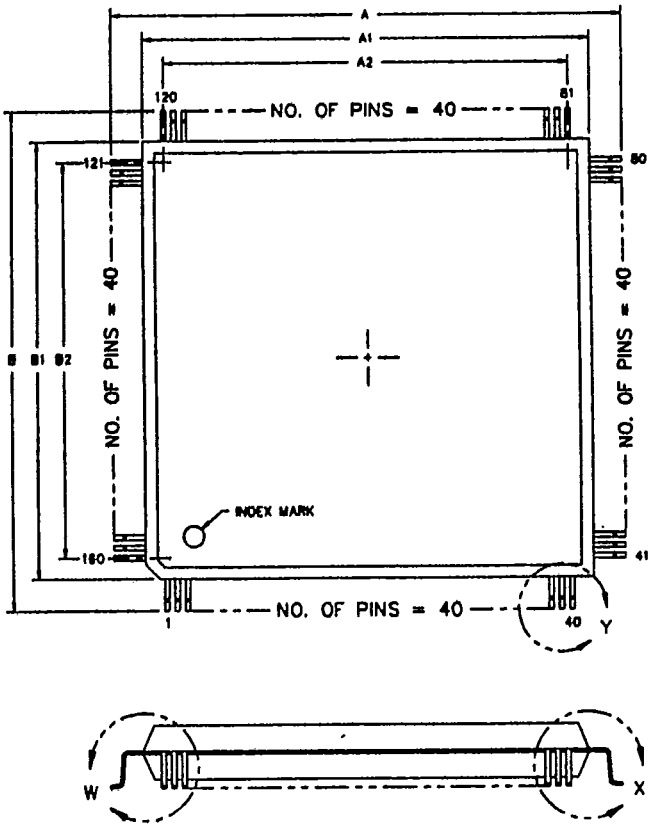


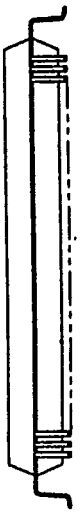
Figure 15

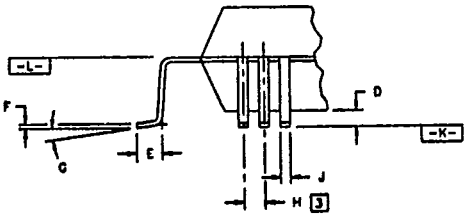
TYP/MAX
TIMINGS

GC113
Package Outline

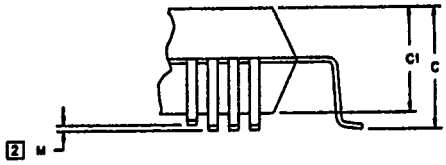
160-Pin Flat Pack (Gull Wing)



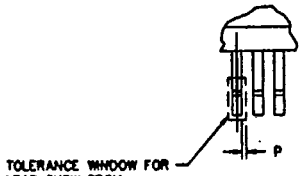




DETAIL W



DETAIL X



DETAIL Y

NOTES: UNLESS OTHERWISE SPECIFIED

1. NOMINAL DIMENSIONS IN MILLIMETERS. INCHES ROUNDED TO THE NEAREST .001 INCH.
2. COPLANARITY OF ALL LEADS SHALL BE WITHIN 0.1 MM (0.004") (DIFFERENCE BETWEEN HIGHEST AND LOWEST LEAD WITH SEATING PLANE -K- AS REFERENCE)
3. LEAD PITCH DETERMINED AT DATUM -L-
4. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.

[1]

DIMENSIONS IN MM		
SYM	MINIMUM	MAXIMUM
A	31.60	32.40
A1	27.90	28.10
A2	25.35 REF	
B	31.60	32.40
B1	27.90	28.10
B2	25.35 REF	
C	3.68	4.01
C1	3.43	3.66
D	0.25	0.36
E	0.60	1.00
F	0.10	0.25
G	0°	10°
H	0.65 ±0.15	
J	0.25	0.35
M	0.10 MAX	
P	0.05 MAX	
TOTAL NO. OF PINS	160	

[1]

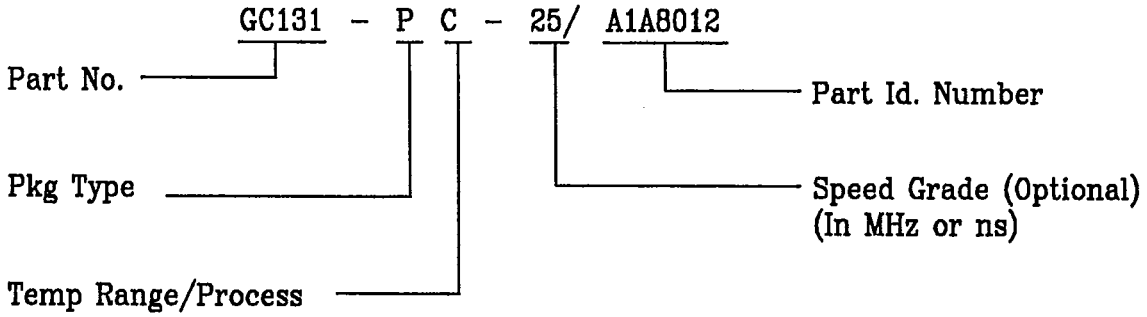
DIMENSIONS IN INCHES		
SYM	MINIMUM	MAXIMUM
A	1.244	1.276
A1	1.098	1.106
A2	0.998 REF	
B	1.244	1.276
B1	1.098	1.106
B2	0.998 REF	
C	0.145	0.158
C1	0.135	0.144
D	0.010	0.014
E	0.024	0.039
F	0.004	0.010
G	0°	10°
H	0.026 ±0.006	
J	0.010	0.014
M	0.004 MAX	
P	0.002 MAX	
TOTAL NO. OF PINS	160	

IMPORTANT NOTE:

If designing in inches, ALL pin positions should be calculated in millimeters (mm) then converted to inches. The inches listed have been rounded.

Product Ordering Information & Part Marking

Order Code/Part Number Example



Temp Range/Process

C – Commercial temp range

I – Industrial temp range

Package Types

P – Plastic

IMPORTANT: Contact your local sales office for the current Order Code/Part Number