LSTTL GATE ARRAY

HT5000

PRODUCT DESCRIPTION

The HT5000 Gate Array (Figure 1) is a 600 picosecond, 5000 equivalent gate density Very Large Scale Integration (VLSI) monolithic integrated circuit built using Honeywell's ADB-II™ fabrication process. The array is composed of an uncommitted array of Current-Mode-Logic gates (Figure 2) and LSTTL compatible I/O cells. Thirty-five hundred (3500) gates are autoroutable to provide the advantages of both VLSI and proprietary design.

Designing with the HT5000 is easy and fast requiring only conventional logic design, logic simulation, and test pattern generation. The computer-aided-design and autorouting methodologies are similar to those used for printed circuit boards.

Logic functions are predefined by Honeywell and are implemented by automatically interconnecting the macrocells using two layers of metal routing. Both cell intraconnection and routing of power buses are invisible to the user. For external interface, up to 120 LSTTL compatible I/O buffers can be specified.

The basic circuit technique used to implement logic functions is a two-level series gated CML structure. This technique gives maximum flexibility and performance in implementing a given function. Macrocells such as adders, decoders, latches, and flip flops are built using only one layer of metal within a cell. This eliminates many interconnects normally done in the routing channels of a gate array, simplifying the autorouting task.

Compared to TTL gate arrays with ECL internal circuitry, the HT5000 with its lower power, higher component density, and more efficiently built macrocells results in substantial performance improvement (circuit speed) and space reduction. The increased use of on-chip components reduces system costs.

The ultra high packing density of the HT5000 offers up to a 200-to-1 reduction in system component count when compared with similar systems built using conventional SSI/MSI LSTTL logic functions. The user obtains a degree of optimization like that of a full custom design and the quick turnaround time of a semicustom part.

FEATURES

- **Customer programmable VLSI**
- **5000 equivalent (OR/NOR) gates**
- **120 LSTTL or CML compatible I/O cells**
- **Input buffer delay: 0.75 ns typical**
- **Internal gate delay: 0.6 ns typical**
- **Output buffer delay: 6.0 ns typical**
- **Operating temperature ranges**
  - **—Commercial: 0° to +70°C (T_A)**
  - **—Military: −55° to +125°C (T_C)**
- **Power dissipation: 2.5 watts typical**
- **Series gated CML internal logic functions**
- **Available packaging includes:**
  - **−68, 84, 108, and 148 pin leadless-chip-carriers**
  - **−100, 144, and 152 pin grid arrays**

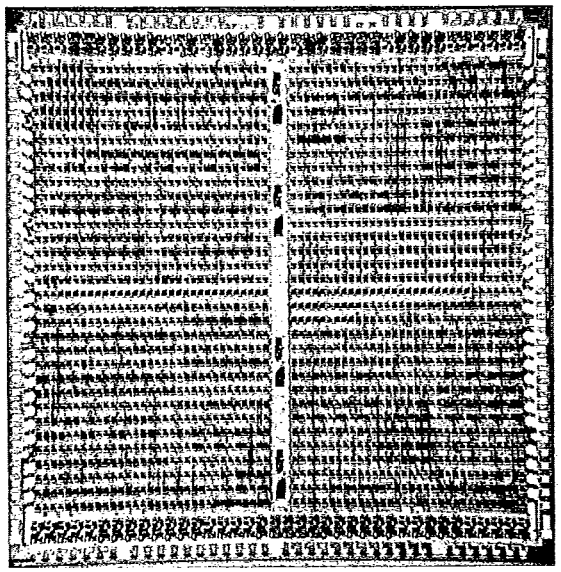

Figure 1. HT5000 Gate Array

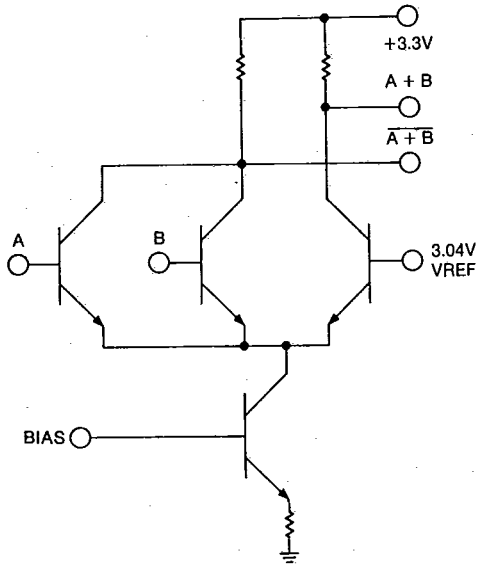

Figure 2. CML Two-Input OR/NOR Gate

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COMPUTER-AIDED-DESIGN SYSTEM

Honeywell's Software Toolkit™ for VLSI gate array design is built around industry standard software programs. Most importantly, a standardized design language, Mentor SIM™, is available for logic simulation. This language is used hierarchically to define complex logic functions in a computer readable data base. The data is then accessed by other software programs for simulation, analysis, autorouting, and array fabrication.

In addition to Mentor SIM, the Software Toolkit contains programs for schematic entry, netlist generation, timing verification, design statistic analysis, loading/fanout analysis, media delay feedback/analysis, and test program compilation. Industry standard programs are also available for automatic placement, automatic routing, and interactive graphics editing.

Honeywell supports the Software Toolkit for customers with a variety of in-house design automation capabilities. A set of tools hosted on popular workstations provides complete schematic-through-PG tape capability in the hands of the system designer. Customers can use the Software Toolkit at Honeywell's Colorado Springs Design Center or in their own facility.

FOR CUSTOMERS WITH MENTOR GRAPHICS ENGINEERING WORKSTATIONS

Mentor Graphics provides the following IDEA 1000™ programs as part of the Software Toolkit:

SYMED™ Mentor symbol generation package used with Honeywell-developed macrocell symbols. User may create new macrocell symbols using the macrocell library provided.

NETED™ Mentor schematic entry package used with Honeywell developed macrocells. User calls symbols from a library and interconnects them to implement his design.

SIM™ Mentor logic simulation package used with Honeywell developed macrocells. User provides input patterns to functionally debug the design.

EXPAND™ Mentor design expansion package used with Honeywell developed macrocells. Used for removing design hierarchy (nesting of macrocells) from design file prior to autoplacement.

Honeywell provides the following programs as part of the Software Toolkit:

LOADS™ Honeywell developed logic rules check and load modeling program. Informs the user of illegal loading or electrical violations. Also modifies macrocell propagation delays based on junction temperature, fanout, and power supply voltage.

STATS™ Honeywell developed design statistics report. Lists chip power, cell count and utilization. Informs user if either cell count or I/O count exceed maximums for the specific gate array.

WIRES™ Honeywell developed wire delay calculation program. Lists all nets by line length and delay with error reporting for nets exceeding specified limits. Recomputes user design files with user specified temperature and actual wire delays.

TESTS™ Honeywell developed automatic test program compilation software. Takes functional test vectors from logic simulation and parametric test requirements to generate Series 20 compatible test tapes.

Ask your local Honeywell sales representative for further information on the Software Toolkit.

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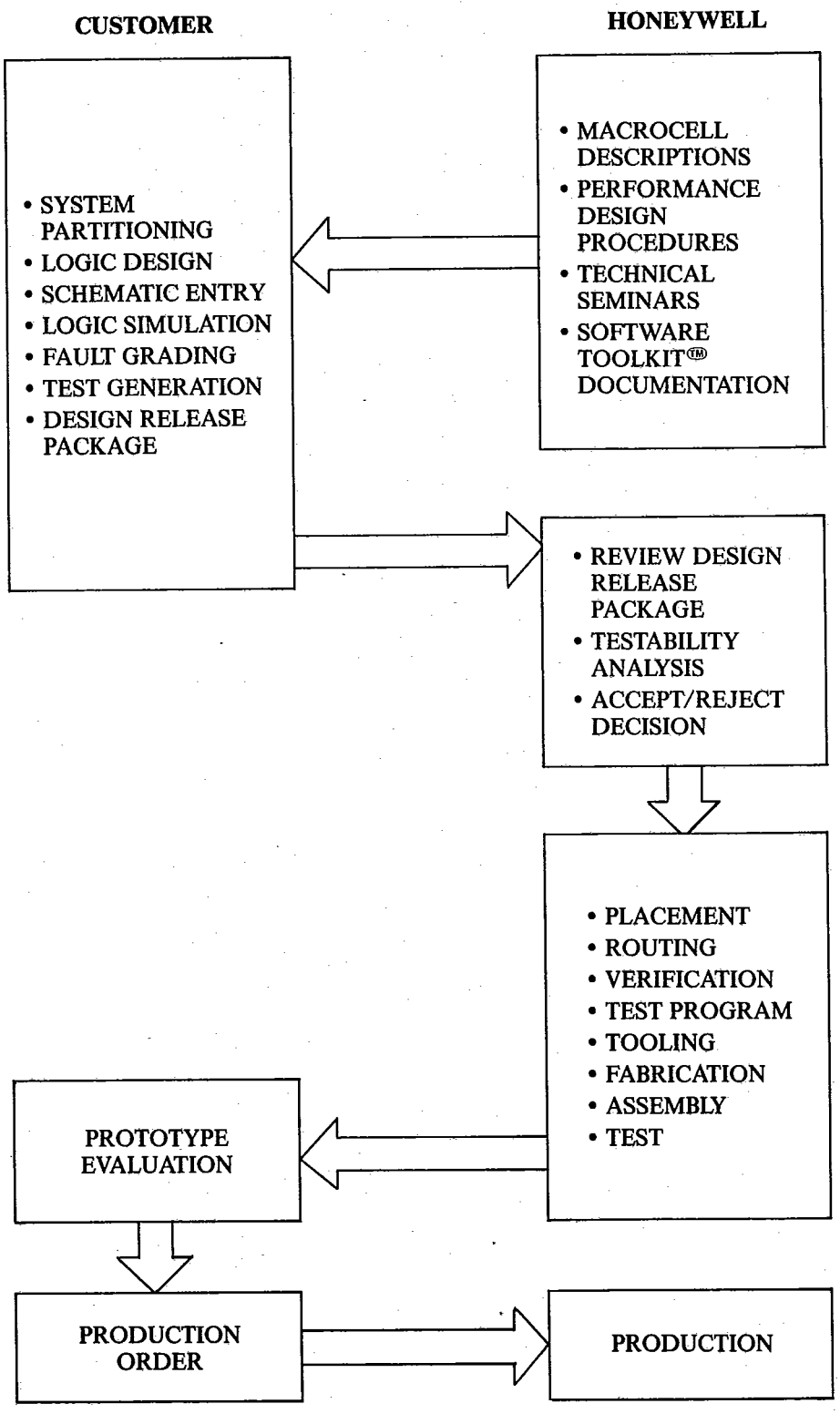
GATE ARRAY DEVELOPMENT FLOW



INPUT/OUTPUT CELLS

All signals within the array interface to external pins through I/O buffers located around the device perimeter.

A description plus the logic for each I/O cell are shown in Figure 3.

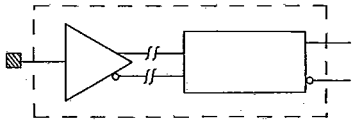
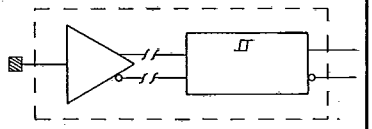
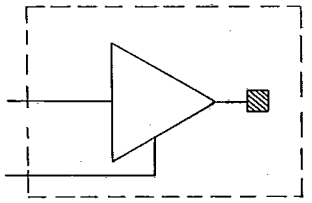
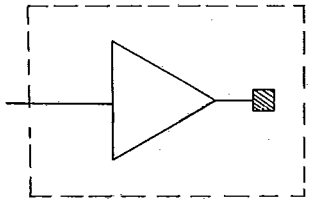
INPUT BUFFERS	
DESCRIPTION: LSTTL compatible input buffer with CML outputs.	**LOGIC:**  **U907-B19**
DESCRIPTION: LSTTL compatible Schmidt trigger input buffer with CML outputs.	**LOGIC:**  **U907-B20**
OUTPUT BUFFERS	
DESCRIPTION: LSTTL compatible output buffer with three-state output.	**LOGIC:**  **U902**
DESCRIPTION: LSTTL compatible output buffer with open collector output.	**LOGIC:**  **U903**

Figure 3. I/O Cells

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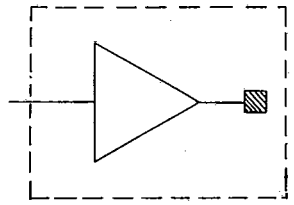
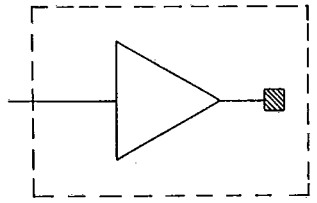
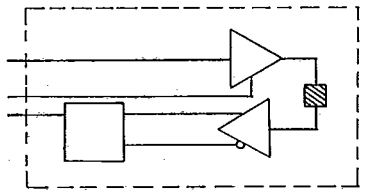
OUTPUT BUFFERS	
DESCRIPTION: LSTTL compatible output buffer with totem pole active pullup.	**LOGIC:**  **U904**
DESCRIPTION: CML differential line driver.	**LOGIC:**  **U905**
DESCRIPTION: LSTTL compatible transceiver buffer with three-state output.	**LOGIC:**  **U909-B19**

Figure 3. I/O Cells (Concluded)

LSTTL GATE ARRAY

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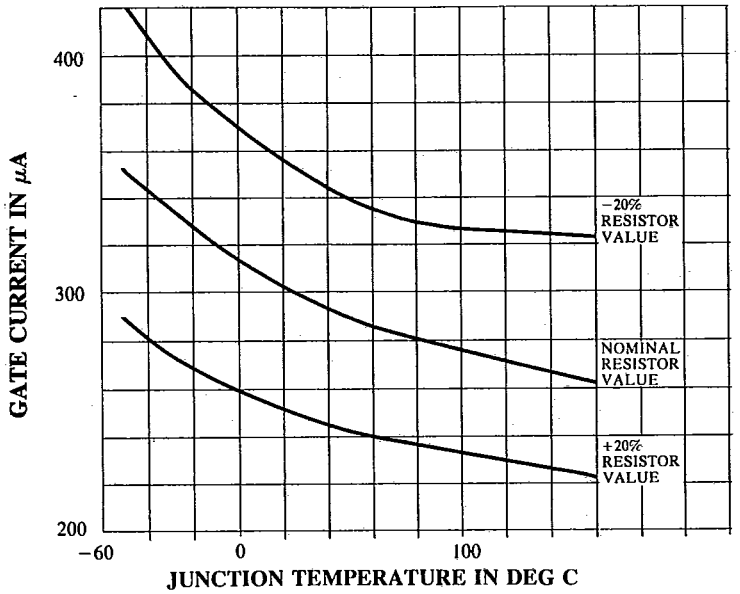
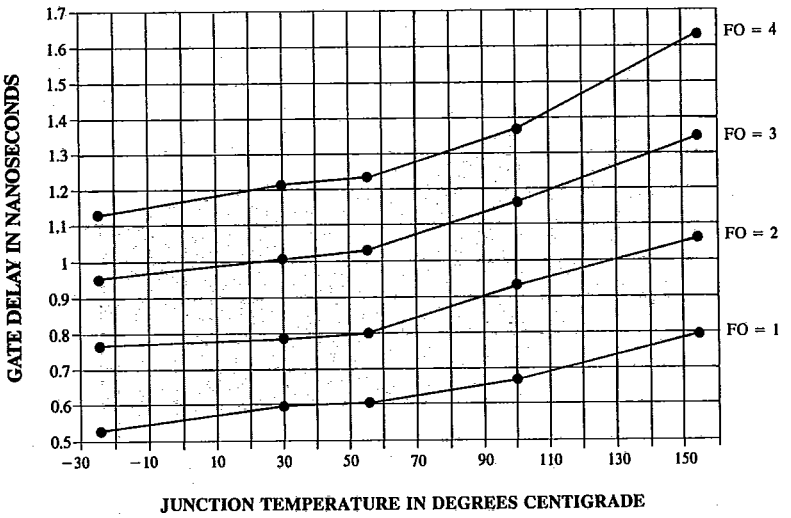
TYPICAL PERFORMANCE CHARACTERISTICS

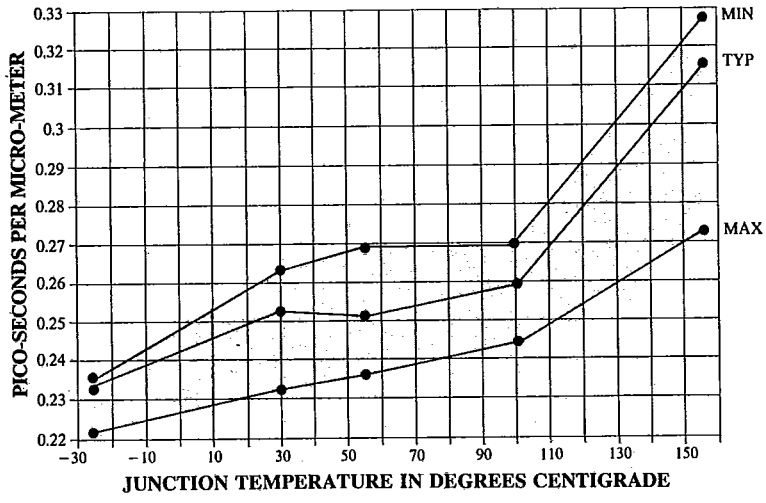
U02 (TWO INPUT OR/NOR) GATE CURRENT VS TEMPERATURE



HT5000 INTRINSIC GATE DELAY

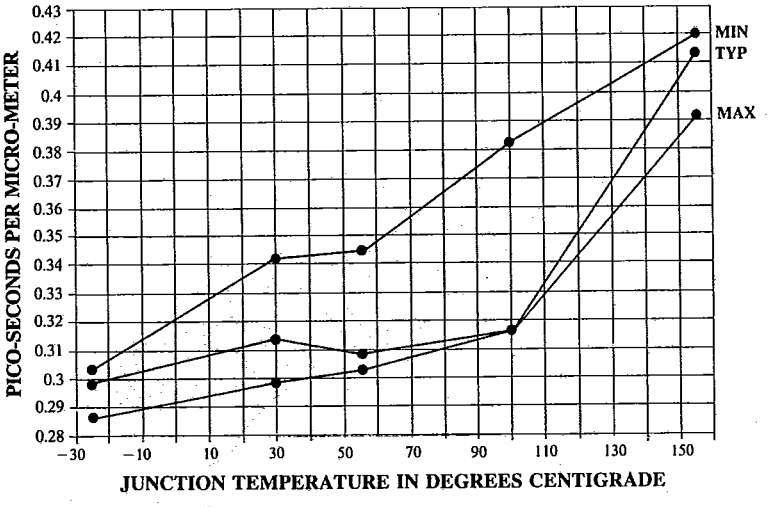


FIRST METAL MEDIA DELAY



KEY	VCC1	VCC2
MIN	4.5V	3.0V
TYP	5.0V	3.3V
MAX	5.5V	3.6V

SECOND METAL MEDIA DELAY



KEY	VCC1	VCC2
MIN	4.5V	3.0V
TYP	5.0V	3.3V
MAX	5.5V	3.6V

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LSTTL GATE ARRAY

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POWER DISSIPATION

The typical power dissipation for any given implementation of the HT5000 Gate Array is given by the following equation:

Typical Power (mW) = .9 × number of CML current sources
+ 10.1 × number of transceivers
+ 7.5 × number of output buffers
+ 1.25 × number of input buffers
+ 120 mW for reference regulators
+ .5 × load current (mA).

Load Current = Maximum I_{OL} for selected temperature range × total number of output buffers and transceivers that can be at a low output state simultaneously.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	DESCRIPTION	COMMERCIAL			MILITARY			UNITS
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
V_{CC1}	Supply voltage	4.75	5.00	5.25	4.50	5.00	5.50	V
V_{CC2}	Supply voltage	3.15	3.30	3.45	3.00	3.30	3.60	V
T_A or T_c	Operating free-air temperature	0		70	−55		125	°C
F_{MAXT}	Maximum internal flip flop toggle frequency			150			150	MHz
F_{IN}	Maximum input frequency at package pin [1]			100			100	MHz

[1] Package selection will determine the maximum input frequency. Consult Honeywell.

ABSOLUTE MAXIMUM RATINGS [2]

PARAMETER	DESCRIPTION	RATING	UNITS
V_{CC1}	Supply voltage	+7.0	V
V_{CC2}	Supply voltage	+4.6	V
E_{IN}	Input voltage continuous	−0.5 to +5.5	V
I_{IN}	Input current continuous	−30 to +1.0	mA

PARAMETER	DESCRIPTION	RATING	UNITS
V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
T_J	Junction temperature	+175	°C

[2] Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
CML GATE (Internal)									
$I_{CC2/G}$	Power supply current per current source[3]	V_{CC1} = +5V, V_{CC2} = +3.3V	230	270	340	225	270	400	μA
ILF	Input load factor			1			1		Unit load
FO	Fanout		1		4	1		4	Unit load
t_{pdAV}	Average gate propagation delay	Fanout = one (1) CML gate	.59	.60	.67	.52	.60	.80	ns

[3] Typical applications estimate 2.5 gates/current source.
Maximum current values at −55°C(C). Minimum current values at +125°C(C).

LSTTL GATE ARRAY HT5000

DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions (cont.)

PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BUFFERS: Standard								**U907-B19**
I_{CC2} Power supply current	V_{IN} = 0.4V, V_{CC2} =3.3V	310	375	465	310	375	465	μA
V_{IH} Input high voltage		2.0			2.0			V
V_{IL} Input low voltage				.8			.7	V
I_{IL} Input low current (side)	V_{IN} = 0.4V, V_{CC2} = 3.3V			−.45			−.45	mA
I_{IH} Input high current (side)	V_{IN} = 2.7V, V_{CC2} = Max			20			20	μA
I_{IL} Input low current (top)	V_{IN} = 0.4V, V_{CC2} = 3.3V			−.84			−.84	mA
I_{IH} Input high current (top)	V_{IN} = 2.7V, V_{CC2} = Max			70			70	μA
FO Fanout		1		4	1		4	Unit load
t_{pdLH} Propagation delay, low-to-high F.O. = one (1) CML load	(See Figure 4a)		0.75	1.00		0.75	1.00	ns
t_{pdHL} Propagation delay, high-to-low F.O. = one (1) CML load	(See Figure 4a)		1.00	1.50		1.00	1.50	ns
t_{pdLH} Propagation delay, low-to-high F.O. = four (4) CML loads	(See Figure 4a)		1.25	2.50		1.25	2.50	ns
t_{pdHL} Propagation delay, high-to-low F.O. = four (4) CML loads	(See Figure 4a)		1.50	3.00		1.50	3.00	ns
INPUT BUFFERS: Schmidt Trigger								**(U907-B20)**
I_{CC2} Power supply current	V_{IN} = 0.4V, V_{CC2} = 3.3V	1.17	1.40	1.75	1.17	1.40	1.75	mA
V_{TH}+ Input high threshold			1.66	1.85		1.66	1.85	V
V_{TH}− Input low threshold		0.98	1.09		0.98	1.09		V
I_{IL} Input low current (side)	V_{IN} = 0.4V, V_{CC2} =3.3V			−.45			−.45	mA
I_{IH} Input high current (side)	V_{IN} = 2.7V, V_{CC2} = Max			20			20	μA
I_{IL} Input low current (top)	V_{IN} = 0.4V, V_{CC2} = 3.3V			−.84			.84	mA
I_{IH} Input high current (top)	V_{IN} = 2.7V, V_{CC2} = Max			70			70	μA
FO Fanout		1		4	1		4	Unit load
t_{pdLH} Propagation delay, low-to-high F.O. = one (1) CML load	(See Figure 4a)		1.50	2.25		1.50	2.25	ns

DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions (cont.)

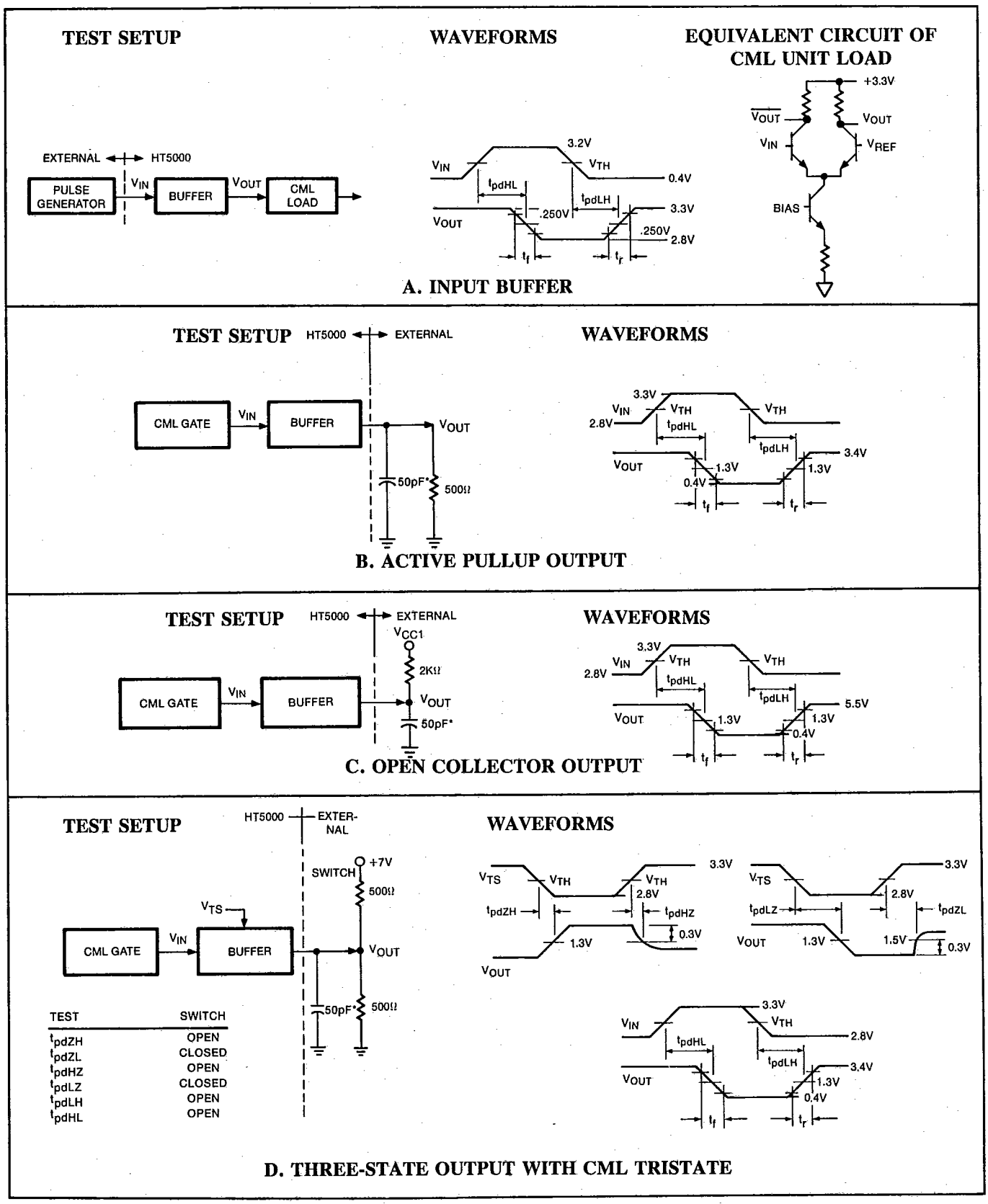
PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BUFFERS: (concluded)								**(U907-B20)**
t_{pdHL} Propagation delay, high-to-low F.O. = one (1) CML load	(See Figure 4a)		1.50	1.75		1.50	1.75	ns
t_{pdLH} Propagation delay, low-to-high F.O. = four (4) CML loads	(See Figure 4a)		2.00	4.00		2.00	4.00	ns
t_{pdHL} Propagation delay, high-to-low F.O. = four (4) CML loads	(See Figure 4a)		1.75	2.50		1.75	2.50	ns
OUTPUT BUFFERS: Totem Pole (Active Pullup)								**(U904)**
I_{CC1} Power supply current	V_{IN} = High, V_{CC1} = Max	.695	.775	.850	.625	.775	.950	mA
I_{CC2} Power supply current	V_{IN} = High, V_{CC2} = 3.3V	.900	1.000	1.100	.800	1.000	1.200	mA
V_{OL} Output low voltage	V_{CC1} = Min. I_{OL} = 8mA			500			400	mV
V_{OH} Output high voltage	I_{OH} = −400μA, V_{CC1} = Min	2.7			2.5			V
t_{tdLH} Propagation delay, low-to high output	(See Figure 4b)		3.5	5.0		3.5	5.5	ns
t_{pdHL} Propagation delay, high-to-low output	(See Figure 4b)		4.0	7.0		4.0	7.5	ns
OPEN COLLECTOR OUTPUT BUFFERS:								**(U903)**
I_{CC1} Power supply current	V_{IN} = High, V_{CC1} =Max	.900	1.000	1.100	.900	1.000	1.250	mA
I_{CC2} Power supply current	V_{IN} = High, V_{CC1} = 3.3V	.900	1.000	1.100	.800	1.000	1.200	mA
V_{OL} Output low voltage	V_{CC1} = Min, I_{OL} = 8mA			500			400	mV
I_{OH} Output high current	V_{OUT} = V_{CC1} Max, V_{CC1} = Min			0.1			0.1	mA
t_{pdLH} Propagation delay, low-to-high output	(See Figure 4c)		30.0	33.0		30.0	33.0	ns
t_{pdHL} Propagation delay, high-to-low output	(See Figure 4c)		8.0	10.0		8.0	12.0	ns

DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions (cont.)

PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
THREE-STATE OUTPUT BUFFERS:								**(U902)**
I_{CC1} Power supply current (U902)	V_{IN} = Low, V_{CC1} = Max	1.215	1.350	1.485	1.120	1.350	1.600	mA
I_{CC2} Power supply current (U902)	V_{IN} = Low, V_{CC2} = Max	.900	1.000	1.100	.700	1.000	1.250	mA
V_{OL} Output low voltage	V_{CC1} = Min. I_{OL} = 8mA			500			400	mV
V_{OH} Output high voltage	I_{OH} = −400μA, V_{CC1} = Min.	2.7			2.5			V
I_{OZL} Off-state output current, output low	V_{OUT} = 0.4V, V_{CC1} = Max			−20			−20	μA
I_{OZH} Off-state output current, output high	V_{OUT} = 2.7V, V_{CC1} = Max			20			20	μA
t_{pdLH} Propagation delay, low-to-high output	(See Figure 4d)		5.5	8.0		5.5	9.0	ns
t_{pdHL} Propagation delay, high-to-low output	(See Figure 4d)		6.0	10.0		6.0	12.0	ns
t_{pdZL} Propagation delay, HI-Z to low output	(See Figure 4d)		6.0	8.5		6.0	10.0	ns
t_{pdZH} Propagation delay, HI-Z to high output	(See Figure 4d)		6.0	10.0		6.0	12.0	ns
t_{pdLZ} Propagation delay, low to HI-Z output	(See Figure 4d)		4.5	7.0		4.5	8.0	ns
t_{pdHZ} Propagation delay, high to HI-Z output	(See Figure 4d)		3.0	4.0		3.0	5.0	ns
CML TO CML BUFFER:								**(U905)**
I_{CC2} Power supply current	V_{IN} = High, V_{CC2} = 3.3V	2.4	3.0	3.6	2.4	3.0	3.6	mA
V_{OL} Output low voltage	V_{CC2} = 3.3V, V_{IN} = Low			2.85			2.90	V
V_{OH} Output high voltage	V_{CC2} = 3.3V, V_{IN} = High	3.25			3.23			V
t_{pdLH} Propagation delay, low-to-high	V_{CC2} = 3.3V C_L = 5pF		2.0	2.5		2.0	3.0	ns
t_{pdHL} Propagation delay, high-to-low	V_{CC2} = 3.3V C_L = 5pF		2.0	2.5		2.0	3.0	ns

DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions (cont.)

PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSCEIVER BUFFERS:								(U909)
I_{CC1} Power supply current (U909)	V_{IN} = LOW, V_{CC1} = Max	1.215	1.350	1.485	1.120	1.350	1.600	mA
I_{CC2} Power supply current (U909)	V_{IN} = LOW, V_{CC2} = Max	.900	1.000	1.100	.700	1.000	1.250	mA
V_{OL} Output low voltage	V_{CC1} = Min, I_{OL} = 8mA			500			450	mV
V_{OH} Output high voltage	I_{OH} = −400μA, V_{CC1} = Min	2.7			2.5			V
I_{IL} Input low current (side)	V_{IN} =0.4V, V_{CC2} = Max			−.84			−.84	mA
I_{IH} Input high current (side)	V_{IN} = 2.7V, V_{CC2} =Max			20			20	μA
I_{IL} Input low current (top)	V_{IN} = 0.4V, V_{CC2} = 3.3V			−.84			−.84	mA
I_{IH} Input high current (top)	V_{IN} = 2.7V, V_{CC2} = Max			70			70	μA
t_{pdLH} Propagation delay, low-to-high output	(See Figure 4d)		5.5	8.0		5.5	9.0	ns
t_{pdHL} Propagation delay, high-to-low output	(See Figure 4d)		6.0	10.0		6.0	12.0	ns
t_{pdZL} Propagation delay, HI-Z to low output	(See Figure 4d)		6.0	8.5		6.0	10.0	ns
t_{pdZH} Propagation delay, HI-Z to high output	(See Figure 4d)		6.0	10.0		6.0	12.0	ns
t_{pdLZ} Propagation delay, low to HI-Z output	(See Figure 4d)		4.5	7.0		4.5	8.0	ns
t_{pdHZ} Propagation delay, high to HI-Z output	(See Figure 4d)		3.0	4.0		3.0	5.0	ns



*Includes jig and probe capacitance.

Figure 4. Test Configurations

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LSTTL GATE ARRAY HT5000

UNDERSTANDING CURRENT MODE LOGIC

From the earliest days of bipolar technology, circuit designers noted that current switches are faster than their voltage counterparts. A logic family based on steering currents, without altering their values, is intrinsically faster than one based on voltage-switching techniques. That is the reason ECL and CML circuits are generally faster than TTL.

Both ECL and CML use a differential pair of NPN transistors for switching current. Circuit diagrams of the basic gates look similar (Figure 5), but they differ in operation.

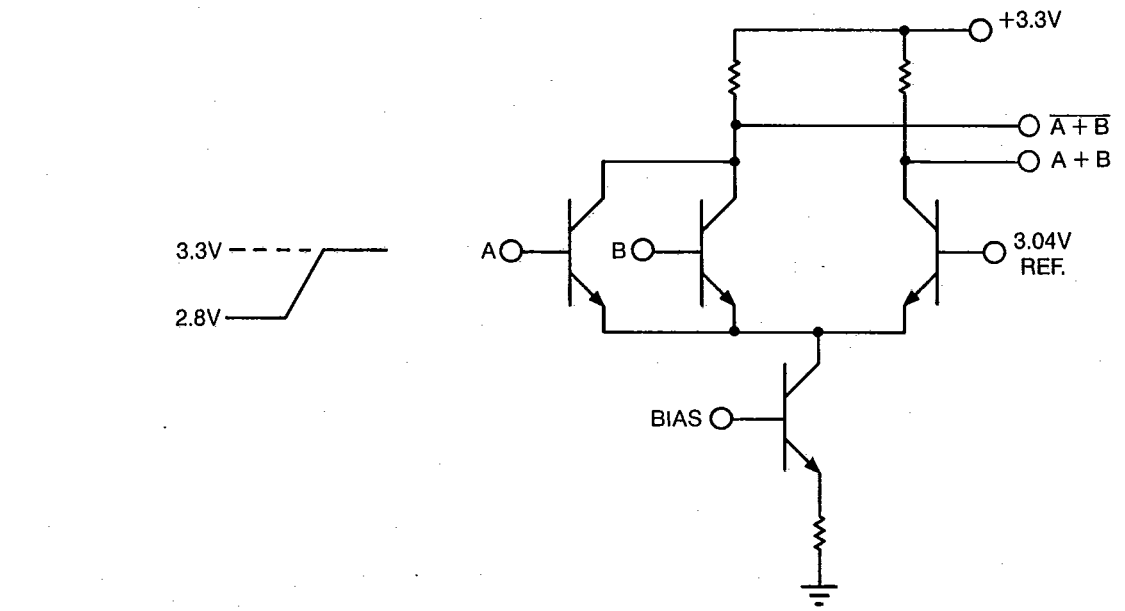
The reference voltages represent the center point of the logic swing. In ECL, with a −1.29 volt reference and a nominal collector voltage swing of .85 volt, the collector-base junction on the signal input side goes to 0 volts under worst case conditions. On the reference side, that junction always remains reverse-biased by .44 volt. Thus, the transistors never saturate. However, the emitter-follower is always on, increasing power consumption. The use of the emitter follower output dictates the ECL operating levels. Rather than rising all the way to the positive power supply voltage, the ECL output high level stays a diode drop below.

In contrast, CML employs a reference voltage of .25 volt below the positive supply and a signal swing of .5 volt. The collector-base junction of the input transistor then becomes forward-biased by .5 volt at most, a condition termed soft saturation because negligible forward injection across the junction takes place. With almost no excess charge stored in the base in soft saturation, switching speed is comparable with that of ECL. At the same time, an off transistor cuts off completely. The additional power of ECL's emitter-follower driver is eliminated.

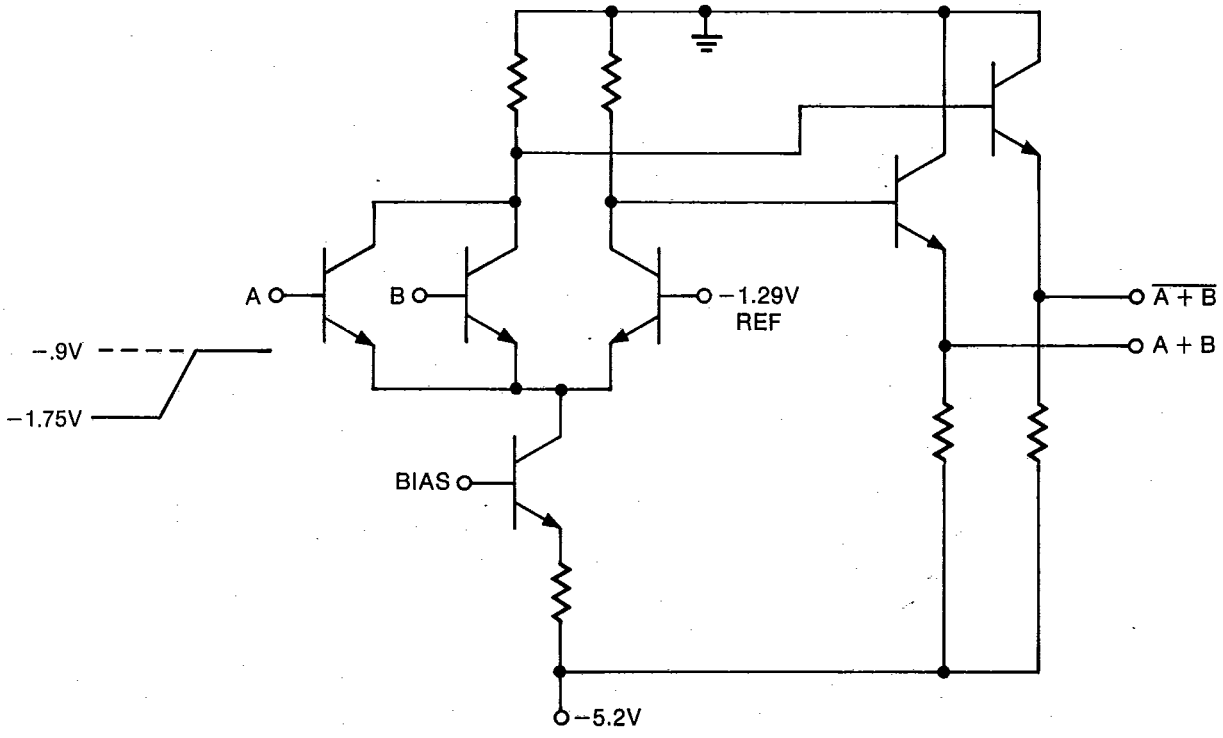
The single differential pair of a CML gate drives following gates directly from either collector. Both true and complement outputs are available with nearly equal speed. Gate delays are essentially a single transistor delay because most logic functions are implemented with a single differential pair as the primary switch. Series gating generates many useful logic functions with a single logic-gate delay, as in the Master Slave D Flip Flop shown in Figure 6. The 3.3 volt supply is the minimum voltage that supports the series-gating logic structure, so CML power consumption is at an absolute minimum without sacrificing any speed.

In CML circuits intended for gate array or VLSI custom chip use, currents are set on chip by a voltage and temperature compensated reference regulator. Reliable operation over commercial and military temperature ranges is achieved.

For further information, ask your Honeywell representative for the article reprints entitled, "Honeywell High Speed Digital Technology".



(A) BASIC CML OR/NOR LOGIC GATE



(B) BASIC ECL OR/NOR LOGIC GATE

Figure 5. Basic Gates

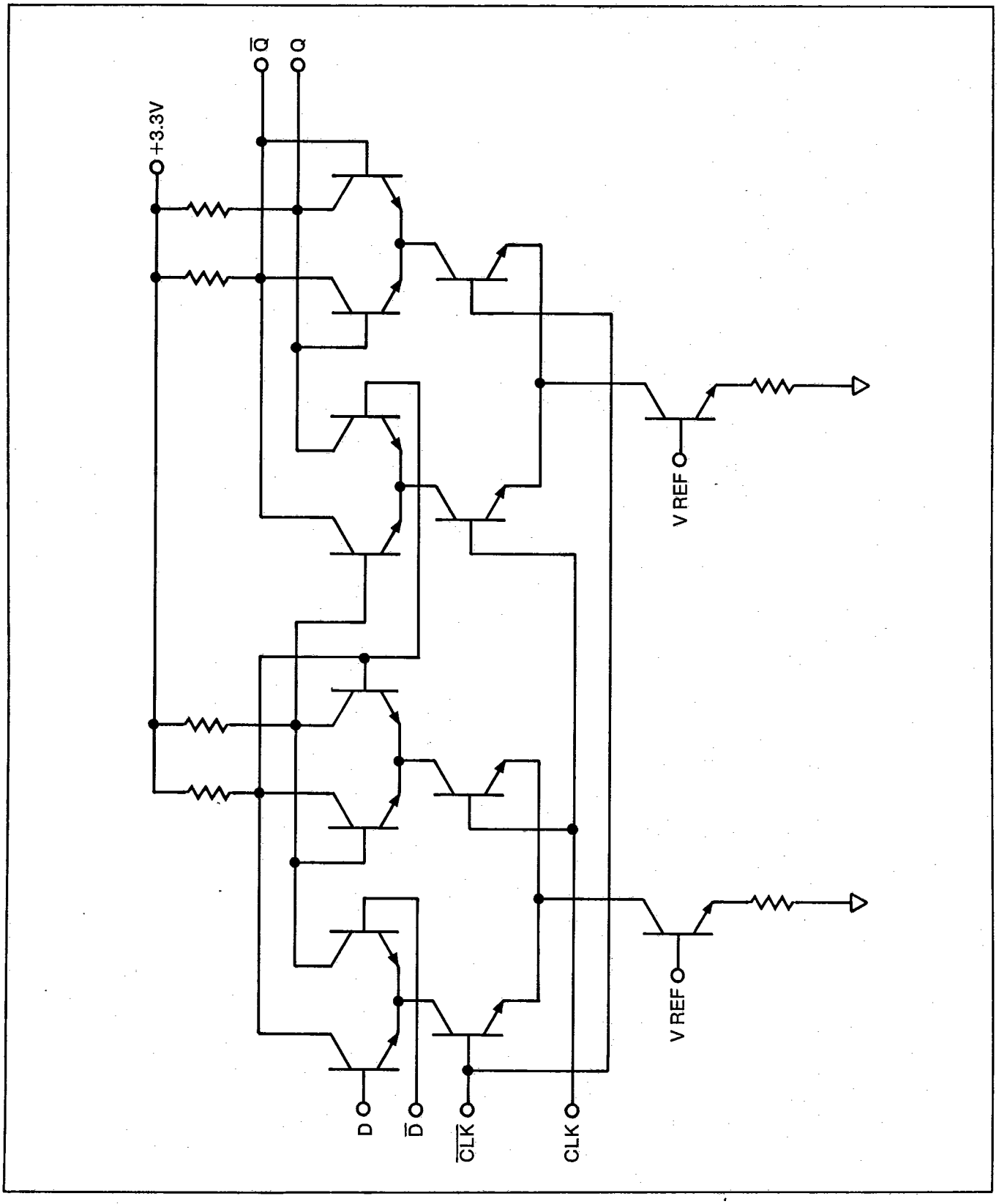


Figure 6. CML Master Slave D Flip Flop

PACKAGING

The HT5000 Gate Array is offered in several high density packages. Among them is the 152-pin-grid package shown in Figure 7. Also available are a 144-pin-grid package (cavity up) and a 148 pin surface mounted leadless-chip-carrier package. Leaded-chip-carrier packages for high reliability military applications are available upon request.

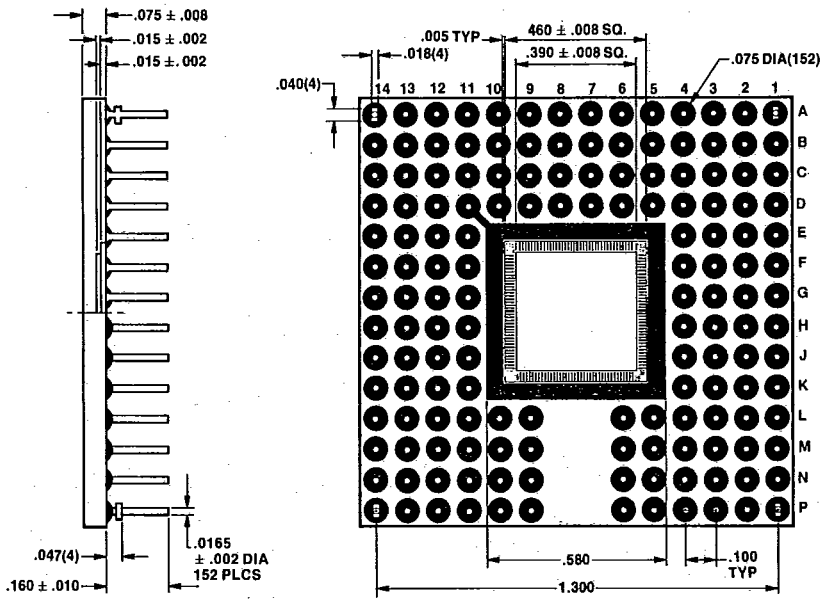
Figure 7 also shows that the die is mounted cavity down to provide an elevated primary heat conducting surface ideally suited to forced-air cooling. The central die cavity is square to provide matched lead lengths and voltage drops. Hermeticity is provided with a solder-sealed lid.

The package has 128 I/O pins, 24 VCC1, VCC2, and ground pins. All pins are positioned in a uniform rectangular grid on 100 mil centers. The HT5000 die is attached to the ceramic substrate using a eutectic die attach to provide a low thermal resistance path. Thermal resistance from junction to case is less than 5 Degrees C/Watt.

HEAT SINKING

The HT5000 Gate Array was designed to be used in either forced-air cooled or convection cooled systems. Maximum junction temperatures of 175 degrees C are allowed. Junction to case thermal resistance is typically less than 5 degrees C/watt, while the junction to ambient thermal resistance is a function of heat sink mounting technique, air flow, and surrounding electronics. See Figure 8.

HT5000 Application Note #2 entitled "Packaging and Thermal Considerations", describes how to calculate thermal resistance and which heat sinks are appropriate.



NOTES:

- Pins D4, D11, L4, and L11 are connected to Die Attach Area
- TTL GND Pins: L5, L6, L9, D9, D7, D6
  TTL VCC_1 Pins: D5, K4, K11, D10
  CML GND Pins: G4, D4, D11, L4, L11, G11
  CML VCC Pins: F4, J4, J11, H11, F11, E11, E4
- Tolerance: ±0.005 unless otherwise specified
- Pins brazed to metallized ceramic using Ag/Cu Eutectic
- Pin Material: Kovar or Alloy 42 + Nickel + Gold (60 Microinch minimum)
- Metallization: Refractory Metal + Nickel + Gold (60 Microinch minimum)
- Material: Ceramic, AL_2O_3 Black

Figure 7. PGAB Package Dimensions

Order Code : GC

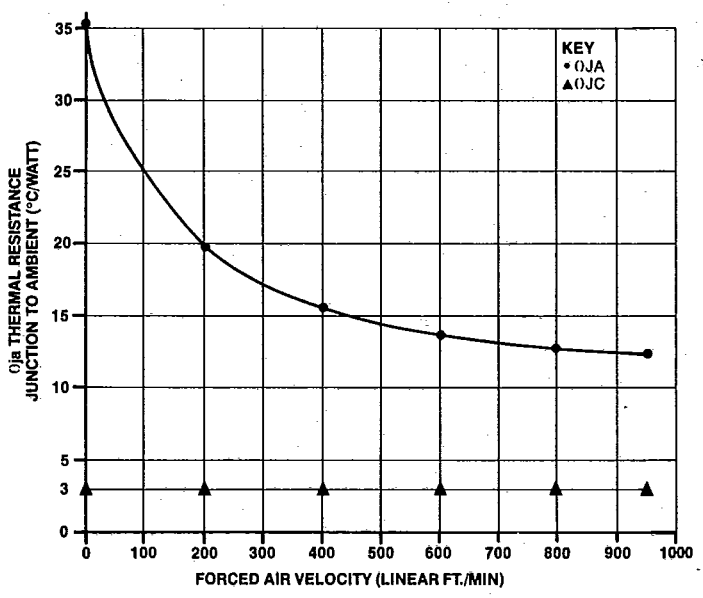


Figure 8. Thermal Characteristics of PGAB Package

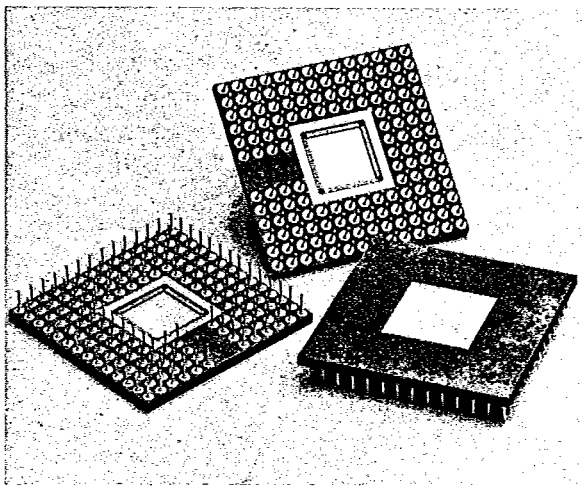


Figure 9. HT5000 PGAB Package

Together, we can find the answers.

Honeywell

ORDERING INFORMATION

For additional information on the HT5000 and other digital bipolar products from Honeywell contact:

HONEYWELL DIGITAL PRODUCT CENTER
1150 E. Cheyenne Mtn. Blvd.,
Colorado Springs, Colorado 80906
1-800-328-5111 ext. 3402

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085—March 1985