HT82003

20-Stage Ripple Carry Binary Counter

Features

- Operating voltage: 2.4V~5.0V
- 20 stage ripple binary counter
- Fully static operation
- Common reset
- Adjustable initial counter value
- 3-chip selection output pins
- Standardized symmetrical output characteristics
- Selectable external memory type: 1Mb/2Mb/4Mb/8Mb
- Offset for the first 10 stage outputs

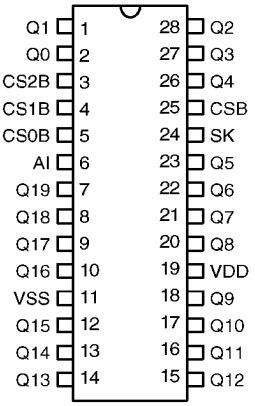
Applications

- Expandable memory interfaces
- Control counters
- Timers
- Frequency dividers

General Description

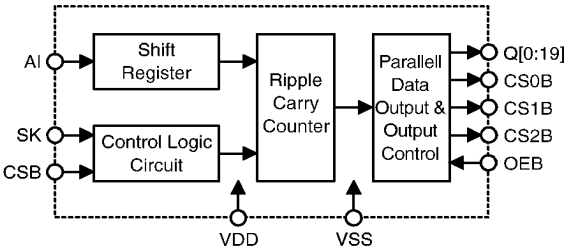
The HT82003 is a 20-stage ripple carry binary counter. All of the 20 stages are master-slave flip-flops. The counter advances one count on a negative transition of an input clock pulse. A high level on the CSB line will reset the 20 stages to their zero states. A Schmitt trigger action on an input line permits input signals of a wide range of rise and fall time. The HT82003 is designed specially for HT82013 with an external memory interface. Its initial counter value as well as interfaced external memory type can be user-defined. A maximum of three external memory chip interfaces can be used for three-chip selection pins.

Pin Assignment

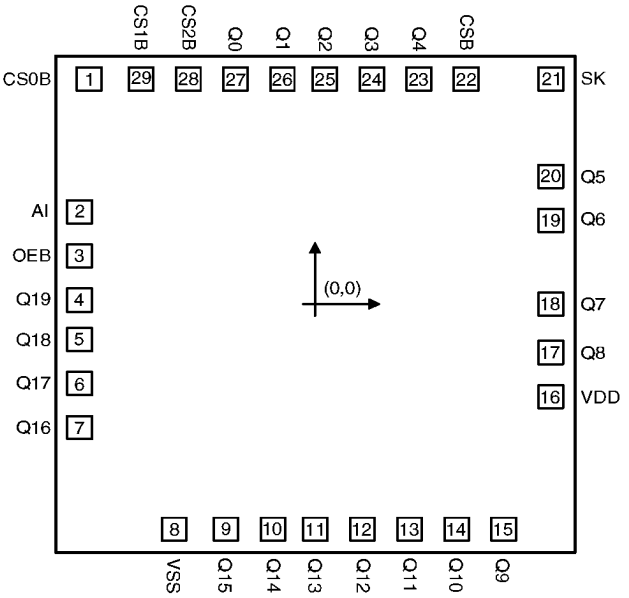


HT82003
– 28 SDIP/SOP

Block Diagram



Pad Coordinates



Chip size: 113 × 115 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Unit: mil

Pin No.	X	Y	Pad No.	X	Y
1	–48.83	51.37	16	50.67	–21.08
2	–50.67	21.53	17	50.67	–11
3	–50.67	11.45	18	50.67	–0.92
4	–50.67	1.37	19	50.67	19.24
5	–50.67	–8.71	20	50.67	29.32
6	–50.67	–18.79	21	50.67	51.37
7	–50.67	–28.87	22	32.72	51.37
8	–30.24	–51.41	23	22.64	51.37
9	–19.8	–51.41	24	12.56	51.37
10	–9.72	–51.41	25	2.48	51.37
11	0.36	–51.41	26	–7.61	51.37
12	10.44	–51.41	27	–17.69	51.37
13	20.52	–51.41	28	–27.77	51.37
14	30.6	–51.41	29	–37.85	51.37
15	40.68	–51.41			

Pad Description

Pad No.	Pad Name	I/O	Internal Connection	Description
28, 29, 1	CS2B~CS0B	O	CMOS	Chip selection output for an external memory
2	AI	I	CMOS	Serial data input for setting an initial output of LSI
3	OEB	I	Pull-Low	CS0B~CS2B output enable controls
4~7	Q19~Q16	O	CMOS	Ripple counter data output
8	VSS	—	—	Negative power supply (GND)
9~15	Q15~Q9	O	CMOS	Ripple counter data output
16	VDD	—	—	Positive power supply
17~20	Q8~Q5	O	CMOS	Ripple counter data output
21	SK	I	CMOS	Serial clock input, schmitt trigger input
22	CSB	I	CMOS	LSI chip enabled, active low
23~27	Q4~Q0	O	CMOS	Ripple counter data output

Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 6V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –20°C to 70°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

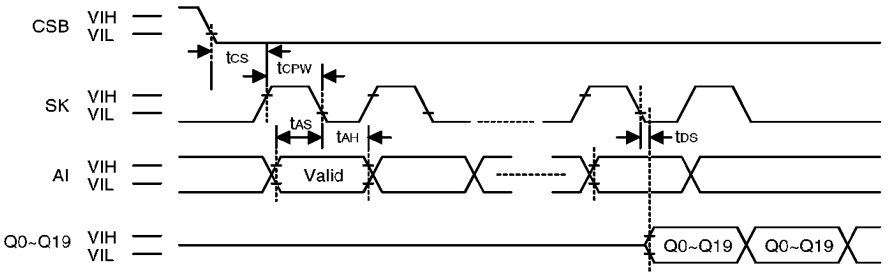
(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	3	5	V
I_{STB}	Standby Current	5V	No load	—	1	5	μA
I_{OL1}	Sink Current (Q0~Q19 or CS0B~CS2B)	5V	V_{OL1}=0.5V	1.5	2.8	—	mA
I_{OH}	Source Current (Q0~Q19 except Q9 or CS0B~CS2B)	5V	V_{OH}=4.5V	–0.6	–0.9	—	mA
R_{PL}	OEB Pull-Low Resistor	5V	V_{IH}=5V	50	—	200	kΩ
V_{IH}	High Level Input Voltage	5V	—	$0.8V_{DD}$	—	5V	V
V_{IL}	Low Level Input Voltage	5V	—	0	—	$0.2V_{DD}$	V
I_{OL2}	Q9 Sink Current	5V	V_{OL2}=0.5V	4.5	7.5	—	mA

A.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{CS}	CSB Setup Time	5V	—	1	—	—	μs
t_{CPW}	Clock Pulse Width	5V	—	2	—	—	μs
t_{AS}	Address Setup Time	5V	—	2	—	—	μs
t_{AH}	Address Hold Time	5V	—	2	—	—	μs
t_{DS}	Data Setup Time	5V	—	—	—	1	μs



Functional Description

The HT82003 is a 20-stage ripple carry binary counter specially designed for expanded address buses. The interface memory type, chip selection output and initial counter value are all programmable. The maximum size of an external memory is 8Mb×3. The LSI is designed specially for HT82013 as an address expander.

Parameter setting

The HT82003 enters an initial setting when the state of CSB changes from high to low. Data to be set includes an initial counter value, chip selection output and external memory type. Once they are set, their results are serially written to a parameter register by the SK control signal. Data on the AIN pin are clocked into the device serially at the falling edge of the SK signal when CSB is low. After 32 clock pulses, the values of the parameters will be set and written in, and the value (Q0~Q19) of the counter will be incremented at the falling edge of every SK signal (refer to Figure 1).

- Initial value

  The initial values of Q0~Q19 are written into the device at the first 20-clock pulses and then output at the falling edge of the 25th clock pulse. Q0~Q19 can address up to 8Mb when the HT82003 is used as expanded addresses. Of Q0~Q19, Q0~Q9 are their offset. In other words, the initial values of Q0~Q9 are always zero.

- Chip selection output

  The chip selection output is written into the device at the falling edge of the 21st (S0) and 22nd (S1) clock pulses. At the falling edge of the 25th clock pulse, the chosen chip selection pin changes from high to low. The remaining chip selection pins always stay high. S0 and S1 define the active pin of the chip selection pins, namely CS0B~CS2B as shown in the following table:

S0	0	1	0	1
S1	0	0	1	1
Pin	CS0B	CS1B	CS2B	CS0B

The output of $CS_{N+1}B$ will replace the output of CS_NB once the outputs of Q0~Q19 exceed the maximum address of the selected external memory (refer to Figure 2).

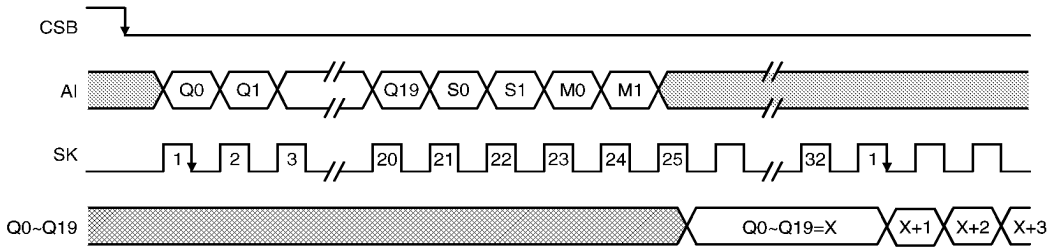


Figure 1

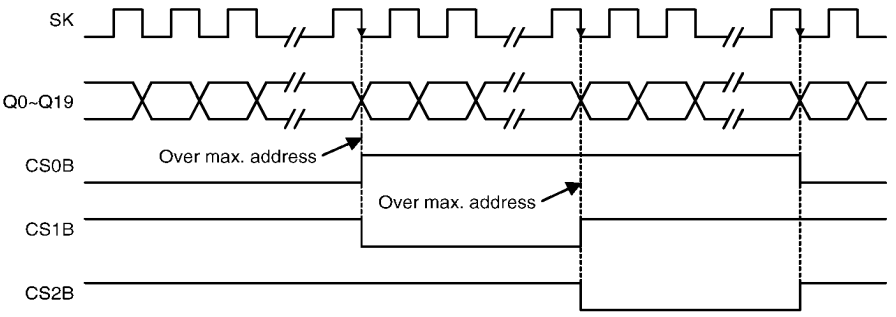


Figure 2

- Memory type setting

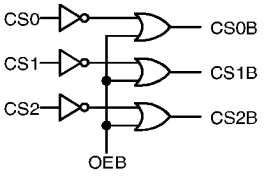
  The memory type setting is written into the device at the falling edge of the 23rd (M0) and 24th (M1) clock pulses. M0 and M1 define the memory type as shown:

M0	0	1	0	1
M1	0	0	1	1
Type	1Mb	2Mb	4Mb	8Mb
Address Buses	Q0~Q16	Q0~Q17	Q0~Q18	Q0~Q19

  After the memory type is set, the output of the chip selection will change to the next pin after MSB of the address bus changes to low.

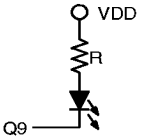
- Disable the chip selection output

  The OEB pad includes an internal pull-low resistor. All the chip selection pins (CS0B~CS2B) will be output high when OEB connects to VDD.



- LSI active display

  The HT82003 provides an extra sink current pin of Q9 (7.5mA typ.) to drive an LED or other indicators.



Application Circuit