

HT8658/HT8659 Voice Recorder (DRAM)

Features

- Operating voltage: 4.5V~5.5V
- · ADM coding algorithm
- DRAM options:
 - 256×4-bit
 - 1M×3-bit
- Built-in 2-stage MIC amplifier
- · Built-in low pass filter

- Data rate options (bits per second):
 - 32Kbps
 - 22Kbps
 - 16Kbps
 - 11Kbps
- Status LED indicator
- Auto playback

Applications

- · Message box
- Recorder

Toys

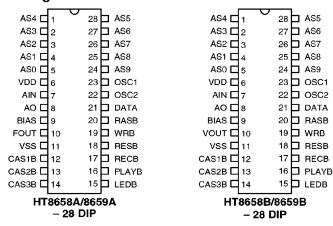
General Description

The HT8658/HT8659 are single chip CMOS LSI designed for applications on recording sounds using an ADM coding technology. The HT8658 and HT8659 have almost the same functions apart from the reset time. The reset time of the HT8658 has to be over 4 seconds while that of the HT8659 should be over 2 seconds.

Blocks within each chip include a DRAM interface circuit, signal amplifier, 8-bit ADC and internal low pass filter. Encoded data are stored

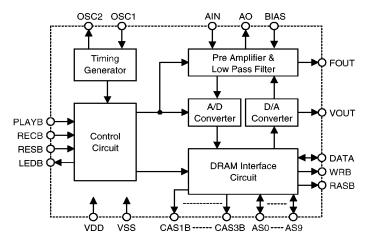
in the external DRAMs and played back after the PLAYB pin is triggered. Each IC provides four kinds of sampling rate that can be selected namely, 32K/22K/16K/11Kbps (bits per second). A higher sampling rate will generate sounds of better quality but sacrifice recording time. With such a powerful built-in circuit, only few components are required for normal applications. Each IC is offered in a dice form or 28-pin DIP.

Pin Assignment





Block Diagram



Pad Coordinates Unit: mil

	OSC1				RASB			Pad No.	X	Y	Pad No.	X	Y	
	29 28	3 27			26	25	WRB	1	-62.92	29.69	16	62.37	-70.76	
						24	RESB	2	-62.92	19.30	17	62.37	-54.61	
								3	-62.92	8.37	18	62.71	-44.84	
• • • •								4	-62.92	-2.30	19	62.71	-34.81	
AS9 AS8	1							5	-62.92	-13.22	20	62.71	-23.04	
	3		†			23	DEOD	6	-62.92	-23.89	21	62.71	-13.94	
AS7 AS6	4		(0,0)	•		22		7	-62.92	-34.81	22	62.71	-2.93	
AS5	5		•		21 L				8	-62.92	-45.48	23	62.71	8.88
AS4	6					CAS3B	9	-62.92	-56.40	24	62.71	58.69		
AS3	7					19	CAS2B	10	-62.92	-67.07	25	62.71	70.34	
AS2	8					18	CAS1B	11	-46.43	-70.76	26	50.98	70.34	
AS1	9					17	vss	12	-38.78	-70.76	27	-45.07	70.51	
AS0	10			_				13	33.55	-70.76	28	-54.93	70.51	
A30	ш	11 12			14 15			14	43.16	-70.76	29	-62.58	70.51	
		AIN VDD		AO	VOUT BIAS	FOUT		15	52.76	-70.76				

Chip size: $138 \times 154 \text{ (mil)}^2$

 $[\]ast$ The IC substrate should be connected to VDD in the PCB layout artwork.



Pad Description

Pad No.	Pad Name	1/0	Internal Connection	Description
1	AS9	I/O	Pull-High CMOS	Input: For IC test only Output: Address output for DRAM of 1Mb and column address strobe for DRAM of 256Kb
2	AS8	I/O	Pull-High CMOS	Input: For IC test only Output: Address output to DRAM
3	AS7	I/O	Pull-High CMOS	Input: For IC test only Output: Address output to DRAM
4	AS6	I/O	Pull-High CMOS	Input: For IC test only 1: For IC test only 0: Not applicable Output: Address output to DRAM
5	AS5	I/O	Pull-High CMOS	Input: DRAM type selection: 1: 256Kb (without external pull-low resistors) 0: 1Mb (with an external pull-low resistor) Output: Address output to DRAM
6	AS4	I/O	Pull-High CMOS	Input: Manual/Auto playback selection: 1: Manual (without external pull-low resistors) 0: Auto (with an external pull-low resistor) Output: Address output to DRAM
7, 8	AS3, AS2	I/O	Pull-High CMOS	Input: DRAM chip number selection (refer to the functional description) Output: Address output to DRAM
9, 10	AS1, AS0	I/O	Pull-High CMOS	Input: Sampling rate selection (refer to the functional description) Output: Address output to DRAM
11	VDD	I	_	Positive power supply
12	AIN	I	_	Pre-amplifier input pin
13	AO	О	_	Pre-amplifier output pin Amplifier gain should be adjusted between AIN and AO by a resistor
14	BIAS	I	_	For internal OP bias de-coupling
15	VOUT	О	_	Audio signal output (non-filtered, direct output)
16	FOUT	О	_	Audio signal output through an internal low-pass filter
17	VSS	I		Negative power supply (GND)



Pad No.	Pad Name	I/O	Internal Connection	Description
18~20	CAS1B~ CAS3B	О	CMOS	Column address strobe for DRAM1~DRAM3
21	LEDB	О	Open Drain NMOS	Status indicator when the chip is active
22	PLAYB	I	Pull-High	Play/Pause trigger input (toggle function)
23	RECB	I	Pull-High	Record/Pause trigger input (toggle function)
24	RESB	I	Pull-High	Reset the system or the play counter
25	WRB	О	CMOS	Write enable signal output for DRAM interface
26	RASB	О	CMOS	Row address strobe output for DRAM interface
27	DATA	I/O	_	Encoded data I/O pin
28 29	OSC2 OSC1	O I	_	Oscillation external resistor connecting pin

Absolute Maximum Ratings*

Supply Voltage0.3 to 6V	Storage Temperature50°C to 125°C
Input Voltage V _{SS} -0.3 Vto V _{DD} +0.3V	Operating Temperature20°C to 70°C

^{*}Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

(Ta=25°C)

G h - 1	Parameter	Te	est Conditions	Min.	т	Max.	Unit
Symbol	Parameter	V_{DD}	Conditions	wiin.	Тур.	Max.	
$V_{ m DD}$	Operating Voltage	_	<u>—</u>	4.5	5.0	5.5	V
${ m I}_{ m DD}$	Operating Current	5V	No load, $ m f_{OSC}$ =384kHz	_	0.8	2.0	mA
I_{STB}	Standby Current	5V	<u>—</u>	_	40	100	μА
$I_{ m OL}$	LED Sink Current	5V	$V_{\rm OL}$ =0.5 V	3.0	5.0	_	mA
V_{IH}	"H" Input Voltage	_	<u>—</u>	$0.7V_{ m DD}$	_	$ m V_{DD}$	v
V_{IL}	"L" Input Voltages		_	0	_	$0.2 V_{ m DD}$	V
V _{OUT}	Max. Vout Output Voltage	5V	R_L >50k Ω	1.5			V_{P-P}
fosc	Oscillating Frequency	5V	R _{OSC} =91kΩ	_	384	_	kHz



Functional Description

The HT8658/HT8659 are single chip LSIs with an external DRAM (dynamic random access memory). They are designed for applications on recording sounds. The recording length is determined by the data rate and the size of the external memory. The type and the amount of DRAM, as well as the operation mode and sampling rate are determined by the connection of the AS0~AS6 pins. The HT8658/8659 provide two audio outputs. One is filtered by an internal low pass filter to improve sound quality and to minimize external required components. The other is non-filtered and a voice signal can be filtered with an external circuit to determine the audio cut-off frequency as well as band width. The two chips have the same functions except for the reset time as shown:

Name	Reset Time (Minimum)
HT8658	$4~{ m seconds}$
HT8659	2 seconds

Initial setting of operation mode

The HT8658/HT8659 load the statuses of the AS0~AS6 pins into a mode register after power is initially turned on or the system is reset. These pins are internally built with pull-high resistors so that all inputs with "1" are the default value of the mode register. External pull-low resistors which are tied to the AS0~AS6 pins defines the operation mode of the ICs as shown in the following table:

AS0	AS1	AS2	AS3	AS4	AS5	AS6	Function Description
0	0	X	X	X	X	X	Data rate: 32Kbps
1	0	X	X	X	X	X	Data rate: 22Kbps
1	1	X	X	X	X	X	Data rate: 16Kbps
0	1	X	X	X	X	X	Data rate: 11Kbps
X	X	0	0	X	X	X	DRAM chip number: 4 pcs.
X	X	1	0	X	X	X	DRAM chip number: 3 pcs.
X	X	0	1	X	X	X	DRAM chip number: 2 pcs.
X	X	1	1	X	X	X	DRAM chip number: 1 pc.
X	X	X	X	1	X	1	Operation mode: Normal mode
X	X	X	X	0	X	1	Operation mode: Auto play back mode
X	X	X	X	1	X	0	Operation mode: Not applicable
X	X	X	X	0	X	0	Operation mode: Not applicable
X	X	X	X	X	1	X	DRAM type: 256Kb
X	X	X	X	X	0	X	DRAM type: 1Mb

Notes: 1. "0" connects an external pull-low resistor to ASn, where n=0~6

^{2. &}quot;1" connects no external pull-low resistor to ASn, where n=0~6 $\,$

^{3. &}quot;X" means don't care



Recording capacity

The HT8658/HT8659 offer four kinds of voice sampling rate namely, 32Kbps, 22Kbps, 16Kbps and 11Kbps (based on a system frequency of 384kHz), selectable by the connection of the AS0 and AS1 pins. The voice sampling rate determines the recording capacity of the ICs in addition to the type and amount of DRAM. A higher sampling rate will generate sounds of better quality but will shorten the recording time.

Sampling Rate	DRAM Size (Maximum)	Recording Time
32Kbps	$1 \text{Mb} \times 3$	94 seconds
$22 { m Kbps}$	1Mb×3	136 seconds
16Kbps	1Mb×3	188 seconds
11Kbps	1Mb×3	272 seconds

Recording Time

Memory selection

The HT8658/HT8659 provide a DRAM interface circuit. The type and the size of the DRAM determines the recording length of the ICs at a designated sampling rate. There are two kinds of DRAM namely, 256Kb and 1Mb, selectable by the connection of the AS5 pin. The ICs can interface with a maximum of 4 DRAMs for the 256Kb type but 3 DRAMs for the 1Mb type. The size of the DRAMs is determined by the connection of the AS2 and AS3 pins.

AS5	AS3	AS2	Memory Size
1	1	1	256Kb×1
1	1	0	256Kb×2
1	0	1	256Kb×3
1	0	0	256Kb×4
0	1	1	1Mb×1
0	1	0	1Mb×2
0	0	1	1Mb×3
0	0	0	1Mb×3

Notes: 1. "0" connects an external pull-low resistor to ASn, where n=2, 3, or 5

Record function

The HT8658/HT8659 enter the recording state from the standby state when the REC key is triggered and the memories are not full. In the recording state, sounds coming from an external microphone are coded by an internal ADM (adaptive delta modulation) algorithm and saved in an external memory until the memories are all full or the REC key is retriggered.

If the REC key is retriggered in the process of recording, recording will pause and the recording counter will stop counting. At this time, if the memories are not full and the REC key is triggered again, the IC will continue recording sounds from the pause position. Once the memories are full, recording will be terminated and any further re-trigger to the REC key will be ignored.

^{2. &}quot;1" connects no external pull-low resistors to ASn, where n = 2, 3 or 5



After recording is stopped, the HT8658/HT8659 will automatically play back the recorded sounds in the AUTO PLAY mode. However, in the normal mode, the chip will play back the recorded sounds if the PLAY key is manually triggered.

Play function

The HT8658/HT8659 provide two kinds of playing modes namely, normal mode and AUTO PLAY mode. In the normal mode, the ICs will play back the recorded sounds when recording is terminated and the PLAY key is triggered. In the AUTO PLAY mode, once recording is terminated, they will automatically play back the recorded sounds without manually triggering the PLAY key. While in the process of playing sounds, triggering the PLAY key will pause the play back and the playing counter. To resume playing back, simply retrigger the PLAY key. Playing back will start at the pause position.

AS4	AS6	Function
1	1	Normal mode
0	1	AUTO PLAY mode
1	0	Not applicable
0	0	Not applicable

Notes: 1. "0" connects an external pull-low resistor to ASn, where n=4, 6

2. "1" connects no external pull-low resistor to ASn, where n=4, 6

System reset

The reset time of the HT8658 and HT8659 is different. The HT8658 will reset the system if the RES key is pressed for more than 4 seconds and reset the playing counter if the RES key is pressed less than 4 seconds. The HT8659, on the other hand, will reset the system if the RES key is pressed for over 2 seconds and reset the playing counter if the RES key is pressed less than 2 seconds. Once the playing counter is reset, the ICs will play back the recorded data from the beginning by triggering the PLAY key. All of the recorded data will be deleted after the system is reset.

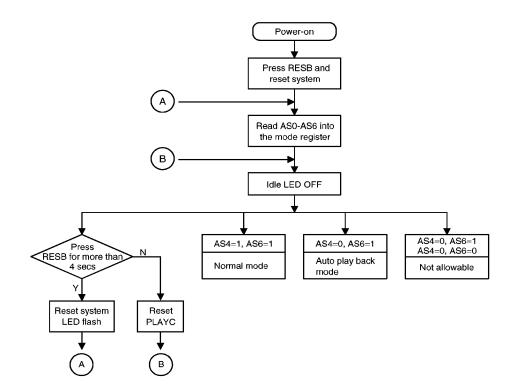
Indicate function

The HT8658/HT8659 provide an LEDB pin to indicate the operation status of the chip through an external LED display. The LEDB pin is of high impedance and an external LED is switched off in the standby state. LEDB, on the other hand, remains at a low level and LED is turned on in the recording state. In the playback state, LED flashes with the volume of the output sounds. When the system is reset, it flashes at a 2Hz rate.



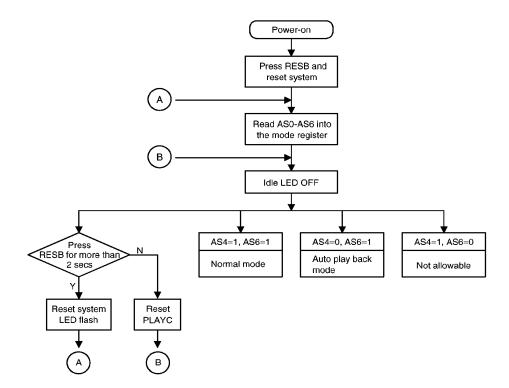
Operation flowchart

• HT8658



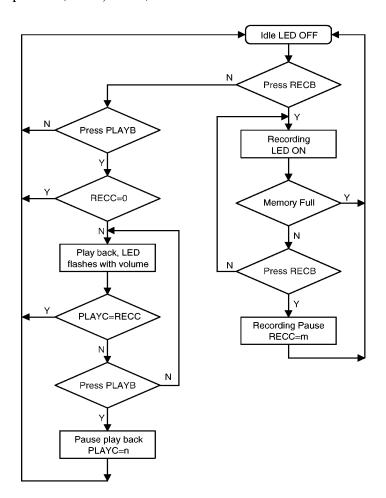


• HT8659



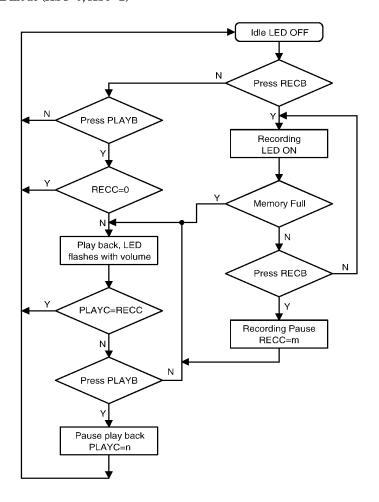


• Normal mode operation (AS4=1, AS6=1)





• Auto play-back mode (AS4=0, AS6=1)



Notes: 1. RECC: Recording counter

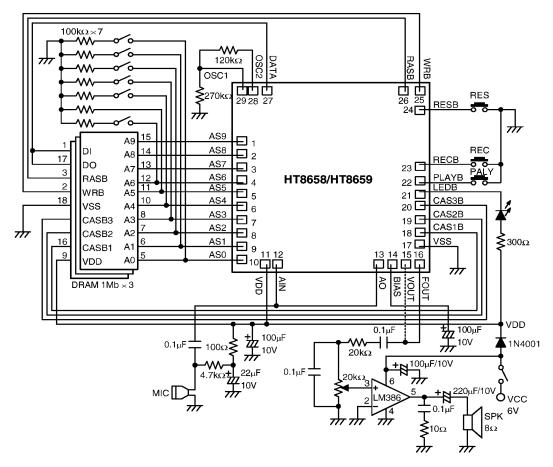
 $2.\ PLAYC: Play-back\ counter$

3. m, n: DRAM addresses



Application Circuits

With a DRAM interface of 1Mb (Chip form)

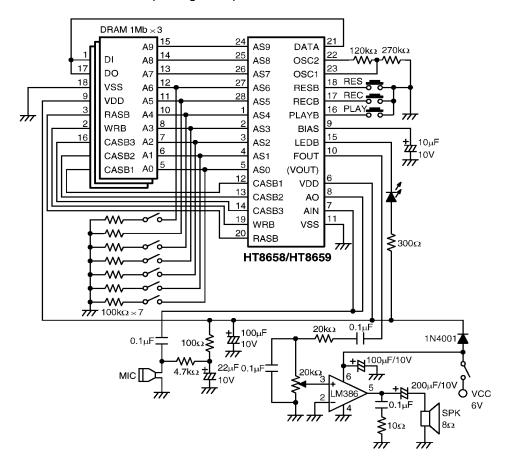


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12

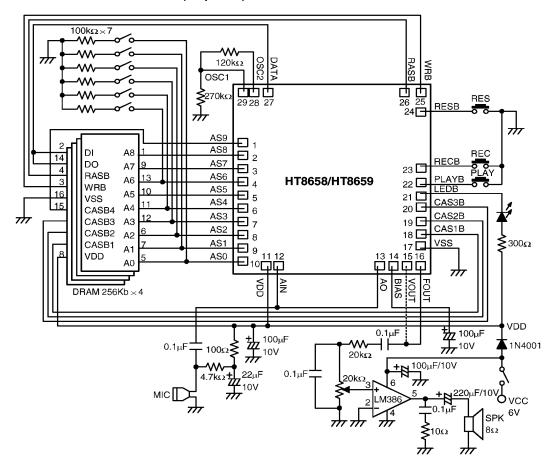


With a DRAM interface of 1Mb (Package form)





With a DRAM interface of 256Kb (Chip form)



* The IC substrate should be connected to VDD in the PCB layout artwork.

14



With a DRAM interface of 256Kb (Package form)

