HARRIS SEMICONDUCTOR

HUF4410DY

ADVANCE INFORMATION

December 1997

10A, 30V, 0.0135 Ohm, N-Channel, Logic Level Power MOSFET

Features

- **Logic Level Gate Drive**
- **10A, 30V**
- **$r_{DS(ON)}$ = 0.0135Ω at I_D = 10A, V_{GS} = 10V**
- **$r_{DS(ON)}$ = 0.020Ω at I_D = 8A, V_{GS} = 4.5V**
- ***Temperature Compensating* PSPICE Model**
- ***Thermal Impedance* SPICE Model**
- **Related Literature**
  - **TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"**

Description

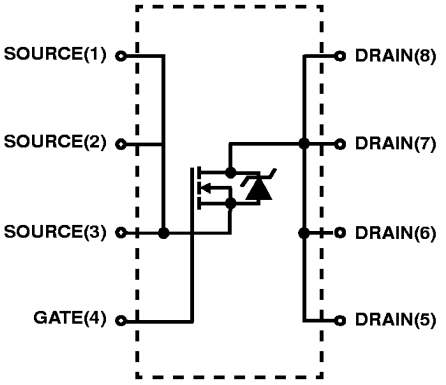
This power MOSFET is manufactured using an innovative process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF4410DY	SO-8	XXXXXX

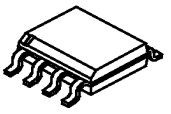
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF4410DYT.

Symbol



Packaging

SO-8



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4468.1**

Absolute Maximum Ratings $T_J = 25^oC$, Unless Otherwise Specified

Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous (Figure 2)	I_D	10	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 16,17	
Power Dissipation	P_D	2	W
Derate Above 25^oC		0.02	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	1	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 30V, V_{GS} = 0V, $T_J = 55^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V	-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 5A, V_{GS} = 4.5V	-	0.015	0.020	Ω
		I_D = 10A, V_{GS} = 10V	-	0.011	0.0135	Ω
Turn-On Time	t_{ON}	V_{DD} = 25V, $I_D \cong$ 1A, R_L = 25Ω, V_{GEN} = 10V, R_G = 6Ω	-	-	36	ns
Turn-On Delay Time	$t_{d(ON)}$		-	15	-	ns
Rise Time	t_r		-	9	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	-	ns
Fall Time	t_f		-	20	-	ns
Turn-Off Time	t_{OFF}		-	-	135	ns
Total Gate Charge	Q_g	V_{DS} = 15V, V_{GS} = 10V, $I_D \cong$ 10A		35	60	nC
Gate-Source Charge	Q_{gs}			7.5		nC
Gate-Drain Charge	Q_{gd}			5.8		nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	3200	-	pF
Output Capacitance	C_{OSS}		-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	200	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse Width <10s (Figure 3) Device Mounted on FR-4 Material	-	-	50	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 2.3A	-	0.7	1.1	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2.3A, dI_{SD}/dt = 100A/μs	-	-	80	ns