

75A, 30V, 0.0055 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs


These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76143.

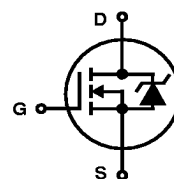
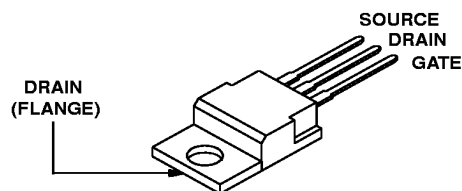
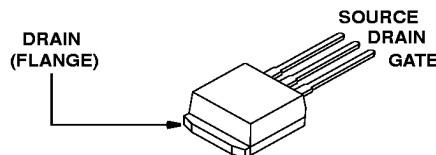
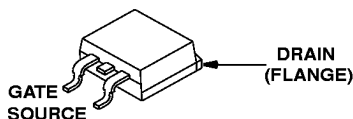
Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76143P3	TO-220AB	76143P
HUF76143S3	TO-262AA	76143S
HUF76143S3S	TO-263AB	76143S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76143S3ST.

Features

- Logic Level Gate Drive
- 75A, 30V
- *Ultra Low On-Resistance*, $r_{DS(ON)} = 0.0055\Omega$
- *Temperature Compensating* PSpice Model
- *Temperature Compensating* SABER Model
- *Thermal Impedance* SPICE Model
- *Thermal Impedance* SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

Packaging
JEDEC TO-220AB

JEDEC TO-262AA

JEDEC TO-263AB


HUF76143P3, HUF76143S3, HUF76143S3S

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30 V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	30 V
Gate to Source Voltage	V_{GS}	± 16 V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2)	I_D	75 A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 5\text{V}$)	I_D	75 A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 4.5\text{V}$) (Figure 2)	I_D	75 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17, 18
Power Dissipation	P_D	270 W
Derate Above 25°C		1.8 W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334.	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25V, V _{GS} = 0V	-	-	1	μA
		V _{DS} = 25V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figures 9, 10)	-	0.0052	0.0055	Ω
		I _D = 75A, V _{GS} = 5V (Figure 9)	-	0.0063	0.0075	Ω
		I _D = 75A, V _{GS} = 4.5V (Figure 9)	-	0.0068	0.0085	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	0.55	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220, TO-262 and TO-263	-	-	62	°C/W
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)						
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 75A, R _L = 0.2Ω, V _{GS} = 4.5V, R _{GS} = 2.5Ω (Figures 15, 21, 22)	-	-	250	ns
Turn-On Delay Time	t _{d(ON)}		-	22	-	ns
Rise Time	t _r		-	145	-	ns
Turn-Off Delay Time	t _{d(OFF)}		-	30	-	ns
Fall Time	t _f		-	18	-	ns
Turn-Off Time	t _{OFF}		-	-	72	ns

HUF76143P3, HUF76143S3, HUF76143S3S

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 75A, R _L = 0.2Ω, V _{GS} = 10V, R _{GS} = 2.5Ω (Figures 16, 21, 20)	-	-	105	ns	
Turn-On Delay Time	t _{d(ON)}		-	14	-	ns	
Rise Time	t _r		-	55	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	40	-	ns	
Fall Time	t _f		-	18	-	ns	
Turn-Off Time	t _{OFF}		-	-	87	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 15V, I _D ≅ 75A, R _L = 0.2Ω I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	95	114	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	50	60	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	3.8	4.6	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	3900	-	pF	
Output Capacitance	C _{OSS}		-	1600	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	270	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	90	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	170	nC

Typical Performance Curves

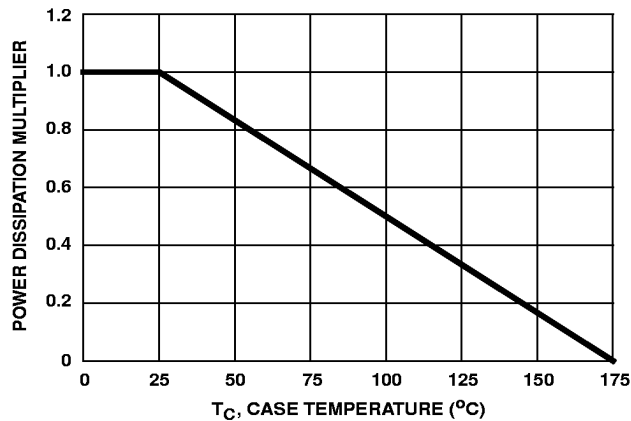


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

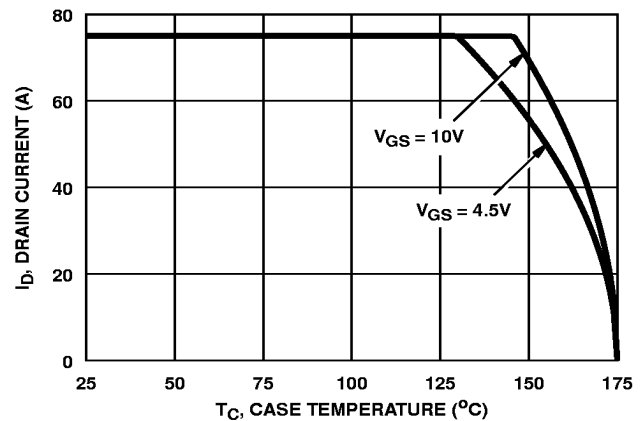


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves (Continued)

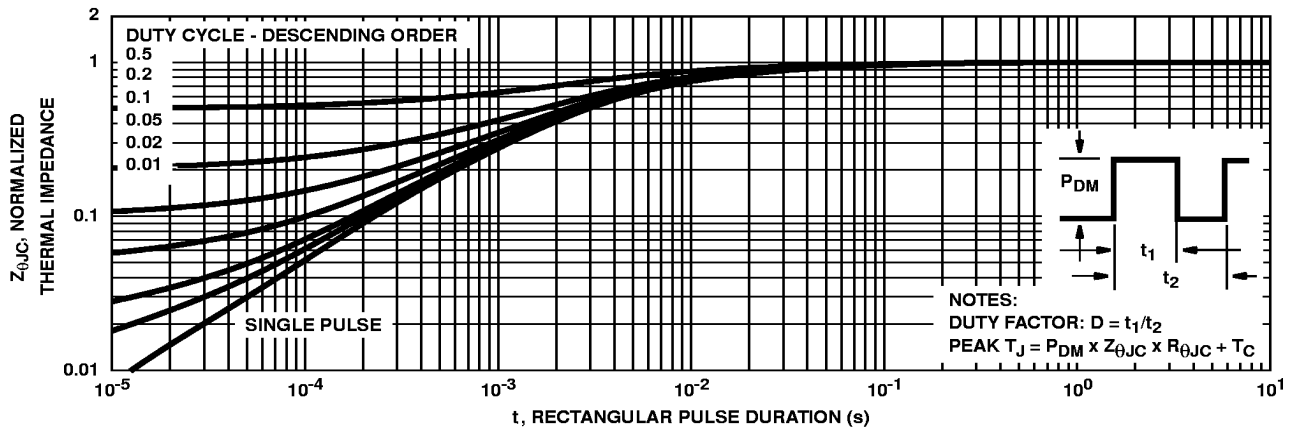


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

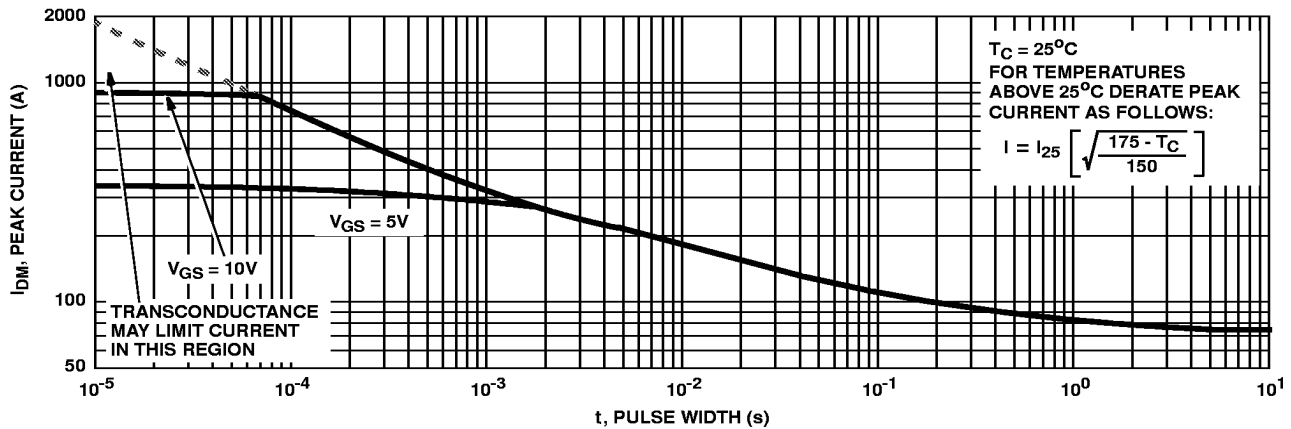


FIGURE 4. PEAK CURRENT CAPABILITY

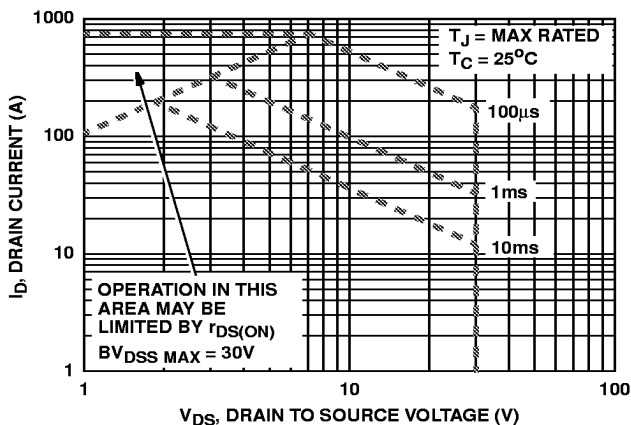
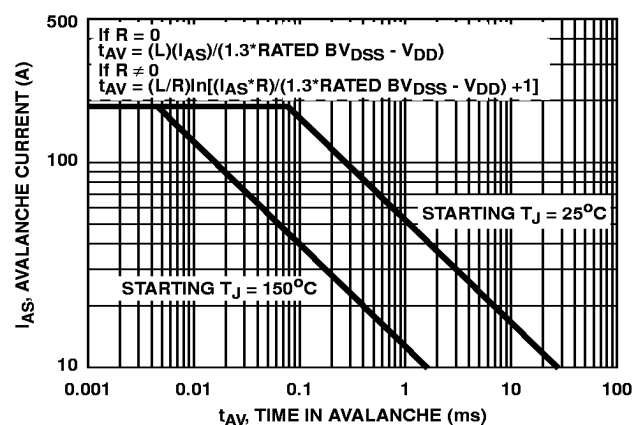


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

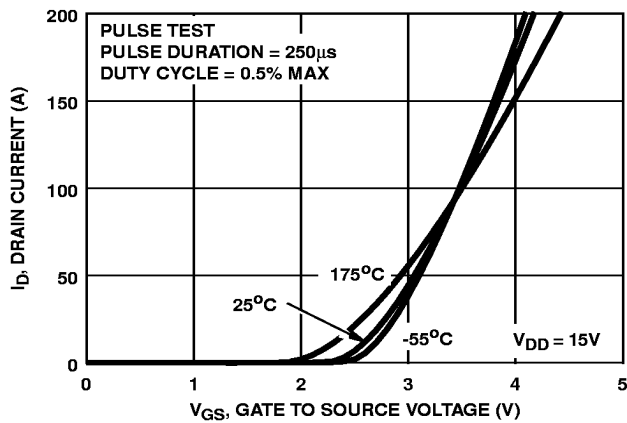


FIGURE 7. TRANSFER CHARACTERISTICS

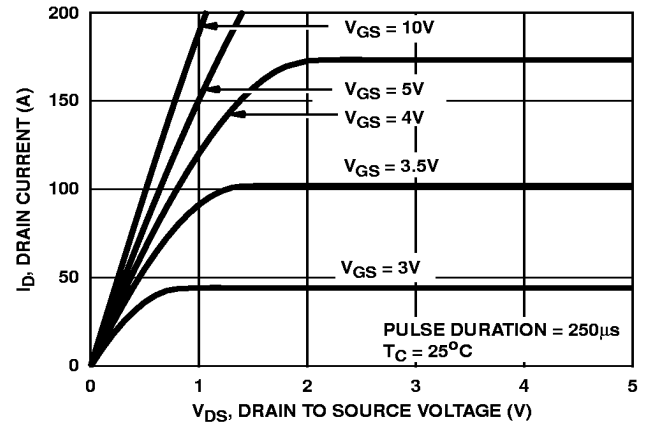


FIGURE 8. SATURATION CHARACTERISTICS

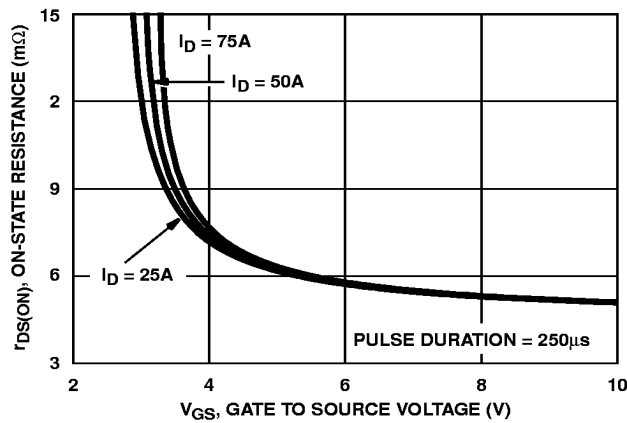


FIGURE 9. SOURCE TO DRAIN ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

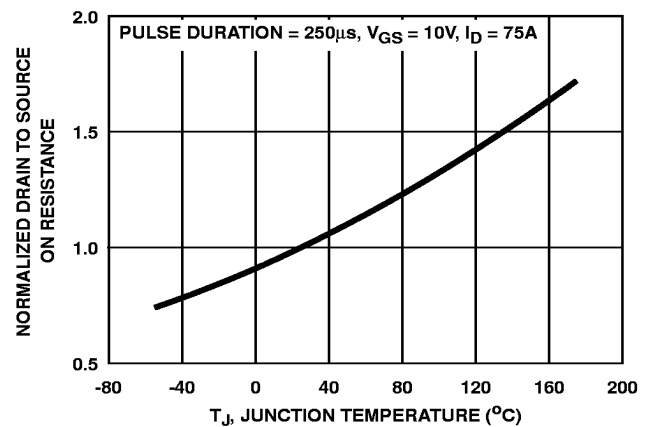


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

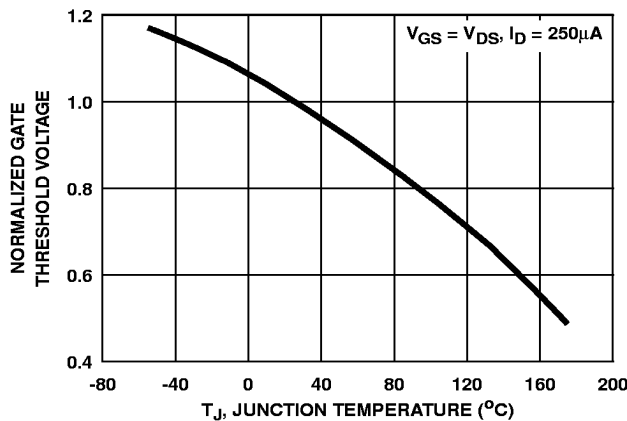


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

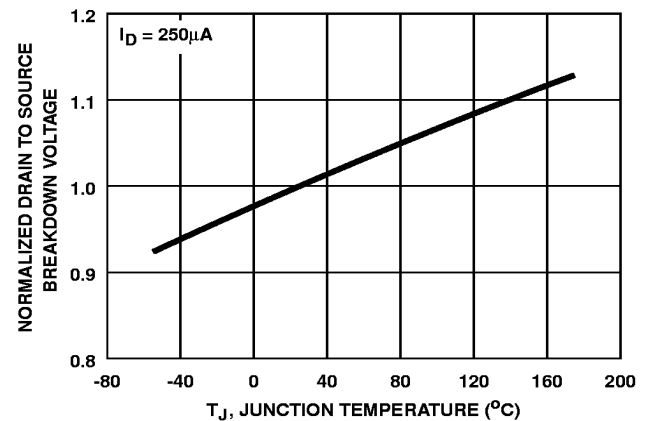


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

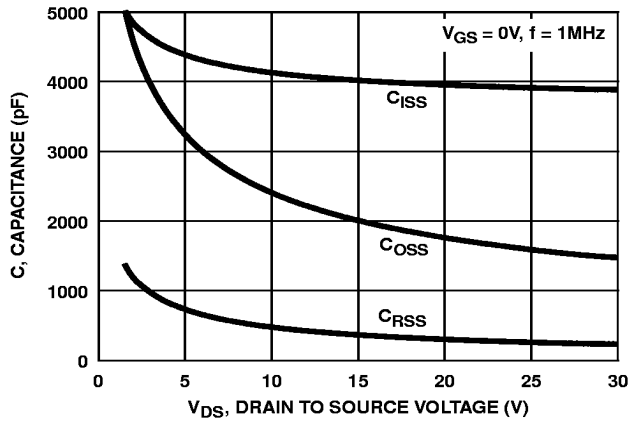
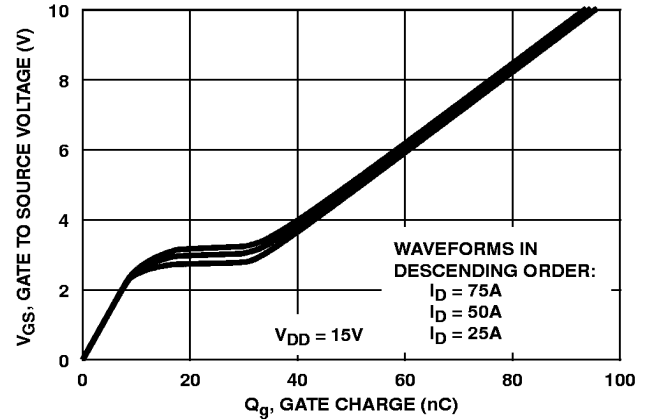


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes 7254 and 7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

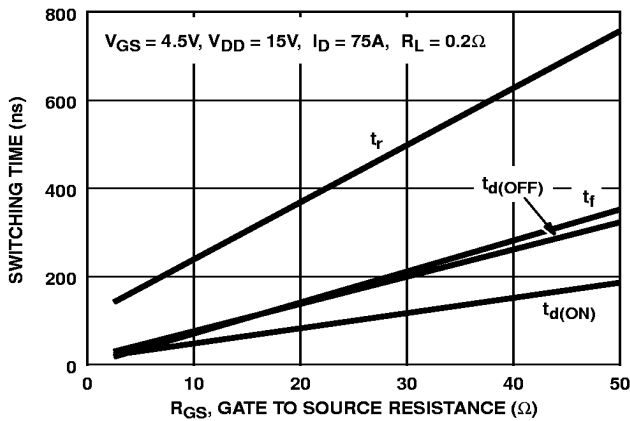


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

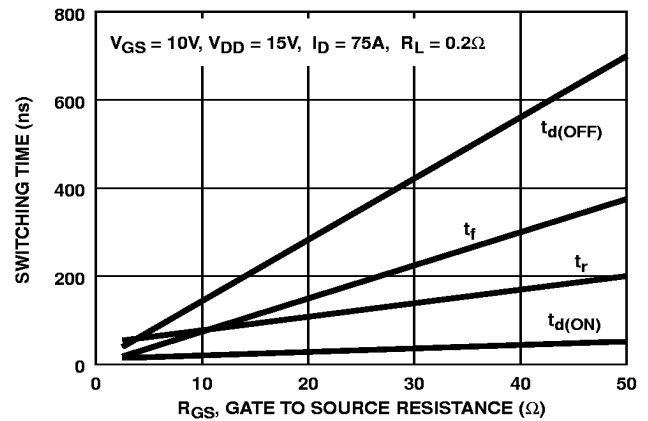


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

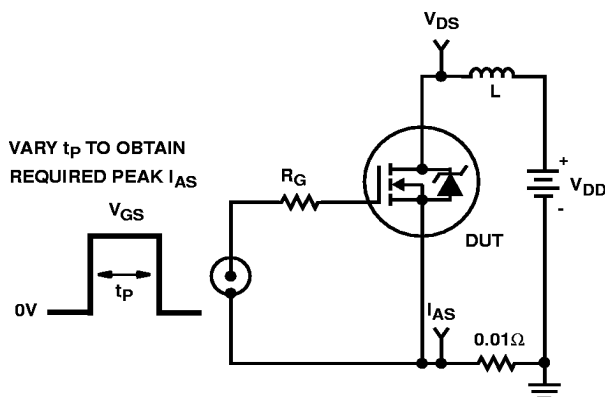


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

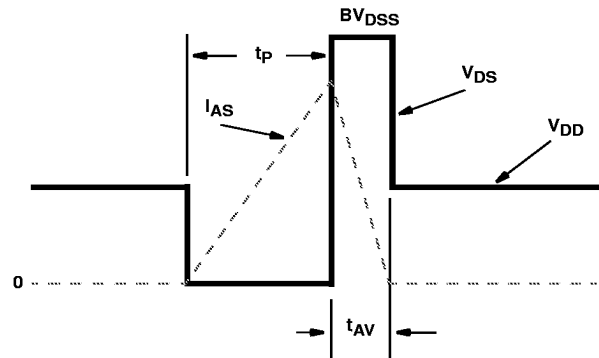


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

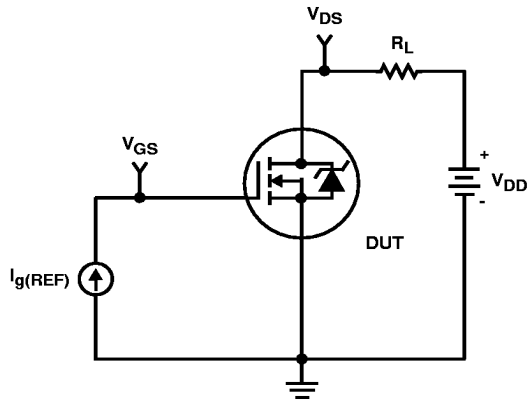


FIGURE 19. GATE CHARGE TEST CIRCUIT

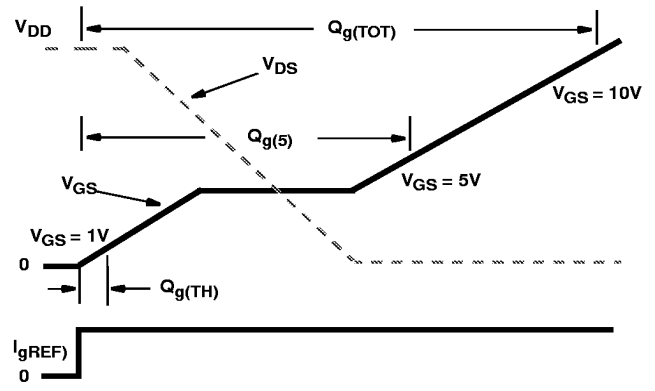


FIGURE 20. GATE CHARGE WAVEFORMS

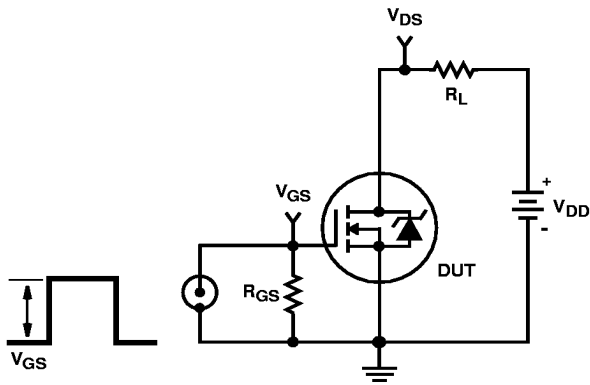


FIGURE 21. SWITCHING TIME TEST CIRCUIT

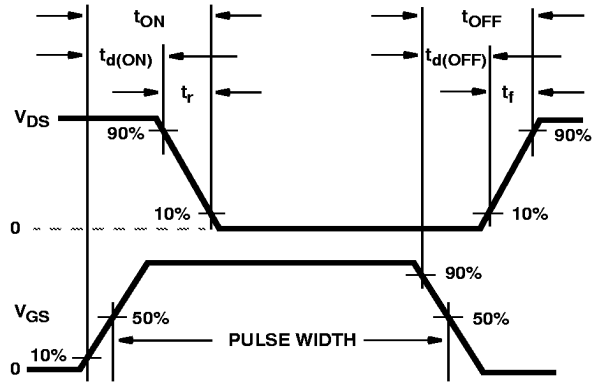


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

SUBCKT HUF76143 2 1 3 ; REV March 1998

CA 12 8 5.2e-9
CB 15 14 5e-9
CIN 6 8 3.65e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 39.38
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.6e-9
LSOURCE 3 7 1.1e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1.5e-3
RGATE 9 20 0.92
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

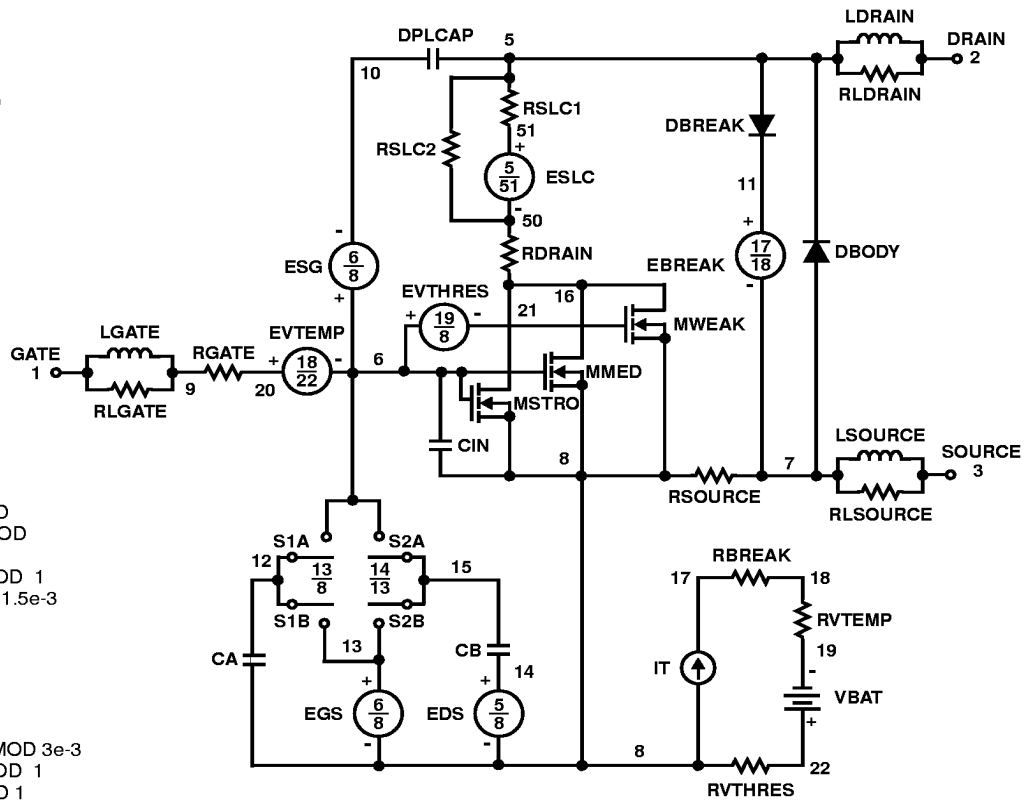
ESLC 51 50 VALUE={((V(5,51)/ABS(V(5,51)))^(PWR(V(5,51))/(1e-6*425),4))}

.MODEL DBODYMOD D (IS = 1.2e-11 RS = 2.65e-3 TRS1 = 2.3e-3 TRS2 = -4.2e-6 CJO = 5.45e-9 TT = 3.9e-8 XTI = 4.3 N = 1.03 M = 0.43)
.MODEL DBREAKMOD D (RS = 8.5e-2 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 2.6e-9 IS = 1e-30 N = 10 M = 0.7)
.MODEL MMEDMOD NMOS (VTO = 1.9 KP = 10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.92)
.MODEL MSTROMOD NMOS (VTO = 2.26KP = 215 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.62 KP = 0.1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 9.2 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.8e-4 TC2 = -4e-7)
.MODEL RDRAINMOD RES (TC1 = 1e-2 TC2 = 0)
.MODEL RSLCMOD RES (TC1 = 3e-3 TC2 = -2e-5)
.MODEL RSOURCEMOD RES (TC1 = 5e-4 TC2 = 1.1e-5)
.MODEL RVTHRESMOD RES (TC = -2.2e-3 TC2 = -6e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.45e-3 TC2 = -2e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5 VOFF = -2)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2 VOFF = -5)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = 1)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1 VOFF = -1.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV March 1998

HUF76143

CTHERM1 th 6 5.0e-3
 CTHERM2 6 5 1.2e-2
 CTHERM3 5 4 2.0e-2
 CTHERM4 4 3 2.8e-2
 CTHERM5 3 2 2e-1
 CTHERM6 2 tl 3

R THERM1 th 6 2.0e-3
 R THERM2 6 5 2.0e-2
 R THERM3 5 4 6.9e-2
 R THERM4 4 3 1.3e-1
 R THERM5 3 2 7.5e-2
 R THERM6 2 tl 3.0e-2

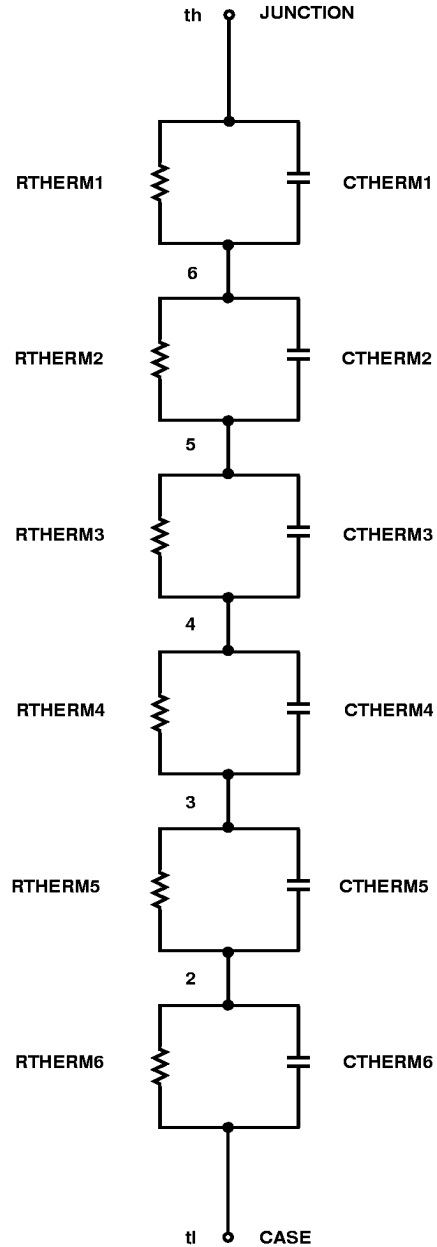
SABER Thermal Model

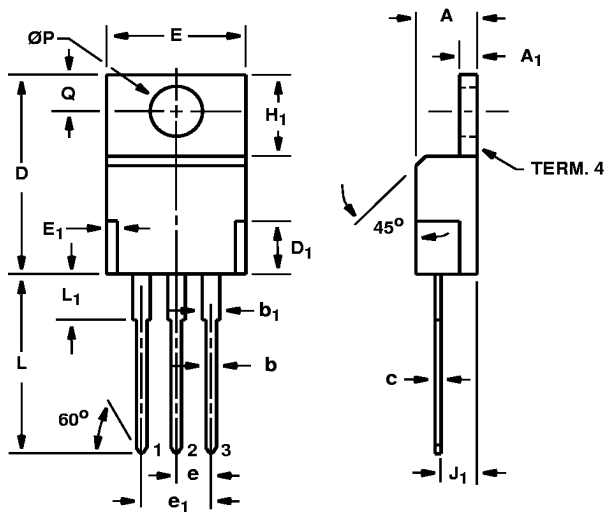
Saber thermal model HUF76143

template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.ctherm1 th 6 = 5.0e-3
    ctherm.ctherm2 6 5 = 1.2e-2
    ctherm.ctherm3 5 4 = 2.0e-2
    ctherm.ctherm4 4 3 = 2.8e-2
    ctherm.ctherm5 3 2 = 2.0e-1
    ctherm.ctherm6 2 tl = 3
}
```

```
rtherm.rtherm1 th 6 = 2.0e-3
rtherm.rtherm2 6 5 = 2.0e-2
rtherm.rtherm3 5 4 = 6.9e-2
rtherm.rtherm4 4 3 = 1.3e-1
rtherm.rtherm5 3 2 = 7.5e-2
rtherm.rtherm6 2 tl = 3.0e-2
}
```



TO-220AB
3 LEAD JEDEC TO-220AB PLASTIC PACKAGE


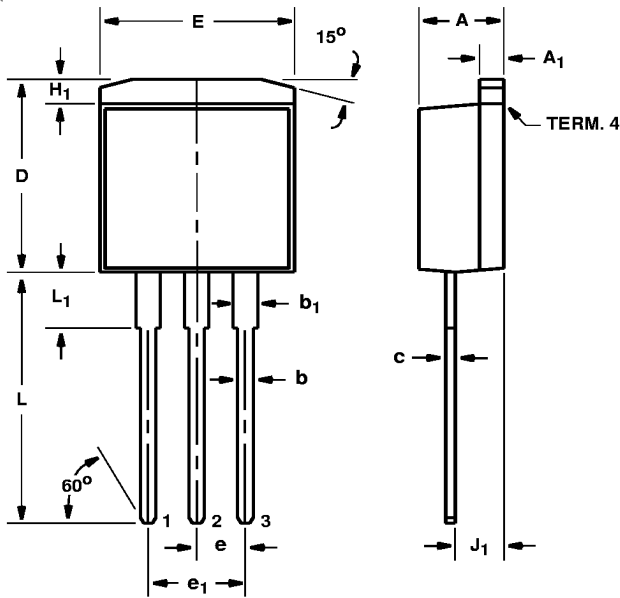
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
$\varnothing P$	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

TO-262AA

3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

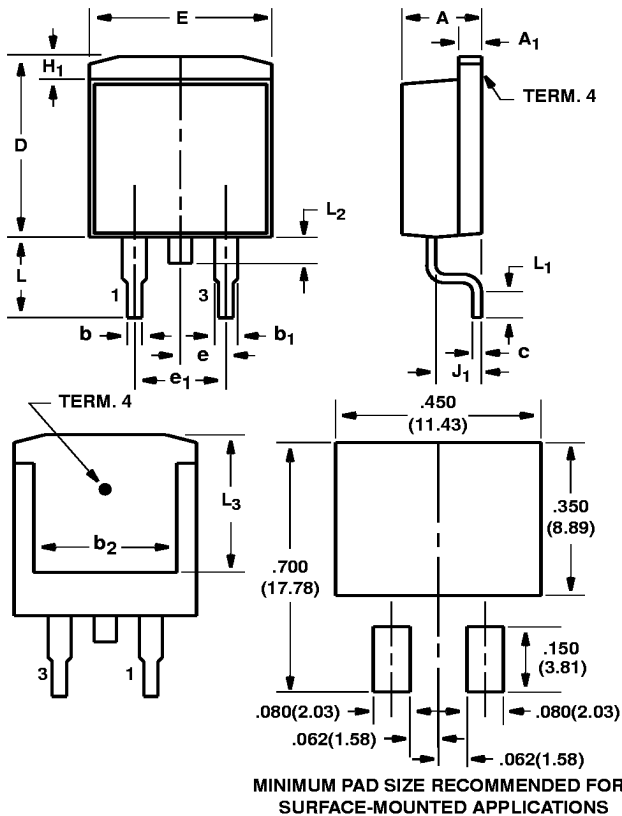


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	2

NOTES:

- These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
- Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



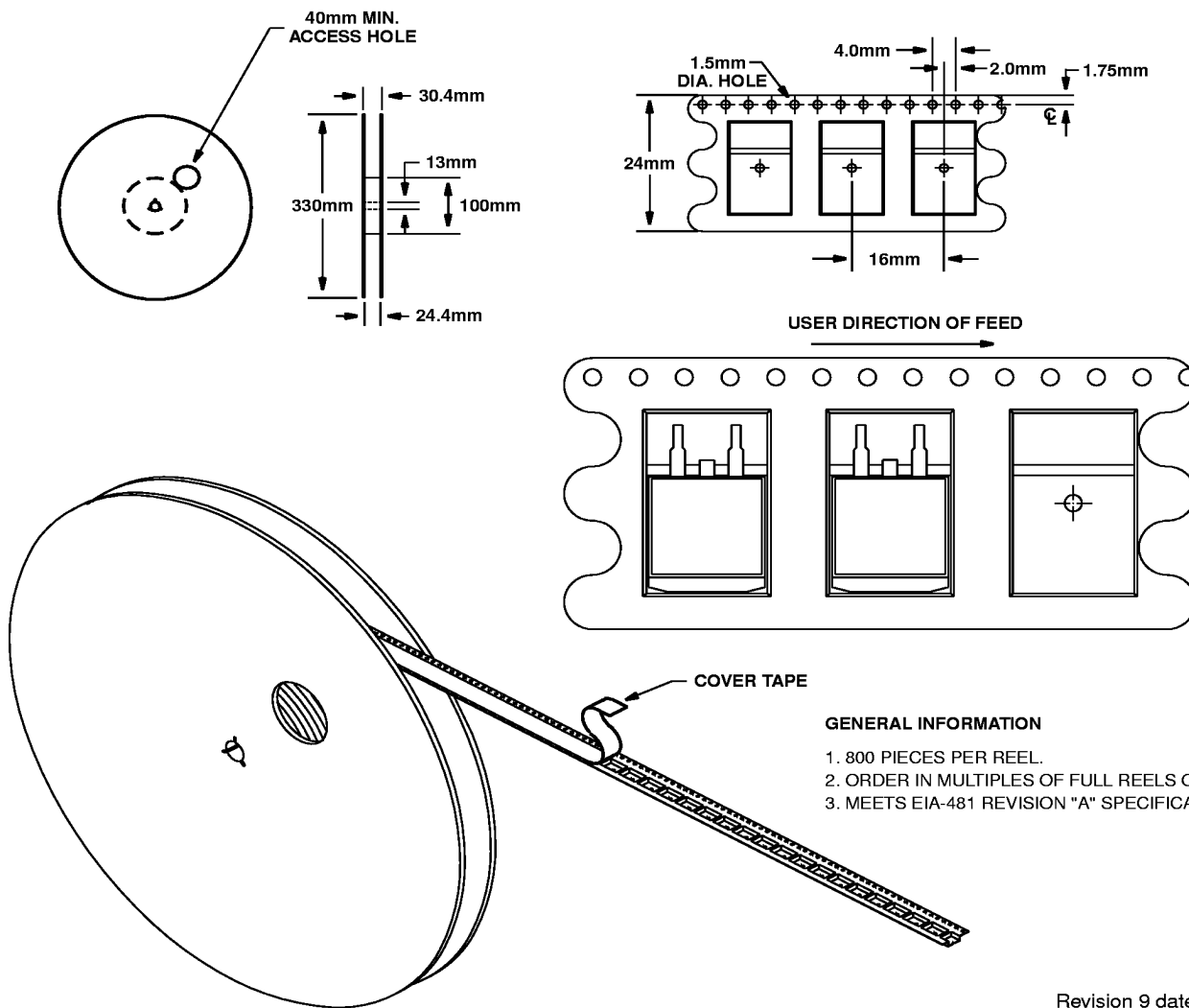
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

NOTES:

- These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
- L₃ and b₂ dimensions established a minimum mounting surface for terminal 4.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- L₁ is the terminal length for soldering.
- Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 9 dated 1-98.

TO-263AB

24mm TAPE AND REEL



Revision 9 dated 1-98