1 of 8 Decoded 8-Channel High Voltage Analog Switch

Ordering Information

V_{PP}	V_{NN}	V_{SIG}	Package Options	
			20-pin Plastic DIP	Die
+80V	-80V	130V P-P	HV1516P	HV1516X

Features

- HVCMOS® Technology
- Up to 130V peak to peak switching capability
- Output on-resistance typically 40 ohms
- Low parasitic capacitances
- DC to 10MHz analog signal frequency
- -45dB typical output off isolation at 5MHz
- CMOS logic circuitry for low power and excellent noise immunity
- On-chip decode, latch and chip select logic circuitry

General Description

Not recommended for new designs. Please use HV202 or HV207 instead.

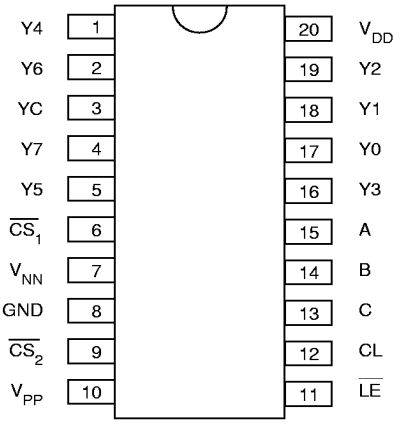
This device is an 8-channel high-voltage integrated circuit (HVIC), configured as a 1 of 8 decode function, intended for use in applications requiring high voltage switching controlled by low voltage signals; e.g., ultrasound imaging and printers. On-chip latches are provided for the decoded data. Using HVCMOS technology, this HVIC combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

Absolute Maximum Ratings*

V_{DD} logic power supply voltage	-0.5V to +18V
V_{PP} - V_{NN} supply voltage	174V
V_{PP} positive high voltage supply	-0.5V to +90V
V_{NN} negative high voltage supply	+0.5V to -90V
Logic input voltages	-0.5 to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	1.5A
Storage temperature	-65°C to +150°C
Power dissipation	1.2W

* Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

Pin Configuration



top view
20-pin DIP

Electrical Characteristics

(over operating conditions, V_{PP} = +80V, V_{NN} = -80V, and V_{DD} = 15V unless otherwise noted)

DC Characteristics

Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Switch (ON) Resistance	R_{ONS}		50		40	50		60	ohms	I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		35		25	35		45	ohms	I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		55		45	55		65	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch (ON) Resistance	R_{ONS}		40		25	40		50	ohms	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 200mA, V_{SIG} = 0V
Switch (ON) Resistance Matching x and y (0-3)	ΔR_{ONS}		30		10	30		30	%	V_{PP} = +50V, V_{NN} = -50V, I_{SW} = 5mA, V_{SIG} = 0V
Switch Off Leakage Per Switch	I_{SOL}		50		0.5	50		150	µA	V_{SIG} = V_{PP} -10V thru 10KΩ with 8 SWS in parallel
DC Offset Switch Off			500		100	500		500	mV	R_L = 100KΩ
DC Offset Switch On			500		100	500		500	mV	R_L = 100KΩ
Pole to Pole Switch Capacitance	C_{SW}		10		4.5	10		10	pF	DC Bias = 40V f = 1MHz
Logic Input Capacitance	C_{IN}				3.5				pF	
Pos. HV Supply Current	I_{PPQ}		200		50	200		200	µA	ALL SWS OFF
Neg. HV Supply Current	I_{NNQ}		-200		-50	-200		-200	µA	
Pos. HV Supply Current	I_{PPQ}				0.8	1.6			mA	1 SW ON, I_{SW} = 5mA,
Neg. HV Supply Current	I_{NNQ}				-0.8	-1.6			mA	V_{SIG} = 0V
Pos. HV Supply Current	I_{PPQ}				0.6	1.2			mA	V_{PP} = +50V, V_{NN} = -50V
Neg. HV Supply Current	I_{NNQ}				-0.6	-1.2			mA	1 SW ON, I_{SW} = 5mA
Switch Output Peak Current					1.5				A	V_{SIG} ≤ 0.1% Duty Cycle, f = 10KHz
Logic Supply Average Current	I_{DD}				4.0				mA	Input Freq. = 3MHz
Logic Supply Quiescent Current	I_{DDQ}				10	500			µA	

AC Characteristics

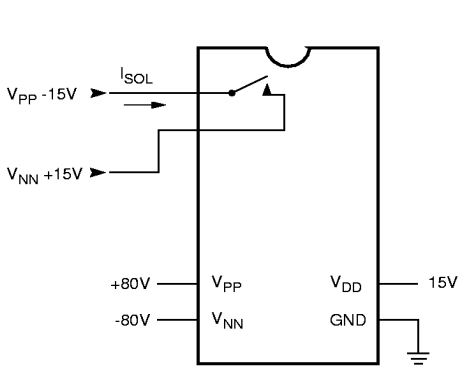
Characteristics	Sym	0°C		+25°C			+70°C		Units	Test Conditions
		min	max	min	typ	max	min	max		
Data Hold Time After $\overline{LE}$ Rises	t_{HD}			5.0					ns	
Set Up Time Before $\overline{LE}$ Rises	t_{SD}			260					ns	
Time Width of $\overline{LE}$	t_{WLE}			300					ns	
Time Width of CL	t_{WCL}			150					ns	
Turn On Time	t_{ON}		5.0		2.5	5.0		5.0	µs	R_L = 10KΩ
Turn Off Time	t_{OFF}		10		5.0	10		10	µs	R_L = 10KΩ
Off Isolation	KO			-35	-45				dB	Signal Freq. = 5MHz
Switch Crosstalk	K_{CR}				-45				dB	Signal Freq. = 5MHz

Operating Conditions

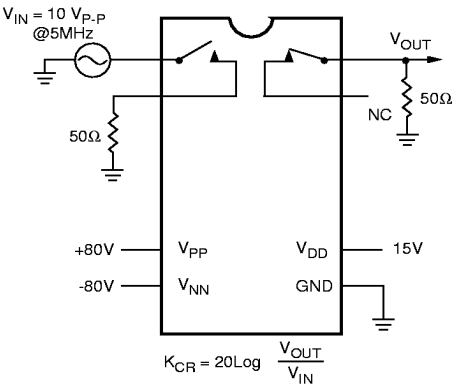
Symbol	Parameter	Value
V_{DD}	Logic power supply voltage[1]	+10.0V to +15.5V
V_{PP}	Positive high voltage supply[1]	+50V to +80V
V_{NN}	Negative high voltage supply[1]	-50V to -80V
V_{IH}	High level input voltage	V_{DD} -2V to V_{DD}
V_{IL}	Low-level input voltage	0 to 2.0V
V_{SIG}	Analog signal voltage peak to peak[2]	V_{NN} +15V to V_{PP} -15V
T_A	Operating free air-temperature	0° to 70°C

Note:
1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.

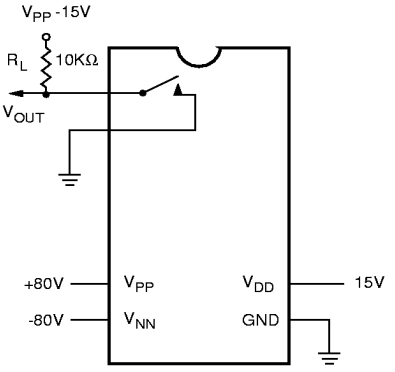
Test Circuits



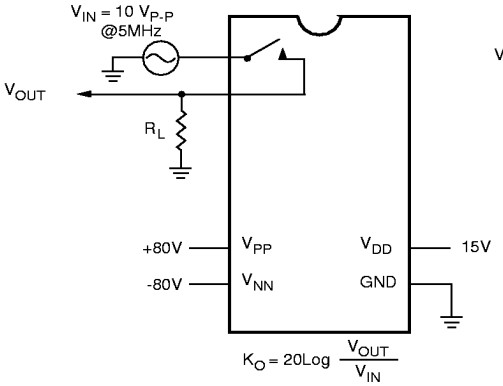
Switch OFF Leakage



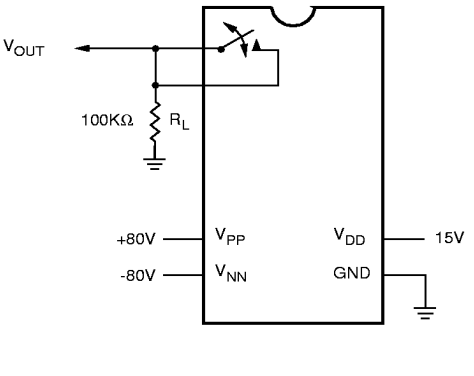
Crosstalk



T_{ON}/T_{OFF}

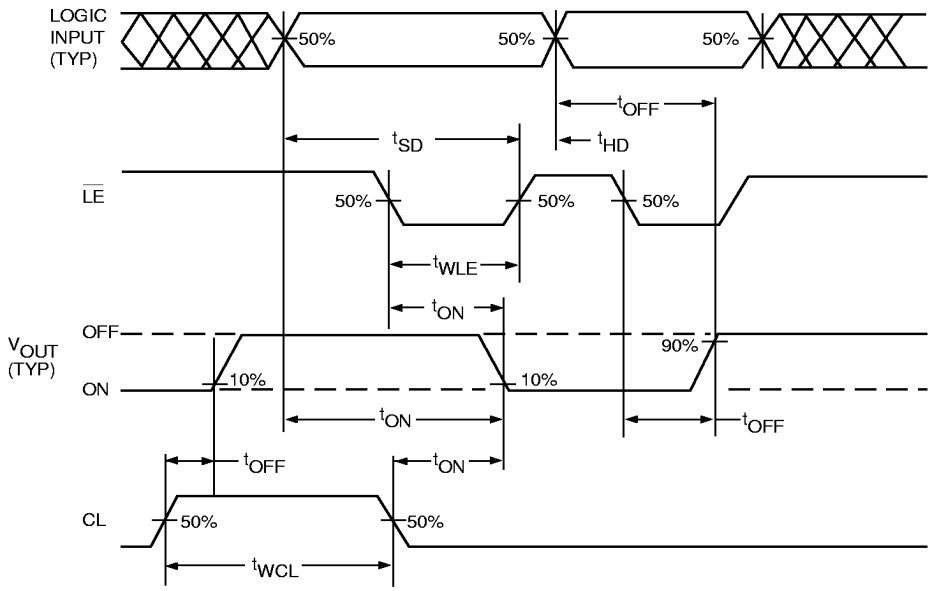


OFF Isolation

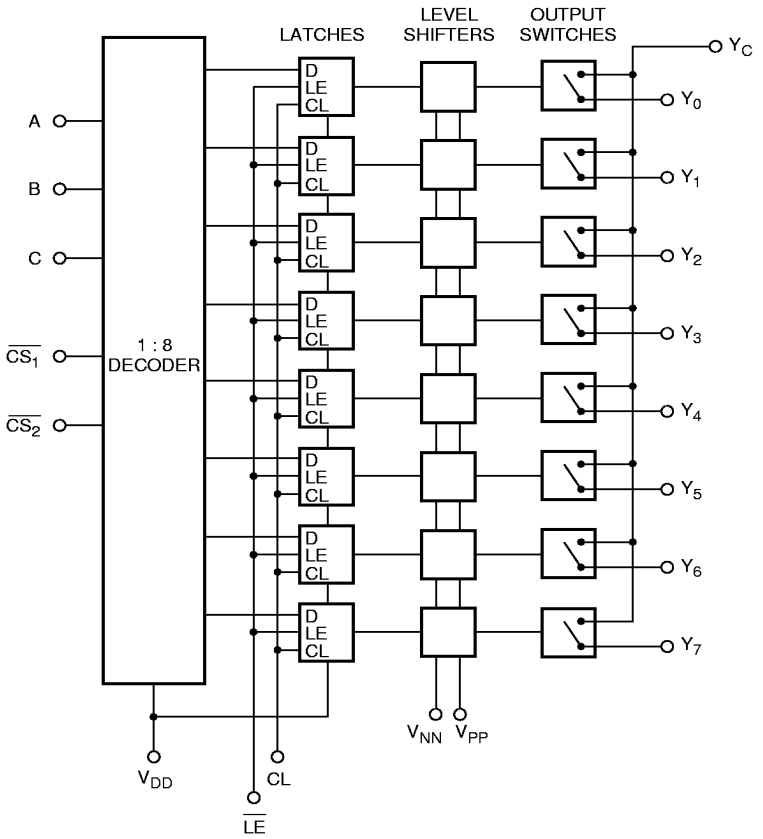


DC Offset ON/OFF

Logic Timing Waveforms



Logic Diagram



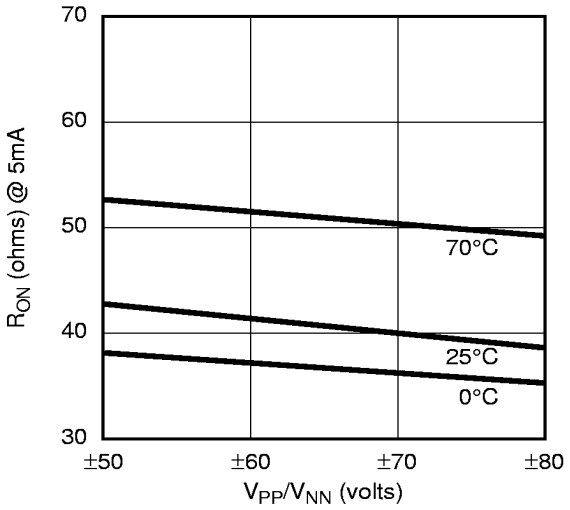
Truth Table

C	B	A	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{LE}$	CL	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	L	L	L	L	L	L	ON							
L	L	H	L	L	L	L		ON						
L	H	L	L	L	L	L			ON					
L	H	H	L	L	L	L				ON				
H	L	L	L	L	L	L					ON			
H	L	H	L	L	L	L						ON		
H	H	L	L	L	L	L							ON	
H	H	H	L	L	L	L								ON
X	X	X	H	X	L	L	ALL OUTPUTS OFF							
X	X	X	X	H	L	L	ALL OUTPUTS OFF							
X	X	X	X	X	X	H	ALL OUTPUTS OFF							
X	X	X	X	X	H	L	HOLDS PREVIOUS STATE							

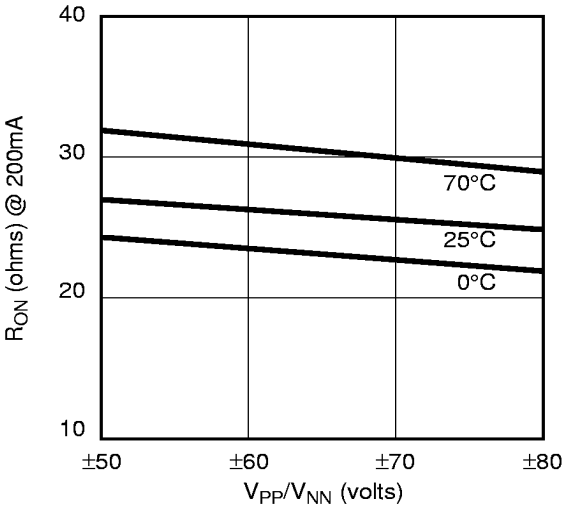
Notes:
1. Address data at A, B, C cause one of the eight switches to be selected for connection to the common bus Y_C.
2. The clear input CL overrides all other inputs.
3. Since the latch follows the decoder, only the CL input matters when $\overline{LE}$ is H.
4. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the decoded selection address information flows through the latch.

Typical Performance Curves

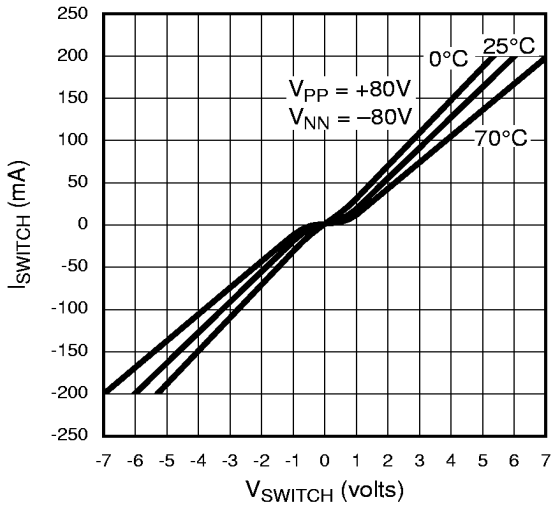
R_{ON} vs. V_{PP}/V_{NN}



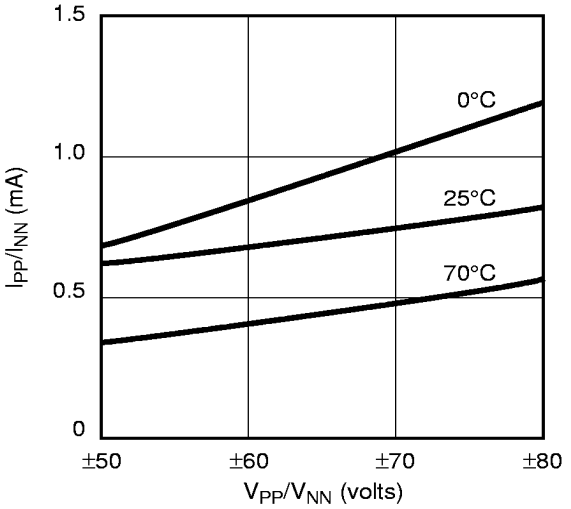
R_{ON} vs. V_{PP}/V_{NN}



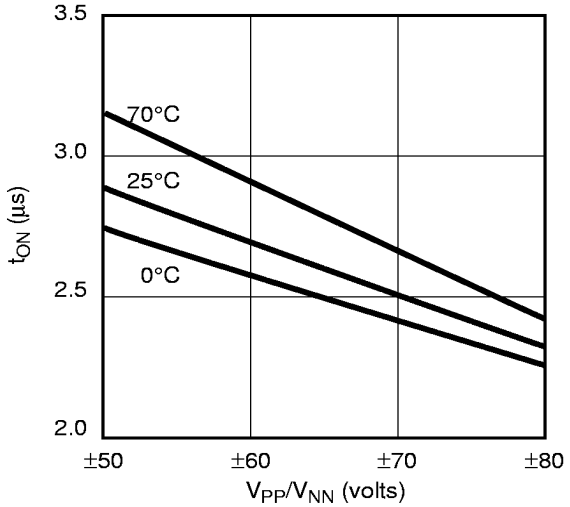
Switch Current vs. Switch Voltage



I_{PP}/I_{NN} vs. V_{PP}/V_{NN} (1 Switch ON)



t_{ON} vs. V_{PP}/V_{NN}



t_{OFF} vs. V_{PP}/V_{NN}