Supertex inc.

HV53
HV54

T-52-13-05

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} max	Package Options		
		44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV53	60V	HV5306DJ	HV5306PJ	HV5306X
	80V	HV5308DJ	HV5308PJ	HV5308X
HV54	60V	HV5406DJ	HV5406PJ	HV5406X
	80V	HV5408DJ	HV5408PJ	HV5408X

Features

- ☐ Processed with HVCMOS® technology
- ☐ Output voltages up to 80V using a ramped supply voltage
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options
- ☐ Diode to VPP allows efficient power recovery
- ☐ Replacements for SN75553 (HV5306), SN75554 (HV5406), SN75555 (HV5308) AND SN75556 (HV5408) Column Drivers
- ☐ 44-lead ceramic surface mount package
- ☐ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.5V to +18V
Supply voltage, V_{PP}	-0.5V to +250V
Logic input levels[1]	-0.5 to V_{DD} + 0.5V
Ground currrent[2]	1.5A
Continuous total power dissipation[3]	1500mW
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes: 1. All voltages are referenced to V_{SS}.
2. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV53 and HV54 are low voltage serial to high voltage parallel converters wtih push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. HVout1 is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the high to low transition of the clock. The HV54 shifts in the counterclockwise direction when viewed from the top of the package and the HV53 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the LE (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is retained when LE is low.

These devices are pin for pin replacements for the SN75553 and SN75554, SN75555 and SN75556. In addition, Supertex HVCMOS technology provides significantly iroved power consumption, speed, and source/sink current capability in the HV53 and HV54 devices.

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Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter			Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} supply current					15	mA	f_{CLK} = 8MHz V_{DD} = V_{DD} max
I_{PP}	High voltage supply current					0.5	mA	Outputs High
						0.5	mA	Outputs Low
I_{DDQ}	Quiescent V_{DD} supply current					0.5	mA	All V_{IN} = 0V
V_{OL}	Low-level output	HV_{OUT}	Commercial	52			V	I_O = -20mA
			Military	52			V	I_O = -15mA
			Data out	10.5			V	I_O = -100µA
V_{OH}	High-level output	HV_{OUT}	Commercial			8	V	I_O = 20mA
			Military			8	V	I_O = 15mA
			Data out			1	V	I_O =100µA
I_{IH}	High-level logic input current					1	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current					-1	µA	V_I = 0V

AC Characteristics (@ V_{DD} = 12V, V_{PP} = 60V, T_C = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{DHL}	Delay time, high to low data out from clock			110	ns	C_L = 10pF
t_{DLH}	Delay time, low to high data out from clock			110	ns	C_L = 10pF
t_{SU}	Data set-up time before clock rises	25			ns	C_L = 10pF
t_H	Data hold time after clock rises	10			ns	C_L = 10pF

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{DD}	Logic supply voltage		10.8	12	13.2	V
V_{PP}	High voltage supply	HV5306 and HV5406	-0.3		60	V
		HV5308 and HV5408	-0.3		80	V
V_{IH}	High-level input voltage		V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage		0		2.0	V
f_{CLK}	Clock frequency		0		8.0	MHz
T_A	Operating free-air temperature	Commercial	0		+70	°C
		Military Hi-Rel (RB)	-55		+125	°C

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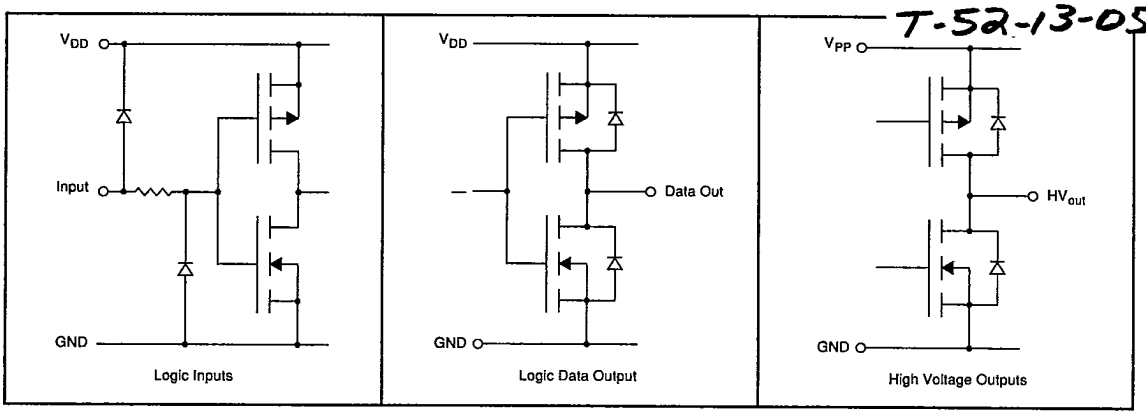
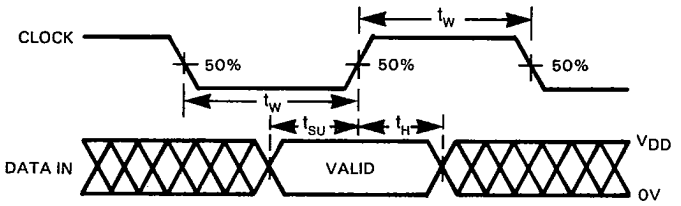
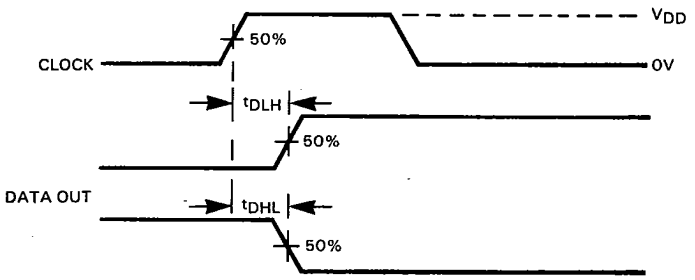
Input and Output Equivalent Circuits

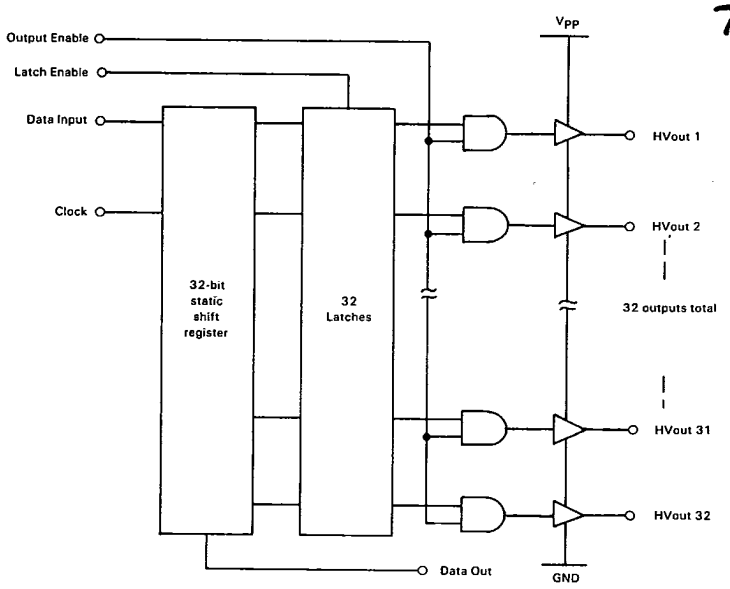


Switching Waveforms





Functional Block Diagram



Function Table

Function	Inputs				Outputs						
					Shift Reg		Latch		HV Outputs		Data Out
	DI	CLK	$\overline{LE}$	OE	1	2...32	1	2...32	1	2...32	
All off	X	X	X	L	*	*...*	*	*...*	L	L...L	2
Load S/R	H or L	↑	X	X	H or L	*...*	*	*...*	*	*...*	2
Load latches	X	H or L	↑	X	*	*...*	New Data		*	*...*	2
Latch mode	X	X	L	H	*	*...*	Stored Data		Stored Data[1]		2

X = Don't care.
* = Dependent on previous stage's state before the last CLK : or last LE high and status of OE.
↑ = low-to-high transition.
H = High level.
L = Low level.
1 = When output enable is high.
2 = Data out takes the same state as the 32nd shift register stage.

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Pin Configurations

HV53
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HVout 17	23	GND
2	HVout 16	24	V_{PP}
3	HVout 15	25	V_{DD}
4	HVout 14	26	Latch Enable
5	HVout 13	27	Data In
6	HVout 12	28	Output Enable
7	HVout 11	29	N/C
8	HVout 10	30	HVout 32
9	HVout 9	31	HVout 31
10	HVout 8	32	HVout 30
11	HVout 7	33	HVout 29
12	HVout 6	34	HVout 28
13	HVout 5	35	HVout 27
14	HVout 4	36	HVout 26
15	HVout 3	37	HVout 25
16	HVout 2	38	HVout 24
17	HVout 1	39	HVout 23
18	Data Out	40	HVout 22
19	N/C	41	HVout 21
20	N/C	42	HVout 20
21	N/C	43	HVout 19
22	Clock	44	HVout 18

HV54
44 Pin J-Lead Package

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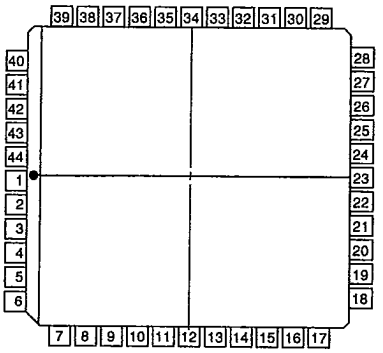
1	HVout 16	23	GND
2	HVout 17	24	V_{PP}
3	HVout 18	25	V_{DD}
4	HVout 19	26	Latch Enable
5	HVout 20	27	Data In
6	HVout 21	28	Output Enable
7	HVout 22	29	N/C
8	HVout 23	30	HVout 1
9	HVout 24	31	HVout 2
10	HVout 25	32	HVout 3
11	HVout 26	33	HVout 4
12	HVout 27	34	HVout 5
13	HVout 28	35	HVout 6
14	HVout 29	36	HVout 7
15	HVout 30	37	HVout 8
16	HVout 31	38	HVout 9
17	HVout 32	39	HVout 10
18	Data Out	40	HVout 11
19	N/C	41	HVout 12
20	N/C	42	HVout 13
21	N/C	43	HVout 14
22	Clock	44	HVout 15

Package Outline



top view

44-pin J-lead Package