Supertex inc

HV61

Preliminary

64-Channel Military TFT ±10V Liquid Crystal Display Driver

T-52-13-07

Ordering Information

Device	Package Options		
	80-Lead Quad Ceramic Gullwing	80-Lead Quad Ceramic Gullwing (MIL-STD-883 Processed*)	Die
HV61	HV6101DG	RBHV6101DG	HV6101X

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Symmetrical + 10V output swing
- Active return to ground
- +12V control logic
- Bidirectional shift control pin
- Data out for cascading
- 8MHz clock

Absolute Maximum Ratings

Supply Voltage, V_{DD}	-0.5 to +15.0V_{DC}
Supply Voltage, V_{SS}	-0.5 to +15.0V_{DC}
Logic Input Levels	(-0.5) to (V_{DD} + 0.5)V_{DC}
Continuous Total Power Disipatation	1500mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Die Storage Temperature Range	-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.

General Description

The HV61 is a 64-channel latched serial-to-parallel converter with bidirectional shifting capability and high-voltage outputs that can be switched in polarity from V_{PP} to V_{NN}. It is intended mainly as a driver for active-matrix liquid crystal displays in military systems.

The shift direction is controlled by pins SHFL and CSB. A low at CSB enables the shift function, which occurs at the low-to-high transition of the clock. A high at SHFL causes data to be shifted "right-to left" (from L_{IN} R_{OUT} toward L_{OUT} R_{IN}), and vice versa.

The 64 latches are transparent when LOAD is high, and the data is latched when load is low.

The FRAME control reverses the voltage polarity of outputs that are in the logical high state. For FRAME = high, high-level outputs will be at V_{DD} level: for FRAME = low, high-level outputs will be at V_{SS} level. Outputs at logic low will be low regardless of FRAME.

Electrical Characteristics

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DC Characteristics

Notes 1 & 2

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Current	0		500	mA	V_{DD} = 12V[3]
I_{SS}	V_{SS} Current	—		-500	mA	V_{SS}= -12V[3]
I_{IH}	Input High Leakage Current	0		10	mA	VIH = 12V
I_{IL}	Input Low Leakage Current	-10		0	mA	VIL = 0V
I_{OMP}	Output Source Current	-1.0		—	mA	V_{OH} = 11.5V
I_{OHN}	Output Source Current	1.0		—	mA	V_{OH} = 11.5V
I_{OL}	Output Sink Current	1.0		—	mA	V_{OH} = 0.5V

Notes:
1. V_{DD} =12V. V_{SS}=-12V
2. Negative current indicates current flow out of the device
3. No load

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply Voltage	9	10	13.2	V	
V_{SS}	Supply Voltage	9	10	13.2	V	
V_{IH}	High-level input voltage	V_{DD}-2		V_{DD}	V	
V_{IL}	Low-level input voltage	0		2	V	

Note:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

Truth Tables

Input

CSB	SHFL	Shift Register
H	X	No Shift
L	H	Shift Left (L_{IN} R_{OUT} to L_{OUT} R_{IN})
L	L	Shift Right (L_{OUT} RI_N to L_{IN} R_{OUT})

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Output

Load	FRAME	Outputs
L	X	L (Previous Data)
H	H	V_{DD} (New Data: Latch Transparent)

Functional Block Diagram

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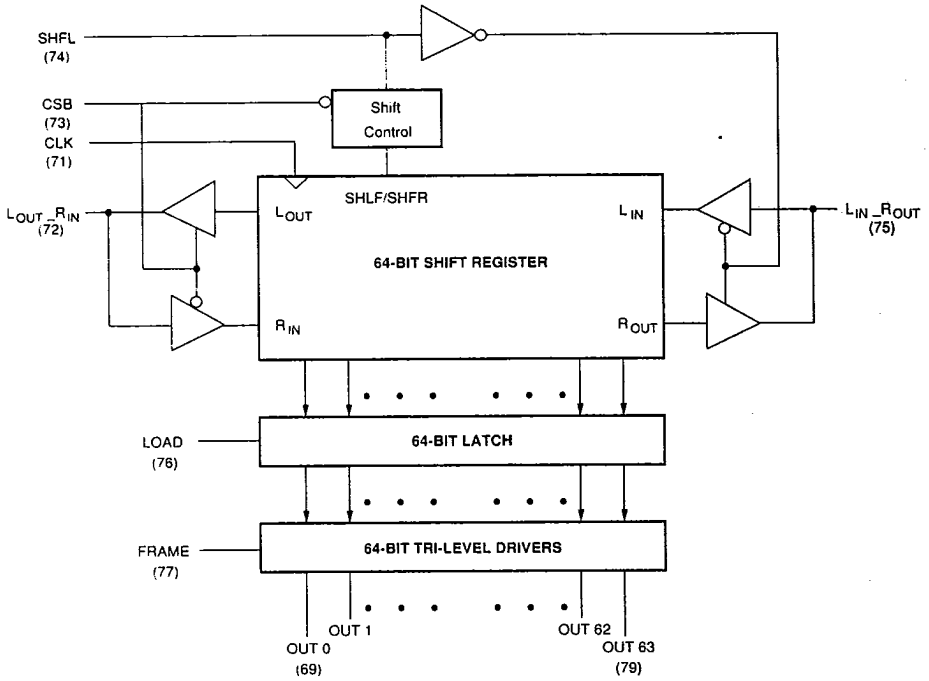
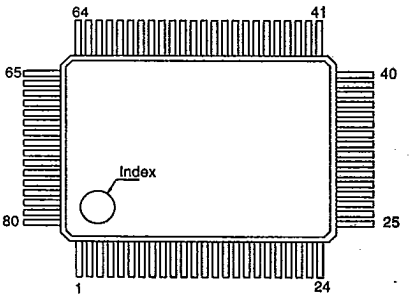


Pin Configuration

80-Gullwing Package

Pin	Function	Pin	Function
1	GND	41	Q25
2	Q61	42	Q24
3	Q60	43	V_{SS}
4	Q59	44	Q23
5	Q58	45	Q22
6	Q57	46	Q21
7	Q56	47	Q20
8	Q55	48	Q19
9	Q54	49	Q18
10	Q53	50	Q17
11	V_{SS}	51	Q16
12	Q52	52	V_{DD}
13	Q51	53	Q15
14	Q50	54	Q14
15	Q49	55	Q13
16	Q48	56	Q12
17	Q47	57	Q11
18	Q46	58	Q10
19	Q45	59	Q09
20	Q44	60	Q08
21	V_{DD}	61	Q07
22	Q43	62	Q06
23	Q42	63	Q05
24	Q41	64	V_{SS}
25	Q40	65	Q04
26	Q39	66	Q03
27	Q38	67	Q02
28	Q37	68	Q01
29	Q36	69	Q00
30	Q35	70	GND
31	Q34	71	CLK
32	GND	72	L_{OUT} R_{IN}
33	Q33	73	CSB
34	Q32	74	SHFL
35	Q31	75	L_{IN} R_{OUT}
36	Q30	76	Load
37	Q29	77	Frame
38	Q28	78	V_{DD}
39	Q27	79	Q63
40	Q26	80	Q62

Package Outline



top view

80-pin Gullwing Package

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