



HV67

32-Channel LCD Driver with Separate Backplane Output

Product Objective Specification

T-52-13-07

Ordering Information

Device	Package Options	
	44 J-Lead Quad Plastic Chip Carrier	Dice in waffle pack
HV67	HV6706PJ	HV6706X

Features

- ☐ Processed with HVCMOS[®] technology
- ☐ Output voltages up to 60V
- ☐ Low power level shifting
- ☐ Source/sink current minimum 5mA
- ☐ Shift register speed 5MHz
- ☐ Latched data outputs
- ☐ Bidirectional shift register (R/L Shift)
- ☐ Backplane Output

Absolute Maximum Ratings¹

Supply voltage, V_{DD} ²	-0.5V to +7.0V
Output voltage, V_{PP}	V_{DD} to +80V
Logic input levels ²	-0.5V to V_{DD} +0.5V
Ground current ³	1.5A
Continuous total power dissipation ⁴	1500mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +125°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to V_{SS} .
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV67 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for LCD displays. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities. The inputs are fully CMOS compatible.

The device consists of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking (optional) of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. A R/L Shift pin causes data shifting counterclockwise when grounded and clockwise when connected to V_{DD} . A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout32). Operation of the shift register is not affected by the LE (latch enable), BL (blanking), or the POL (polarity) inputs. Transfer of data from the shift register to the latch occurs when the LE (latch enable) input is high. The data in the latch is stored during LE transition from high to low.

Electrical Characteristics (over recommended operating conditions unless noted)**DC Characteristics** ($V_{DD} = 5V$, $V_{PP} = 60V$, $V_{SS} = GND$)**T-52-13-07**

Symbol	Parameter	Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		15	mA	$V_{DD} = V_{DD} \text{ max}$ $f_{CLK} = 5\text{MHz}$
I_{PP}	High voltage supply current		0.5	mA	Outputs high
			0.5	mA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current		0.5	mA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	Q	52	V	$I_O = 5\text{mA}$, $V_{PP} = 60V$
		Data out	4.6	V	$I_O = -500\mu A$
V_{OL}	Low-level output	Q	8	V	$I_O = 5\text{mA}$, $V_{PP} = 60V$
		Data out	0.4	V	$I_O = 500\mu A$
I_{IH}	High-level logic input current		1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-1	μA	$V_{IL} = 0V$
V_{OLBP}	Low-level output voltage, backplane		8	V	$I_O = 40\text{mA}$
V_{OHBP}	High-level output voltage, backplane	52		V	$I_O = -40\text{mA}$

AC Characteristics ($V_{DD} = 5V$, $V_{PP} = 60V$, $T_C = 25^\circ C$)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		5	MHz	
t_W	Clock width high or low	100		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	50		ns	
t_{ON}, t_{OFF}	Time from latch enable or POL to HV_{OUT}		500	ns	$C_L = 30\text{pF}$
t_{ON}, t_{OFF}	Time from POL to BP output		500	ns	$C_L = 30\text{pF}$
t_{DHL}	Delay time clock to data high to low		75	ns	$C_L = 15\text{pF}$
t_{DLH}	Delay time clock to data low to high		75	ns	$C_L = 15\text{pF}$
t_{OLE}	Delay time clock to LE low to high	50		ns	
t_{WLE}	Width of LE pulse	100		ns	
t_{SLE}	LE set-up time before clock rises	50		ns	

11

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output off voltage	35	60	V
V_{IH}	High-level input voltage	3.5	V_{DD}	V
V_{IL}	Low-level input voltage	0	0.8	V
f_{CLK}	Clock frequency		5	MHz
T_A	Operating free-air temperature	-40	+85	$^\circ C$
I_{OD}	Allowable current through output diodes		200	mA

Note:

Power-up sequence should be the following:

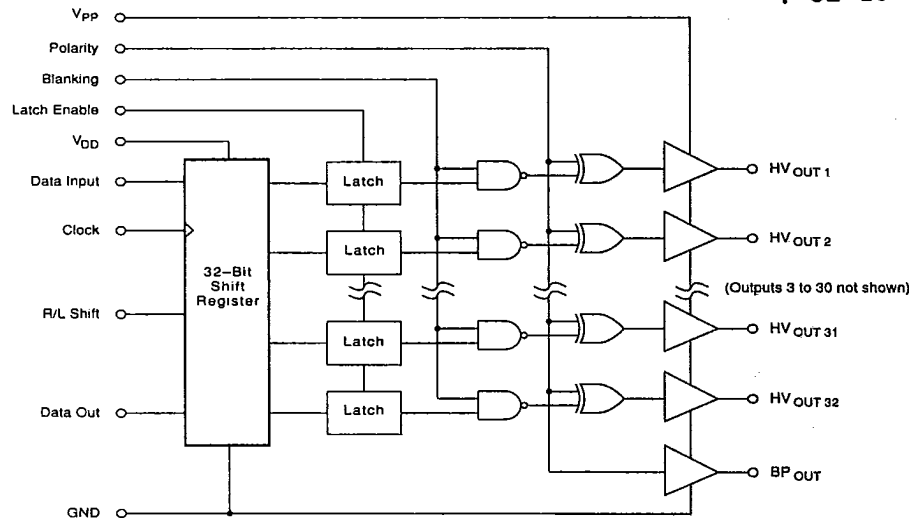
1. Connect ground.
2. Apply V_{DD} .
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP} .

Power-down sequence should be the reverse of the above.

5. The V_{PP} should not drop below V_{DD} during operation.

Functional Block Diagram

T-52-13-07



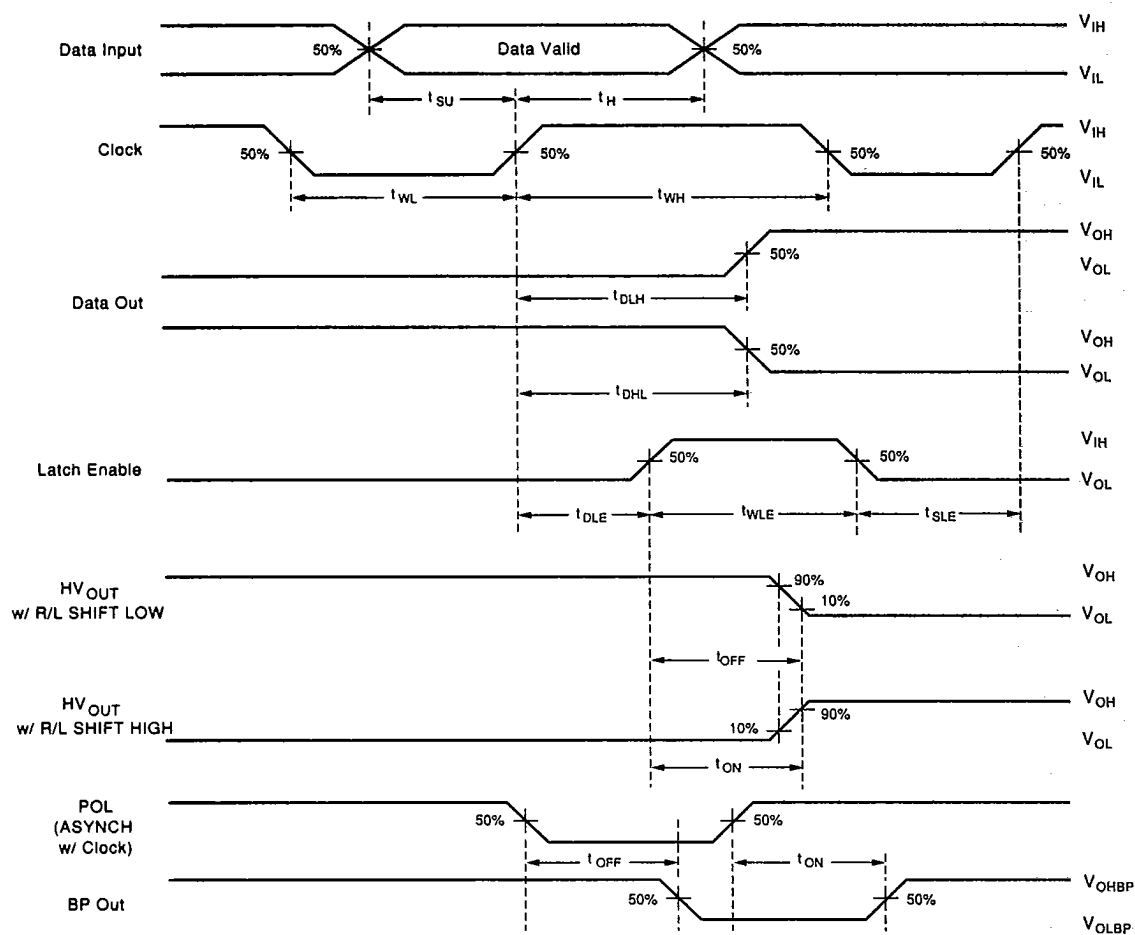
Function Table

Function	Inputs					Outputs			
	Data	CLK	LE	BL	POL	Shift Reg 1 2...32	HV Outputs 1 2...32		Data Out *
All on	X	X	X	L	L	* *...*	H	H...H	*
All off	X	X	X	L	H	* *...*	L	L...L	*
Invert mode	X	X	L	H	L	* *...*	$\overline{*}$	$\overline{*}$...	*
Load S/R	H or L	↑	L	H	H	H or L *...*	*	*...*	*
Load latches	X	H or L	↑	H	H	* *...*	*	*...*	*
	X	H or L	↑	H	L	* *...*	$\overline{*}$	$\overline{*}$...	*
Transparent latch mode	L	↑	H	H	H	L *...*	L	*...*	*
	H	↑	H	H	H	H *...*	H	*...*	*

Notes:
H = high level, L = low level, X = irrelevant, * = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last LE high.

Switching Waveforms

T-52-13-07



Pin Configuration

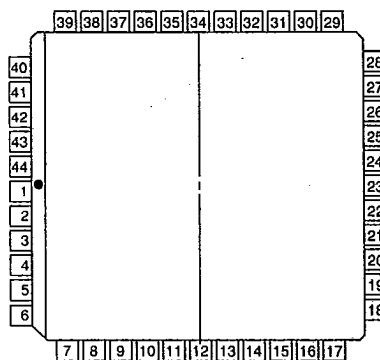
Package Outline

T-52-13-07

HV67

44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV _{OUT} 17/16	23	LE
2	HV _{OUT} 16/17	24	V _{DD}
3	HV _{OUT} 15/18	25	Clock
4	HV _{OUT} 14/19	26	R/L Shift
5	HV _{OUT} 13/20	27	Data In
6	HV _{OUT} 12/21	28	V _{PP}
7	HV _{OUT} 11/22	29	BP Out
8	HV _{OUT} 10/23	30	HV _{OUT} 32/1
9	HV _{OUT} 9/24	31	HV _{OUT} 31/2
10	HV _{OUT} 8/25	32	HV _{OUT} 30/3
11	HV _{OUT} 7/26	33	HV _{OUT} 29/4
12	HV _{OUT} 6/27	34	HV _{OUT} 28/5
13	HV _{OUT} 5/28	35	HV _{OUT} 27/6
14	HV _{OUT} 4/29	36	HV _{OUT} 26/7
15	HV _{OUT} 3/30	37	HV _{OUT} 25/8
16	HV _{OUT} 2/31	38	HV _{OUT} 24/9
17	HV _{OUT} 1/32	39	HV _{OUT} 23/10
18	Data Out	40	HV _{OUT} 22/11
19	GND	41	HV _{OUT} 21/12
20	BL	42	HV _{OUT} 20/13
21	N/C	43	HV _{OUT} 19/14
22	POL	44	HV _{OUT} 18/15



top view

44-pin J-lead Package

Note:

- Pin designation for R/L Shift = L/H
Example: for R/L Shift = L Pin 1 is HV_{OUT} 17
for R/L Shift = H Pin 1 is HV_{OUT} 16
- Blanking function is optional. BL pin can be left open when not used.