Supertex inc.

Advanced Information

High-Voltage Current-Mode PWM Controller

Ordering Information

$+V_{IN}$		Feedback Accuracy	Max Duty Cycle	Package Options			
Min	Max			14 Pin Plastic DIP	14 Pin Ceramic DIP	14 Pin Narrow Body SOIC	DICE
15V	200V	±1.5%	49%	HV9114P	HV9114C	HV9114NG	HV9114X

Standard temperature range for all parts is industrial (-40° to +85°C). For military temperature range parts (-55° to +125°C) contact factory.

Features

- ☐ Latched $\overline{\text{SHUTDOWN}}$
- ☐ 15 to 200V input range
- ☐ Current-mode control
- ☐ High efficiency
- ☐ Up to 2MHz internal oscillator
- ☐ Internal start-up circuit
- ☐ Low internal noise
- ☐ Soft start
- ☐ 1.5MHz error amp

Applications

- ☐ DC/DC converters
- ☐ Distributed power systems
- ☐ ISDN equipment
- ☐ PBX systems
- ☐ Modems

General Description

The Supertex HV9114 is a BiCMOS/DMOS single-output, pulse width modulator IC intended for use in high-speed high-efficiency switchmode power supplies. It provides all the functions necessary to implement a single-switch current-mode PWM, in any topology, with a minimum of external parts.

Because it utilizes Supertex's proprietary BiCMOS/DMOS technology, it requires less than one tenth of the operating power of conventional bipolar PWM ICs, and can operate at more than twice their switching frequency. Dynamic range for regulation is also increased, to approximately 8 times that of similar bipolar parts. It starts directly from any DC input voltages between 15 and 200VDC, requiring no external power resistor. The output stage is push-pull CMOS and thus requires no clamping diodes for protection, even when significant lead length exists between the output and the external MOSFET. The clock frequency is set with an external resistor and capacitor.

Accessory functions are included to permit fast remote shutdown (latching or nonlatching) and undervoltage shutdown.

For similar ICs intended to operate directly from up to 450VDC input, please consult the data sheet for the HV9120/9123.

Absolute Maximum Ratings*

$+V_{IN}$, Input Voltage	200VDC
V_{DD}, Logic Voltage	15.5VDC
Logic Input Voltage	-0.3V to V_{DD}+0.3V
Storage Temperature	-65°C to 150°C
Power Dissipation, SOIC	750mW
Power Dissipation, Plastic DIP	1000mW
Power Dissipation, Ceramic DIP	1000mW

*All voltages reference to $-V_{IN}$.

Electrical Characteristics

(Unless otherwise specified, V_{DD} = 10V, $-V_{IN}$ = 0V oscillator disabled.)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
Reference						
V_{REF}	Output Voltage	3.94	4.00	4.06	V	OSC, T_A = 25°C
		3.88	4.00	4.12	V	OSC disabled over voltage and temperature ranges
I_{SHORT}	Short Circuit Current		-15	-5	ma	$V_{REF} = -V_{IN}$
$\Delta V_R/\Delta I_R$	Load Regulation		3	40	mV	I_{REF} = 0 to -3ma
Oscillator						
f_{OSC}	Initial Accuracy[2]	90	100	110	KHz	R_{OSC} = 374KΩ, C_{OSC} = 200pF
		450	500	550		R_{OSC} = 133KΩ, C_{OSC} = 100pF
Δf/f	Voltage Stability		1	2%	%	R_{OSC} = 133KΩ, C_{OSC} = 100pF [f(13.5V) - f(9.5V)]/f(9.5V)
OSC T_C	Temperature Coefficient		200	500	ppm/°C	T_A = -40°C to 85°C, f_{OSC} = 100KHz
I_{SYNC}(S)	Sync Output Current (Slave Mode)		±1	±500	µa	$V_{ROSC} = V_{DD}$
I_{SYNC}(M)	Sync Output Current (Master Mode)	±1.0	±3.0		ma	$V_{ROSC} \leq 5V$
PWM						
D_{MAX}	Maximum Duty Cycle	49.0	49.4	49.6	%	
D_{MIN}	Deadtime		225		nsec	
	Minimum Duty Cycle			0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]		80	125	nsec	
Current Limit						
V_{SENSE}	Current Limit Threshold Voltage	1.15	1.23	1.30	V	V_{FB} = 0V, NI = V_{REF}
t_d	Current Limit Delay to Output		70	100	ns	V_{SENSE} = 1.5V, $V_{COMP} \leq 2.0V$ (See figure 1)
Error Amplifier ($C_{OSC} = -V_{IN}$)						
V_{FB}	Feedback Voltage	3.94	4.00	4.06		V_{FB} Shorted to Comp
I_{IN}	Input Bias Current		±25	±200	nA	V_{FB} = 5.0V, NI = V_{REF}
V_{OS}	Input Offset Voltage		±5	±25	mV	
A_{VOL}	Open Loop Voltage Gain[1]	65	88		dB	
GB	Unity Gain Bandwidth[1]	1.5	2.3		MHz	
PSRR	Power Supply Rejection	50	88		dB	$9.5 \leq V_{DD} \leq 13.5V$
I_{SOURCE}	Output Source Current		-2.0	-1.0	mA	V_{FB} = 3.5V, NI = V_{REF}
I_{SINK}	Output Sink Current	1.0	4.0		mA	V_{FB} = 4.5V, NI = V_{REF}

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC IN pin must be ≤5pF.

Electrical Characteristics (continued)

(Unless otherwise specified, V_{DD} = 10V, $-V_{IN}$ = 0V, oscillator disabled)

Symbol	Parameters	Min	Typ	Max	Unit	Conditions
Pre-regulator/Startup						
I_{IN}	Input Leakage Current		1	10	µA	$+V_{IN}$ = 200V, $V_{DD} \geq$ 10V
I_{START}	Pre-regulator Start-up Current	8	20		ma	$+V_{IN}$ = 48V, tpw ≤ 300µs $V_{DD} = V_{UVLO}$
V_{PR}	V_{DD} Pre-regulator Voltage	8.8	9.1	9.4	V	V_{IN} = 48V
V_{DELTA}	$V_{PR} - V_{UVLO}$ (turn-on)	0.1	0.2	0.7	V	
V_{HYST}	Undervoltage Lockout Hysteresis	0.18	0.3	0.4	V	
Supply						
I_{DD}	Supply Current		1.3	2.5	mA	$C_L \leq$ 50pF, f_{OSC} = 100KHz
			1.8	3.0		$C_L \leq$ 50pF, f_{OSC} = 500KHz
V_{DD}	Operating Range	9.5		13.5	V	
Shutdown Logic						
V_{SD}	$\overline{\text{Shutdown}}$ Logic Threshold		2.5	0.5	V	
t_{SD}	$\overline{\text{Shutdown}}$ Delay to Latched Output		0.30	1.0	µs	See figure 2
I_{SD}	$\overline{\text{Shutdown}}$ Pull-up Current	12	17	30	µA	V_{SD} = 0V
I_{SS}	Soft-start Current	12	17	30	µA	
$V_{SS(off)}$	Output Inhibit Voltage		1.7	0.5	V	Soft-start to disable driver output
Output						
V_{OH}	Output High Voltage	9.85	9.9		V	I_{OUT} = 10mA
V_{OL}	Output Low Voltage		0.05	0.15	V	I_{OUT} = -10mA
I_{SOURCE}	Peak Output Current		400	200	mA	V_{OUT} = 0V
I_{SINK}	Peak Output Current	-500	-700		mA	$V_{OUT} = V_{DD}$

Note:

1. Guaranteed by design. Not subject to production test.
2. Stray C on OSC in pin must be ≤ 5pF.

Shutdown Timing Waveforms

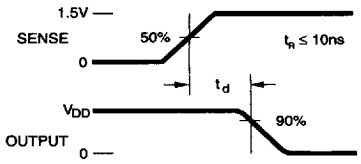


Figure 1

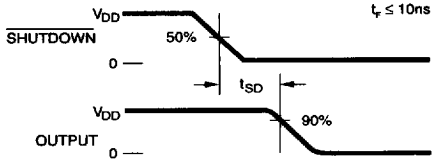
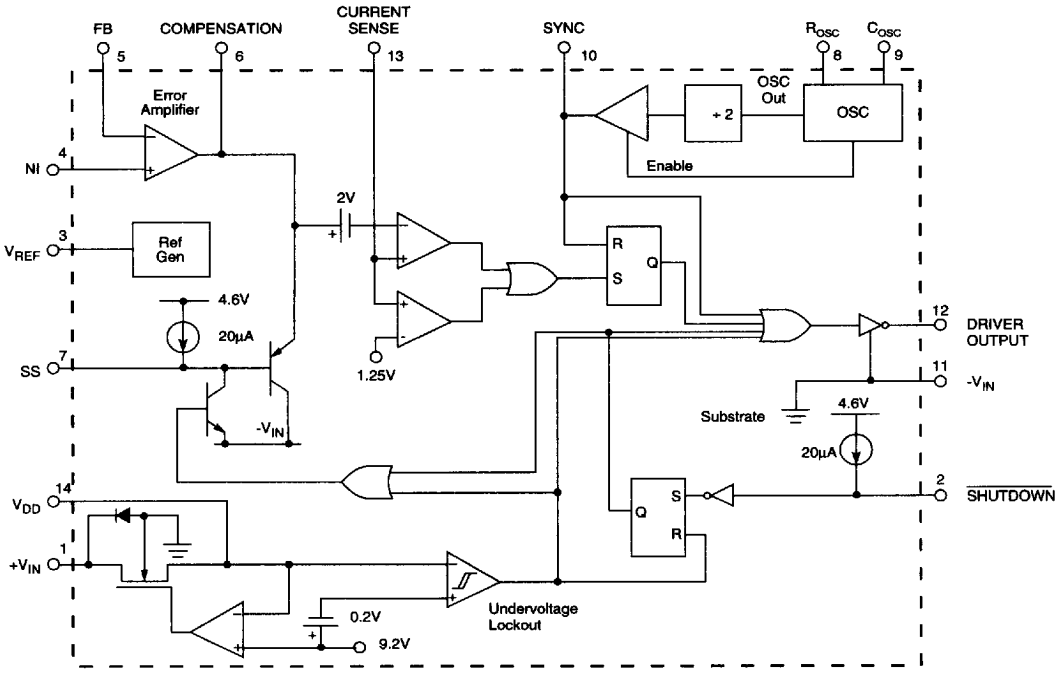


Figure 2

Functional Block Diagram



Detailed Description

Preregulator

The preregulator/startup circuit for the HV9114 consists of a high-voltage N-channel depletion-mode DMOS transistor driven by an error amplifier to form a variable current path between the V_{IN} terminal and the V_{DD} terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 8.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling) no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip in the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the *effective* gate capacitance of the MOSFET being driven, i.e.,

$C_{storage} \geq 100$ x (gate charge of FET at 10V ÷ 10V)

as well as very good high frequency characteristics. Stacked polyester or ceramic caps work well. Electrolytics capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Clock Oscillator

The clock oscillator of the HV9114 consists of a ring of CMOS inverters, and a frequency dividing flip-flop. a single external resistor and capacitor are required to set oscillator frequency.

Reference

The Reference of the HV9114 consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of 1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be.

Error Amplifier

The error amplifier in the HV9114 is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: A PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV9114 uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

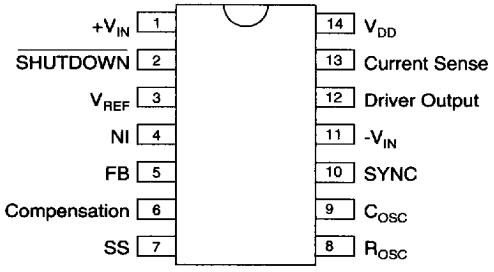
Shutdown

The shutdown pin of the HV9114 can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used they should be left open, or connected to V_{DD}.

Output Buffer

The output buffer of the HV9114 is of standard CMOS construction (P-channel pull-up, N-channel pull-down). Thus the body-drain diodes of the output stage can be used for spike clipping if necessary, and external Schottky diode clamping of the output is not required.

Pinout



14 Pin SOIC/DIP Package