Preliminary

RICMOS™ SEA OF TRANSISTORS GATE ARRAY HX1060

FEATURES

RADIATION HARDNESS

- Total Dose Hardness of >1x10^6 rad(SiO_2)
- Dose Rate Upset Hardness to 1x10^{11} rad(Si)/sec
- Dose Rate Survivability to 1x10^{13} rad(Si)/sec
- SEU Hardness to 1x10^{-11} upsets/bit-day (Flip-Flops & SRAMs)
- Neutron Fluence Hardness to 1x10^{14} cm^{-2}

PERFORMANCE

- Typical Gate Delays of 0.5 ns (Post-Radiation)
- Flip-Flop Toggle Frequencies of 200 MHz
- Capable of Supporting System Speeds of 30 MHz

OTHER

- In production on Honeywell's 1.2 µm Minimum Feature RICMOS™ - SOI Process
- Devices Available as a QML Class V or Class Q in addition to Class B or modified Class S
- Outside Foundry Netlist Import Capability
- 60K Gates: 24K Usable Minimum
- I/O Compiler With Over 200 Options
- Compatible with TTL or CMOS I/O
- Configurable 2K SRAM or 16K ROM
- Up to 254 Useable I/O Pads

4

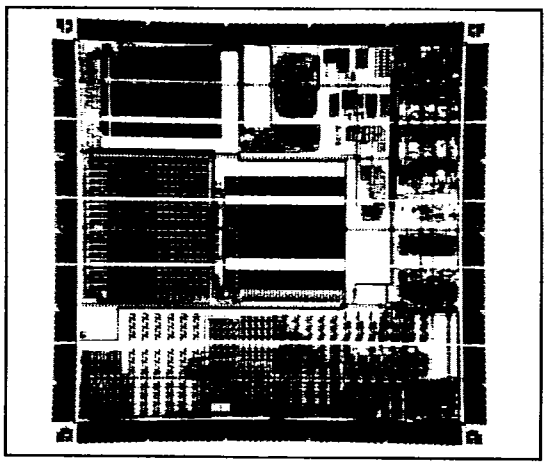
GENERAL DESCRIPTION

The RICMOS™ HX1060 is a performance-oriented radiation-hardened sea of transistors gate array based on the RICMOS™ process. The high density and performance characteristics of the RICMOS™ Silicon-On-Insulator (SOI) process allow the HX1060 to operate up to 30 MHz over the full military temperature range after exposure to ionizing radiation exceeding 1x10^6 rad(SiO_2). Flip-Flops and SRAMs have been hardened to Single Event Upsets (SEU) to less than 1x10^{-10} errors/bit-day. ROMs are SEU immune.

Logic designers need not have a background in radiation hardening. Honeywell's VDS ToolKit™ provides a full suite of user friendly design tools encompassing static timing analysis, test program generation, and automated place and route. User friendliness is enhanced through the use of design aids known as soft macro compilers which increase the designer's productivity during the schematic capture phase of the design cycle. The library for HX1060 is virtually identical to Honeywell's RICMOS Standard Cell Library.

HX1060's design system contains 30 SSI logic elements, 13 data storage elements, five MSI soft macro compilers, two LSI supercells, and over 200 I/O pad options. Configurable SRAMs and configurable ROMs can be sized in single-bit increments to 64 bits. The library allows system integration of over 24,000 gates per chip with up to 254 signal pins.

Each I/O site can be either Input, Output, or Bidirectional. The I/O cells are IEEE 1149.1 compatible. An I/O compiler with over 200 options can configure for TTL/CMOS, high or low drive, pull up/pull down resistors, and Schmitt triggers. The HX1060 also supports SSD (Synchronous Scan Design) which permits scan path testing on all flip-flops and registers. The HX1060 is available as a QML Class V or Class Q device or can be screened to meet either Class B and modified Class S requirements.



HX1060 Characteristics	
Raw / Usable Gate Count	61,820 / 24,000
Typical Delay	0.5 ns
Maximum Flip-Flop Toggle Frequency	200 MHz
I/O Interface Levels	CMOS, LSTTL, Schmitt Trigger
Total Package Pins Available	84 to 256 (LDCC)
Input/Output Pins	Up to 254
Typical Power Dissipation	0.5 to 1.5W
Operating Temperature	-55 to 125°C
Process Technology (1)	RICMOS™ SOI
Minimum Geometry	1.2µm
Design-For-Test Technique(2)	SSD/ IEEE 1149.1 Boundary Scan

(1) RICMOS™ SOI (Radiation Insensitive CMOS Silicon-On-Insulator) process technology
(2) SSD (Synchronous Scan Design). Refer to Honeywell's RICMOS™ ASIC Library Data Book for more information.

Total Ionizing Radiation Dose

Each cell in the library meets all stated functional and electrical specifications after a total ionizing radiation dose of $1x10^6$ rad(SiO_2) applied under recommended operating conditions.

Transient Pulse Ionizing Radiation

Each integrated circuit designed with the HX1060 is capable of writing, reading, and retaining stored data through a 20 ns transient ionizing radiation pulse of over $1x10^{11}$ rad(Si)/second, applied under recommended operating conditions. Additionally, all devices are capable of meeting all functional and electrical specifications after exposure to a 20 ns transient ionizing radiation pulse of over $1x10^{13}$ rad(Si)/second applied under recommended operating conditions. Note that the current conducting during the transient ionizing radiation pulse by the inputs, outputs, and power supply may significantly exceed the normal operating values. The system design must accommodate these increases.

Neutron Radiation

Each integrated circuit designed with the HX1060 will meet all stated functional and electrical specifications after a total neutron fluence of over $1x10^{14}$ neutrons/cm^2, applied under recommended operating conditions, assuming an equivalent neutron energy of 1 MeV.

Latchup

The HX1060 integrated circuits will not latch up when exposed to any of the above radiation conditions applied under recommended operating conditions. The on-chip power supply grid is designed and placed first, according to cell block placement to guard against excessive supply voltage drop. Special guardbanding within each cell help to minimize any parasitic transistors that cause latchup to occur.

HONEYWELL/S S E C

HX1060 Cell Library Index

Cell Description	Note	Pre-Rad Intrinsic Delay Rising	Pre-Rad Intrinsic Delay Falling	Pre-Rad Loading Factor Rising	Pre-Rad Loading Factor Falling	Post-Rad Intrinsic Delay Rising	Post-Rad Intrinsic Delay Falling	Post-Rad Loading Factor Rising	Post-Rad Loading Factor Falling
Inverters/Buffers									
Inverter 1X Power		0.54	0.63	0.93	0.97	0.60	0.52	1.00	0.85
Inverter 2X Power		0.48	0.60	0.53	0.50	0.59	0.45	0.53	0.47
Inverter 3X Power		0.44	0.56	0.40	0.36	0.55	0.41	0.39	0.35
Inverter 4X Power		0.42	0.55	0.32	0.29	0.53	0.39	0.31	0.28
Inverter 5X Power		0.41	0.53	0.27	0.24	0.52	0.38	0.26	0.24
Buffer 1X Power		0.28	0.36	1.41	1.60	0.31	0.30	1.52	1.37
Buffer 4X Power		1.29	1.29	0.30	0.30	1.18	1.29	0.31	0.28
Tristate Inverter		0.89	1.02	0.89	0.86	1.04	0.82	0.97	0.75
Combinational Logic									
2 Input NAND		0.72	0.95	0.93	1.65	0.79	0.78	1.01	1.43
3 Input NAND		0.86	1.58	0.96	2.34	0.95	1.33	1.03	2.03
4 Input NAND		0.98	2.48	0.98	3.03	1.09	2.12	1.06	2.63
2 Input AND		0.35	0.39	1.68	1.60	0.39	0.33	1.86	1.37
3 Input AND		0.44	0.47	1.89	1.84	0.55	0.39	2.14	1.38
4 Input AND		2.64	1.44	1.17	1.04	2.48	1.46	1.21	0.93
2 Input NOR		0.69	0.73	1.75	0.99	0.80	0.64	1.94	0.86
3 Input NOR		0.47	0.86	1.07	1.11	0.54	0.68	1.12	0.91
2 Input OR		0.31	0.47	1.42	2.05	0.34	0.38	1.52	1.68
3 Input OR		0.37	0.66	1.42	2.40	0.41	0.48	1.52	1.92
2 Input XOR		2.02	2.00	1.03	0.99	2.08	1.96	1.08	0.97
2 Input XNOR		1.07	1.45	1.62	1.66	1.04	1.44	1.95	1.43
2 Input OR to 2 Input NAND		1.16	1.37	1.77	1.69	1.32	1.12	1.96	1.48
2 Input AND to 2 Input NOR		1.13	1.30	1.76	1.73	1.28	1.04	1.96	1.51
2X2 Input AND to 2 Input OR		1.43	1.30	0.96	1.66	1.34	1.31	1.04	1.44
3X2 Input AND to 3 Input OR		1.60	1.88	0.97	2.34	1.52	1.81	1.04	2.04
4X2 Input AND to 4 Input OR		1.63	2.18	0.96	3.01	1.53	2.08	1.04	2.62
Multiplexers									
2 to 1 MUX	Data	1.76	1.53	0.98	1.66	1.65	1.50	1.05	1.44
	Select	1.78	1.64	0.98	1.66	1.65	1.62	1.04	1.44
4 to 1 MUX	Data	2.87	3.28	1.06	3.03	2.75	3.06	1.12	2.64
	Select	4.42	4.59	1.06	3.02	4.24	4.34	1.12	2.63
Adders									
1 Bit Half Adder	Sum	2.10	2.11	1.02	0.98	2.13	1.95	1.08	0.93
	Carry	1.57	1.26	1.03	1.03	1.46	1.28	1.08	0.91
1 Bit Full Adder	Sum	4.26	4.45	0.97	0.98	4.04	4.37	1.03	0.84
	Carry	1.03	1.04	0.89	1.09	0.87	1.03	0.89	0.91
Latches (Positive Level)									
D Latch	D to Q	2.37	2.40	1.09	1.18	2.16	2.43	1.12	1.09
	EN to Q	2.81	3.22	1.09	1.18	2.75	3.16	1.13	1.11
D Latch (SEU-hard)	D to Q	2.16	2.23	0.66	0.70	1.98	2.24	0.67	0.67
	EN to Q	2.91	3.36	0.66	0.69	2.90	3.28	0.66	0.67
D Latch W/Set & Reset	D to Q	2.38	2.42	1.09	1.17	2.17	2.43	1.12	1.09
	EN to Q	2.82	3.24	1.09	1.16	2.76	3.17	1.13	1.09
D Latch W/Set & Reset (SEU-hard)	D to Q	2.17	2.23	0.65	0.71	1.99	2.27	0.66	0.66
	EN to Q	2.92	3.51	0.67	0.70	2.91	3.43	0.66	0.67

Cell Library Index (cont.)

Cell Description	Note	Pre-Rad Intrinsic Delay Rising	Pre-Rad Intrinsic Delay Falling	Pre-Rad Loading Factor Rising	Pre-Rad Loading Factor Falling	Post-Rad Intrinsic Delay Rising	Post-Rad Intrinsic Delay Falling	Post-Rad Loading Factor Rising	Post-Rad Loading Factor Falling
Flip-Flops (Positive Edge Trigger)									
D Flip-Flop	CLK to Q	3.48	3.66	0.94	0.99	3.23	3.51	1.01	0.87
D Flip-Flop W/NFT	CLK to Q	3.49	3.66	0.94	1.01	3.24	3.52	1.01	0.87
D Flip-Flop (SEU-hard)	CLK to Q	3.23	2.98	0.66	0.70	3.18	2.67	0.66	0.65
D Flip-Flop W/NFT (SEU-hard)	CLK to Q	3.94	4.31	0.50	0.52	2.36	2.47	0.79	0.81
D Flip-Flop W/Reset	CLK to Q	2.73	2.77	1.11	1.22	2.66	2.50	1.15	1.13
D Flip-Flop W/Reset (SEU-hard)	CLK to Q	4.42	4.56	0.66	0.57	4.20	4.38	0.67	0.52
D Flip-Flop W/Set & Reset	CLK to Q	4.11	3.90	1.03	1.02	3.84	3.78	1.08	0.10
D Flip-Flop W/Set & Reset (SEU-hard)	CLK to Q	3.77	4.21	0.56	0.51	3.56	4.09	0.57	0.47
I/O									
Nominal Drive Ouput		1.82	1.74	0.03	0.04	2.30	2.47	0.03	0.03
High Drive Output		1.95	1.87	0.02	0.02	1.70	1.76	0.02	0.02
Nom. Drive Tristate Output W/Enable		2.13	1.97	0.03	0.04	1.85	1.86	0.03	0.03
High Drive Tristate Output W/Enable		2.29	2.08	0.02	0.02	2.03	1.95	0.02	0.02
Nominal Drive Bi-Dir. Output W/Enable	Input	1.03	1.06	0.30	0.31	0.81	0.87	0.19	0.20
	Output	2.14	1.99	0.03	0.04	1.87	1.88	0.03	0.03
High Drive Bi-Dir. Output W/Enable	Input	1.03	1.06	0.30	0.31	0.81	0.87	0.19	0.20
	Output	2.29	2.07	0.02	0.02	2.03	1.96	0.02	0.20
TTL Inverting/Noninverting Input		0.55	0.76	0.30	0.31	0.41	0.37	0.24	0.27
CMOS Inverting/Noninverting Input		4.24	7.00	0.31	0.30	3.78	2.69	0.26	0.26
		4.33	6.89	0.31	0.30	3.86	2.55	0.26	0.25
Miscellaneous Cells									
2 to 32 Bit Configurable Binary Counter		Design Dependent							
2 to 32 Bit Configurable Shift Register		Design Dependent							
To 2K Configurable RAM		Design Dependent							
To 16K Configurable ROM		Design Dependent							

Nominal Gate Delay Calculation

For calculating the nominal delay of any give gate in the library the following equations should be used:

$$D_{Falling} = D_{Intrinsic\ Falling} + LF_{Falling} * C_L$$

$$D_{Rising} = D_{Intrinsic\ Rising} + LF_{Rising} * C_L$$

This equation assumes nominal conditions, i.e., the junction temperature 25°C and the supply voltage (VDD) is 5.0V. The capacitive load (C_L) should be expressed in pF and the loading factor (LF) is from the Cell Library Index table above. The equation is expressed in nanoseconds.

Power Dissipation Calculation

The typical Power Dissipation for any given implementation of the HX1060 is given by the following equation:

Power(mW) = $(V_{DD})^2$ * (Clock Frequency) * [(0.25) * (# of Nets * 0.5pF)+(0.25 * (#of Output Pads) * 50pF)].

RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Military Limits			Units
		Min	Typ	Max	
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Free-Air Temperature	-55		125	°C

ABSOLUTE MAXIMUM RATINGS (1)

Parameter	Description	Rating	Units
V_{DD}	Supply Voltage	+7.0	V
V_{IN}	Input Voltage Continuous	-0.5 to (V_{DD}+0.5)	V
V_O	Voltage Applied to Three-State Output in Off-State	-0.5 to (V_{DD}+0.5)	V
T_J	Junction Temperature	+175	°C

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods of time may adversely effect devices.

DC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Military Limits			Units
		Min	Typ	Max	
V_{IH}	CMOS Input Buffer	0.7*V_{DD}			V
	TTL Input Buffer	2.2			V
V_{IL}	CMOS Input Buffer			0.3*V_{DD}	V
	TTL Input Buffer			0.8	V
I_{IN}	TTL/CMOS Input Buffer $0 \le V_{IN} \le V_{DD}$	-10		10	µA
V_{OL}	Output Buffers I_{OL} = max (3-15 mA options)	400			mV
V_{OH}	Output Buffers I_{OH} = max (3-15 mA options)			4.0	V

HONEYWELL/S S E C

Radiation-Hardened Assurance Plan

Honeywell radiation-hardened integrated circuits are designed and processed to meet all stated functional and electrical specifications after a total ionizing radiation dose of one Mrad (SiO_2). All circuits are designed to remain within design specifications after rebound at 5.5V, 125°C extrapolated to ten years. Honeywell assures the total dose radiation hardness of its devices by:

- Total dose testing of process monitor structures at wafer level
- Total dose testing of product at wafer level
- Package level testing per MIL-STD-883, Method 5005, Group E, if requested by the customer.

Wafer level testing is done using a 10KeV X-ray radiation source. To ensure that the wafer level X-ray testing is equivalent to standard military test environments, several experiments have been performed to determine the correlation between X-ray and Cobalt-60 gamma ray sources. Both performance and transistor parametric shifts have been analyzed. The results have shown that the X-ray radiation source provides an equivalent radiation environment and, in many cases, induces more degradation than an equivalent dose on a Cobalt-60 source.

On every wafer lot, two die from each of the three wafers are dosed on an X-ray radiation source. The dosing is done in three increments up to, and including, one Mrad (SiO_2). The data is reviewed to determine if the parameters are within specified levels. The wafer lots are sent on for packaging only if they pass the electrical test limits at one Mrad (SiO_2).

Package level total dose radiation testing is performed per MIL-STD-883, Method 5005, Group E, if required by the customer. An alternative to the MIL-STD testing is to modify the sample size and/or perform the testing on the in-house X-ray source.

The radiation hardness assurance strategy starts with a design and technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by monitoring key process monitor parameters to which hardness is sensitive, before and after exposure to total dose radiation. In addition, the radiation hardness of product samples from every lot is assured. This Total Quality approach ensures our customers of a reliable product by engineering reliability into the process development and guaranteeing that quality through extensive qualification and screening.

900120
5/93