Aerospace Electronics

FIFO—SOI

HX6409
HX6218
HX6136

FEATURES

- 1K x 36, 2K x 18, 4K x 9 Organizations
- Fabricated with RICMOS™ IV Silicon on Insulator (SOI) 0.8 µm Process (L_{eff} = 0.65µm)

RADIATION

- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- Dose Rate Survivability through $1x10^{11}$ rad(Si)/s
- Soft Error Rate of $<1x10^{-10}$ upsets/bit-day
- No Latchup

OTHER

- Read/Write Cycle Times <35 ns (-55° to 125°C)
- Expandable in Width
- Supports Free-Running 50% Duty Cycle Clock
- Empty, Full, Half Full, 1/4 Full, 3/4 Full, Error Flags
- Parity Generation/Checking
- Fully Asynchronous with Simultaneous Read and Write Operation
- Output Enable (OE)
- CMOS or TTL Compatible I/O
- Single 5 V ± 10% Power Supply
- Various Flat Pack Options

GENERAL DESCRIPTION

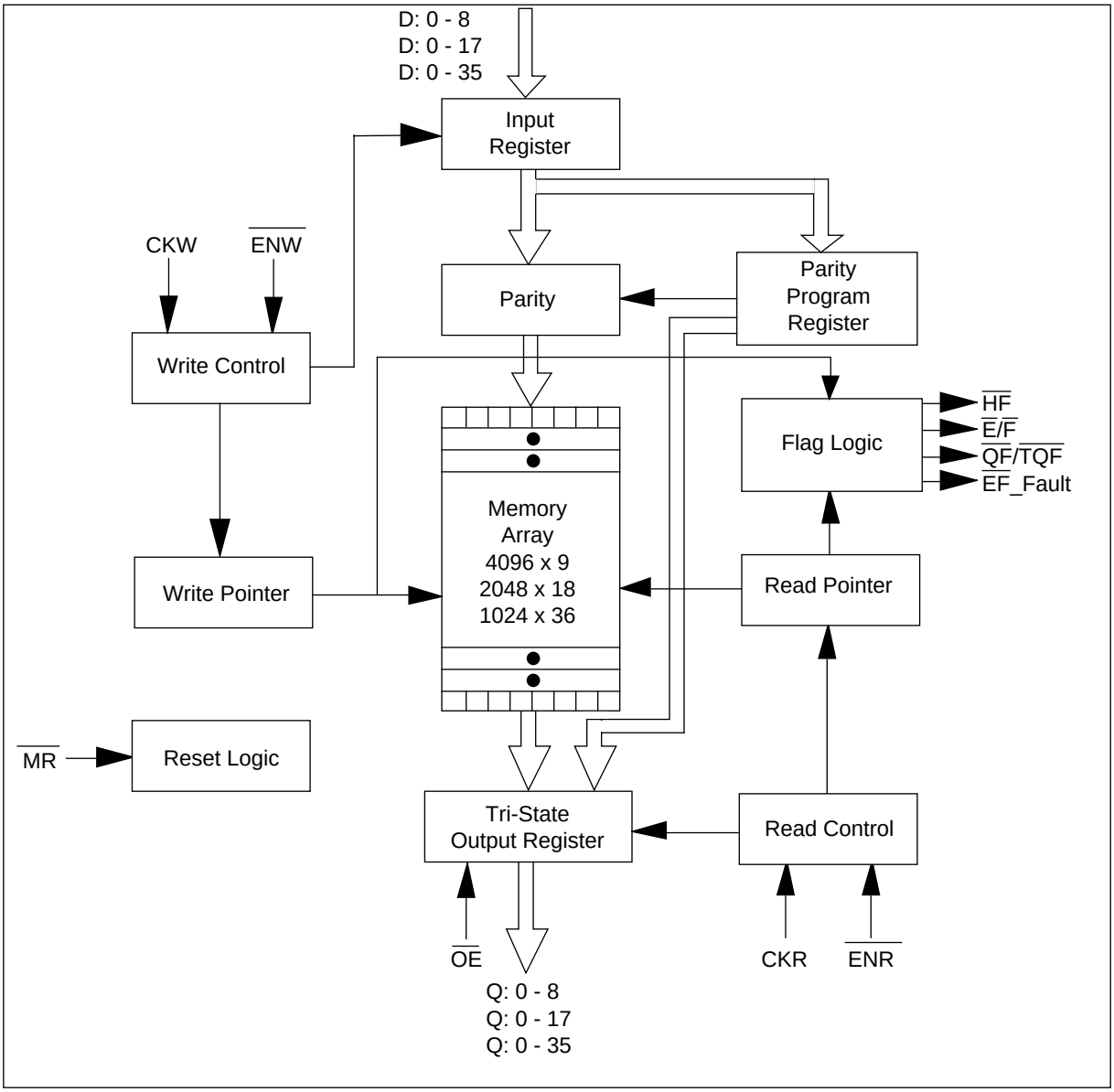
The HX6409, HX6218, and HX6136 are high speed, low-power, first-in first-out memories with clocked read and write interfaces. The HX6409 is a 4096 word by 9 bit memory array, the HX6218 is a 2048 word by 18 bit memory array, and the HX6136 is a 1024 word by 36 bit memory array. The FIFOs support width expansion while depth expansion requires external logic control using state machine techniques. Features include programmable parity control, an empty/full flag, a quarter/three quarter full flag, a half full flag and an error flag.

These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering. These FIFOs have separate input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free running clock (CKW) and a write enable pin $\overline{ENW}$. When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle.

The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). In addition, the three FIFOs have an output enable pin ($\overline{OE}$) and a master reset pin ($\overline{MR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 30 MHz are achievable in the three configurations.

Honeywell's enhanced SOI RICMOS™ IV (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. The FIFO is fabricated with Honeywell's radiation hardened technology, and is designed for use in systems operating in radiation environments. The SOI RICMOS™ IV process is a 5-volt, SIMOX CMOS technology with a 150 Å gate oxide and a minimum drawn feature size of 0.8 µm, (0.65 µm effective gate array—L_{eff}). Additional features include tungsten via plugs, Honeywell's proprietary SHARP planarization process, and a lightly doped drain (LDD) structure for improved short channel reliability.

LOGIC BLOCK DIAGRAM



FLAG DECODE TABLE

					Word Count		
$\overline{EF}$_Fault	$\overline{E}$/ $\overline{F}$	$\overline{QF}$/TQ$\overline{F}$	$\overline{HF}$	**State**	**4K x 9**	**2K x 18**	**1K x 36**
0	0	0	1	Empty Fault (Enabled Read when Empty)	0	0	0
1	0	0	1	Empty	0	0	0
1	1	0	1	Less than or Equal to 1/4 Full	1 to 1024	1 to 512	1 to 256
1	1	1	1	Less than or Equal to 1/2 Full	1025 to 2048	513 to 1024	257 to 512
1	1	1	0	Greater that 1/2 Full	2049 to 3071	1025 to1535	513 to 767
1	1	0	0	Greater than or Equal to 3/4 Full	3072 to 4095	1536 to 2047	768 to 1023
1	0	0	0	Full	4096	2048	1024
0	0	0	0	Full Fault (Enabled Write when Full)	4096	2048	1024

SIGNAL DEFINITIONS

Signal Name	I/O	Description
D: 0 - 35	I	Data Inputs: Data Inputs are written into the FIFO on the rising edge of CKW when $\overline{ENW}$ is active and the FIFO is not full.
Q: 0 - 35	O	Data Outputs: Data Outputs are read out of the FIFO memory and updated on the rising edge of CKR when $\overline{ENR}$ is active and the FIFO is not Empty. The Data Outputs are in a high impedance state if $\overline{OE}$ is not active.
$\overline{ENW}$	I	Enable Write: An active low signal that enables the write of the Data Inputs on the CKW rising edge (if FIFO is not full).
$\overline{ENR}$	I	Enable Read: An active low signal that enables the read and update of the Data Outputs on the CKR rising edge (if FIFO is not empty).
CKW	I	Write Clock: The rising edge clocks data into the FIFO when $\overline{ENW}$ is low (active). On the rising edge, this signal also updates the Half Full, 3/4 Full, Full, and Full Fault Flags.
CKR	I	Read Clock: The rising edge clocks data out of the FIFO when $\overline{ENR}$ is low (active). On the rising edge, this signal also updates the 1/4 Full, Empty, and Empty Fault Flags.
$\overline{HF}$	O	Half Full Flag: Updated on the rising edge of CKW and indicating that the FIFO is greater than half full.
$\overline{E}$/ $\overline{F}$	O	Empty or Full Flag: Empty is updated on the rising edge of CKR, and Full is updated on the rising edge of CKW.
$\overline{QF}$/$\overline{TQF}$	O	1/4 Full or 3/4 Full Flag: 1/4 Full is updated on the rising edge of CKR, and 3/4 Full is updated on the rising edge of CKW. 1/4 Full signifies 256 or less words in the 1K x 36 FIFO and 3/4 Full signifies 256 words or less until a full condition.
$\overline{EF}$_Fault	O	Empty or Full Fault Flag: empty Fault is updated on the rising edge of CKR, and Full Fault is updated on the rising edge of CKW. Empty Fault signifies a read to an already empty FIFO, and Full Fault signifies a write to an already full FIFO. Once a fault condition is detected, the Fault Flag remains latched until the empty or full condition is removed.
$\overline{MR}$	I	Master Reset: Active low signal which, when active, resets device to empty condition.
$\overline{OE}$	I	Output Enable: Active low signal which, when active, enables low impedance Data Outputs, Q: 0 - 35.

PROGRAMMABLE PARITY OPTIONS

D2	D1	D0	Conditions
O	X	X	Parity Disabled
I	O	O	Generate Even Parity, Q8, Q17, Q26, Q35
I	O	I	Generate Odd Parity, Q8, Q17, Q26, Q35
I	I	O	Check for Even Parity, Error on Q8, Q17, Q26, Q35, Error is a Low Signal
I	I	I	Check for Odd Parity, Error on Q8, Q17, Q26, Q35, Error is a Low Signal

RADIATION CHARACTERISTICS

Total Ionizing Radiation Dose

All FIFO configurations will meet all stated functional and electrical specifications over the entire operating temperature range after the specified total ionizing radiation dose. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T = 125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and product using 10 KeV X-ray and radiation sources. Transistor gate threshold shift correlations have been made between 10 KeV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

Each FIFO configuration is capable of writing, reading and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤50 ns duration up to $1x10^9$ rad(Si)/s, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation (timing degradation during transient pulse radiation is ≤10%), it is suggested that stiffening capacitance be placed near the package VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitor of 0.7 nH per part. If there are no operate-through or valid stored data requirements, typical circuit board mounted de-coupling capacitors are recommended.

Each FIFO will meet any functional or electrical specification after exposure to a radiation pulse of ≤50 ns duration up to $1x10^{11}$ rad(Si)/s, when applied under recommended operating conditions. Note the current conducted during the pulse by the inputs, outputs and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

Each FIFO configuration will meet any functional or timing specification after a total neutron fluence of up to $1x10^{14}$ cm^{-2} applied under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

This FIFO configuration has a soft error rate (SER) performance of $<1x10^{-10}$ upsets/bit-day, under recommended operating conditions. This hardness level is defined by the Adams 90% worst case cosmic ray environment.

Latchup

This FIFO configuration will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SIMOX substrate with its oxide isolation ensure latchup immunity.

RADIATION-HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	$\geq 1x10^6$	rad(SiO_2)	T_A=25°C
Transient Dose Rate Upset	$\geq 1x10^9$	rad(Si)/s	Pulse width ≤50 ns
Transient Dose Rate Survivability	$\geq 1x10^{11}$	rad(Si)/s	Pulse width ≤50 ns, X-ray, VDD=6.0 V, T_A=25°C
Soft Error Rate	$<1x10^{-10}$	upsets/bit-day	T_A=125°C, Adams 90% worst case environment
Neutron Fluence	$\geq 1x10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, T_A=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.
(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to 125°C.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating		Units
		Min	Max	
VDD	Supply Voltage Range (2)	-0.5	7.0	V
VPIN	Voltage on Any Pin (2)	-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)	-65	150	°C
TSOLDER	Soldering Temperature (5 Seconds)		270	°C
PD	Maximum Power Dissipation (3)		2.5	W
IOUT	DC or Average Output Current		25	mA
VPROT	ESD Input Protection Voltage (4)	2000		V
ΘJC	Thermal Resistance (Jct-to-Case)		5	°C/W
TJ	Junction Temperature		175	°C

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) FIFO power dissipation (IDDSB + IDDOP) plus FIFO output driver power dissipation due to external loading must not exceed this specification.
(4) Class 2 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical (1)	Worst Case		Units	Test Conditions
			Min	Max		
CI	Input Capacitance			7	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance			9	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only.

DATA RETENTION CHARACTERISTICS

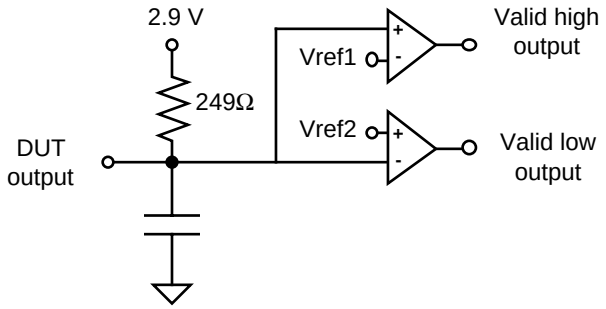
Symbol	Parameter	Typical (1)	Worst Case (2)		Units	Test Conditions
			Min	Max		
VDR	Data Retention Voltage		2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current			500	µA	NCS=VDD=VDR VI=VDR or VSS

(1) Typical operating conditions: TA= 25°C, pre-radiation.
(2) Worst case operating conditions: TC= -55°C to +125°C, post total dose at 25°C.

DC ELECTRICAL CHARACTERISTICS

Symbol	Test Parameters	Worst Case (1) Min	Worst Case (1) Max	Units	Conditions
VIH	Input High Voltage CMOS TTL	0.7xVDD 2.2	—	V	VDD=5.5V
VIL	Input Low Voltage CMOS TTL	—	0.3xVDD 0.8	V	VDD=4.5V
VOH1	High Output Voltage	3.5	—	V	VDD=4.5V IOH=-4.0ma
VOH2	High Output Voltage	VDD-0.4	—	V	VDD=4.5V IOH=-100µa
VOL	Low Output Voltage	—	0.4	V	VDD=4.5V IOL=4.0ma
II	Input Leakage Current	-1.0	+1.0	µA	VDD=5.5V VIN=0V or VDD TC=-55°C TO +125°C
IOZL IOZH	Output OFF, High Z Current	-10.0	+10.0	µA	OE≥VIH, VSS<VO<VDD
IDDSB	Standby Power Supply Current (2)	—	1	mA	VIN=0V or VDD CLK(s)=1 MHz
IDDOP	Operating Power Supply Current (2)	—	7	mA	VIN=0V or VDD CLK(s)=1 MHz
IDDSB	Standby Power Supply Current (2)	—	40	mA	VIN=0V or VDD CLK(s)=40MHz
IDDOP	Operating Power Supply Current (2)	—	280	mA	VIN=0V or VDD CLK(s)=40MHz

(1) Worst case operating conditions: VDD =4.5 V to 5.5 V, TC=-55°C to +125°C, post total dose at 25°C.
(2) Standby current for the device includes the Read Clock (CKR) and Write Clock (CKW) only. Both the Read Enable ($\overline{ENR}$) and Write Enable ($\overline{ENW}$) are disabled ($\overline{ENR}$, $\overline{ENW}$=Vdd). For operating currents, $\overline{ENR}$ and $\overline{ENW}$ are enabled (=0.0 V) and data inputs are switching at one half the clock speed between 0.0 V and VDD.



Tester Equivalent Load Circuit

AC TIMING CHARACTERISTICS (1)

Symbol	Test Parameter	Worst Cast (2) —55•C to 125°C Min	Worst Cast (2) —55•C to 125°C Max	Units
TCKW	Write Clock Cycle	24	—	ns
TCKR	Read Clock Cycle	34	—	ns
TCKH	Clock High Read	24	—	ns
TCKH	Clock High Write	14	—	ns
TCKL	Clock Low	10	—	ns
TA	Data Access Time	—	30	ns
TOH	Previous Output Data Hold After Rd High	2	—	ns
TFH	Previous Flag Hold After Rd/Wr High	2	—	ns
TSD	Data Set-UP	9	—	ns
THD	Data Hold	4	—	ns
TSEN	Enable Set-UP	8	—	ns
THEN	Enable Hold	2	—	ns
TOE	OE Low to Output Data Valid	—	10	ns
TOLZ	OE Low to Output Data in Low Z	1	—	ns
TOHZ	OE High to Output Data in High Z	—	10	ns
TFD	Flag Delay	—	17	ns
TSKEW1	Opposite Clock after Clock (3)	0	—	ns
TSKEW2	Opposite Clock before Clock (4)	25	—	ns
TPMR	Master Reset Pulse Width (Low)	25	—	ns
TSCMR	Last Valid Clock Low Set-up to Master Reset Low	0	—	ns
TOHMR	Data Hold from Master Reset Low	2	—	ns
TMRR	Master Reset Recovery	8	—	ns
TMRF	Master Reset High to Flags Valid	—	17	ns
TAMR	Master Reset High to Data Outputs Low	—	17	ns
TSMRP	Parity Program Mode—MR Low Set-up	34	—	ns
THMRP	Parity Program Mode—MR Low Hold	24	—	ns
TFTP	Parity Program Mode—Write HIGH to Read HIGH	34	—	ns
TAP	Parity Program Mode—Data Access Time	—	30	ns
TOHP	Parity Program Mode—Data Hold Time from MR HIGH	4	—	ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V (CMOS), VIL/VIH=0V/3V (TTL), input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing characteristics Table, capacitive output loading C_L=50 pF. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Worst case operating conditions: VDD=4.5V to 5.5V, TC= -55°C to +125°C, post total dose at 25°C.
(3) For flag updates, tskew1 is the minimum time an opposite clock can occur after a clock and still not be included in the current clock cycle. At less that tskew1, inclusion of the opposite clock is arbitrary.
(4) For flag updates, tskew2 is the minimum time an opposite clock can occur before a clock and still be included in the current clock cycle. At less than tskew2, inclusion of the opposite clock is arbitrary.
(5) Timing parameters are defined in Figures 1 through 6.

AC TIMING WAVEFORMS

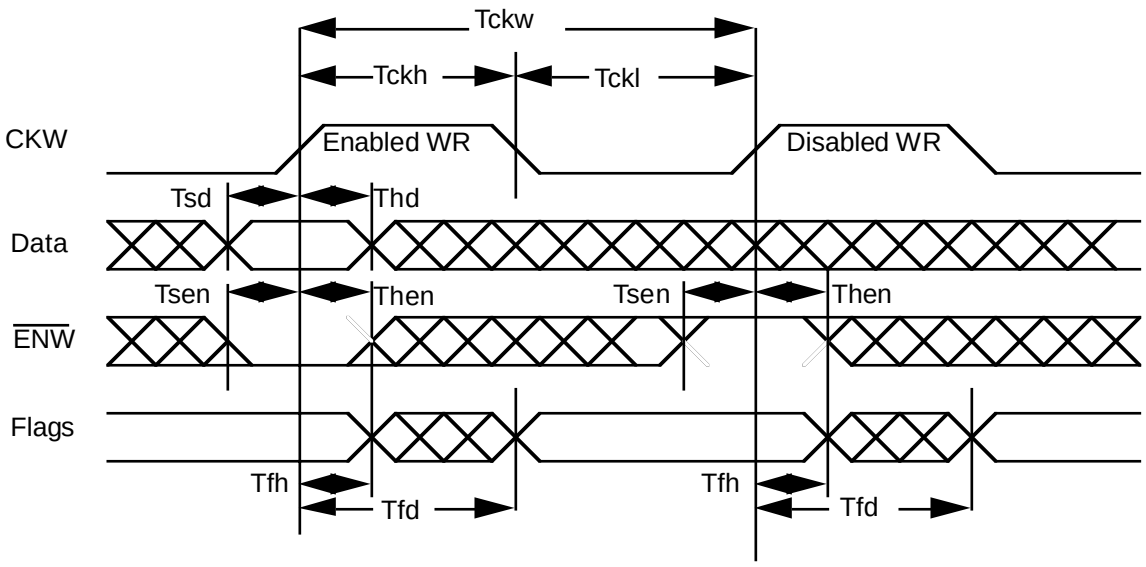


Figure 1. Write Timing

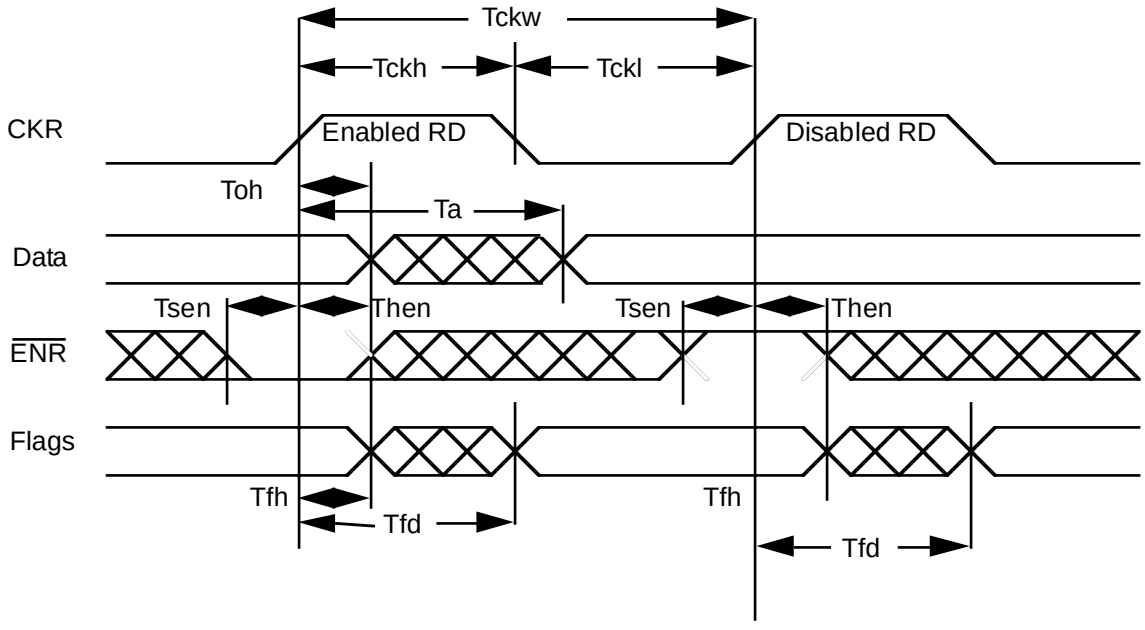


Figure 2. Read Timing

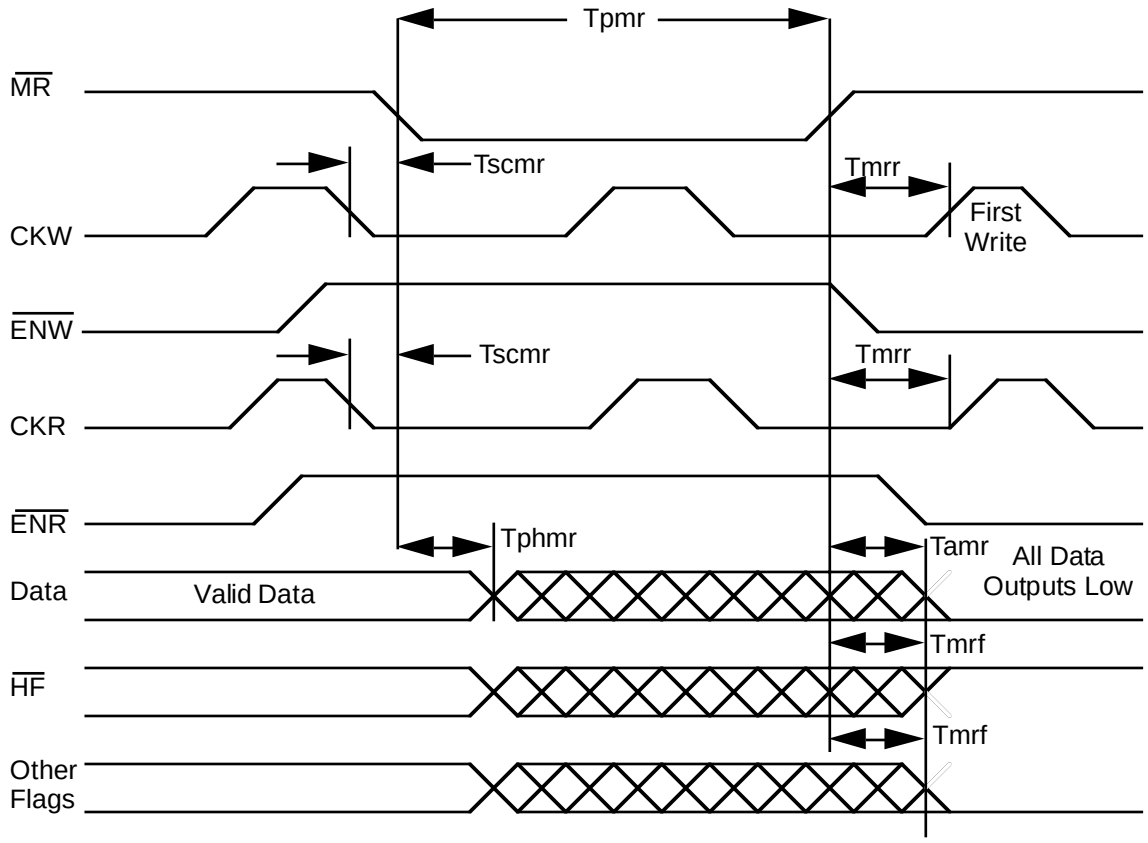


Figure 3. Master Reset Timing

NOTE: If $\overline{ENW}$ is held high during Master Reset, the parity is disabled.

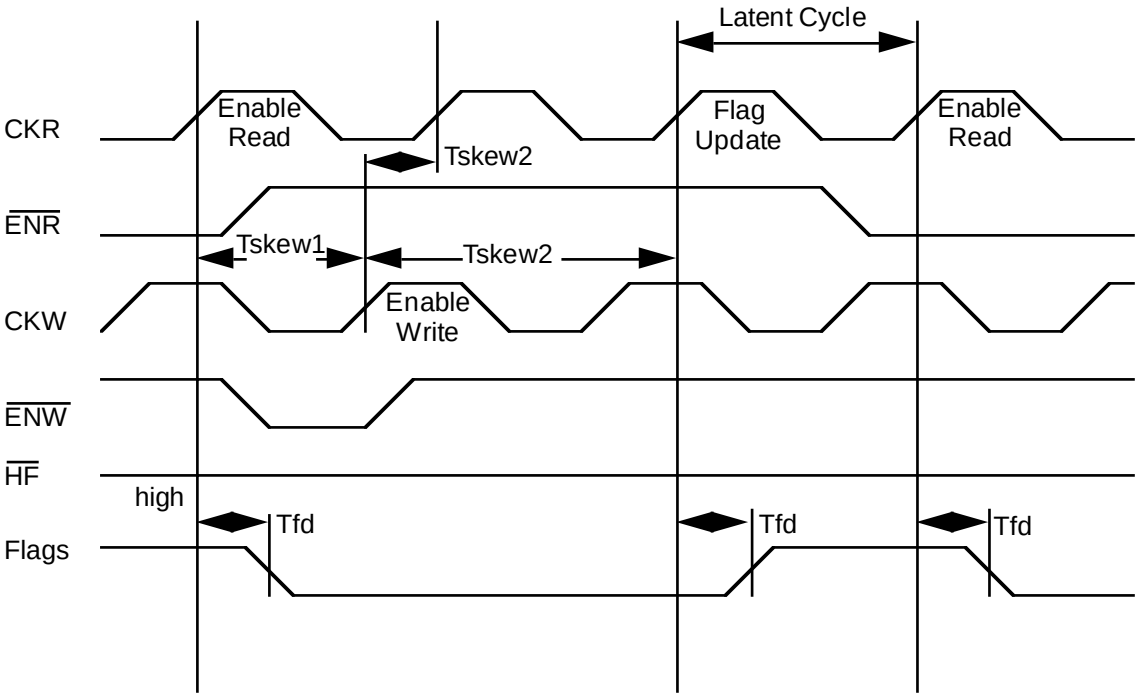


Figure 4. Read Flag Update Timing

NOTE: When an empty condition occors, the empty flag is set. The performance of another read requires at least one write, on read clock to reset the empty flag and then an enabled read clock.

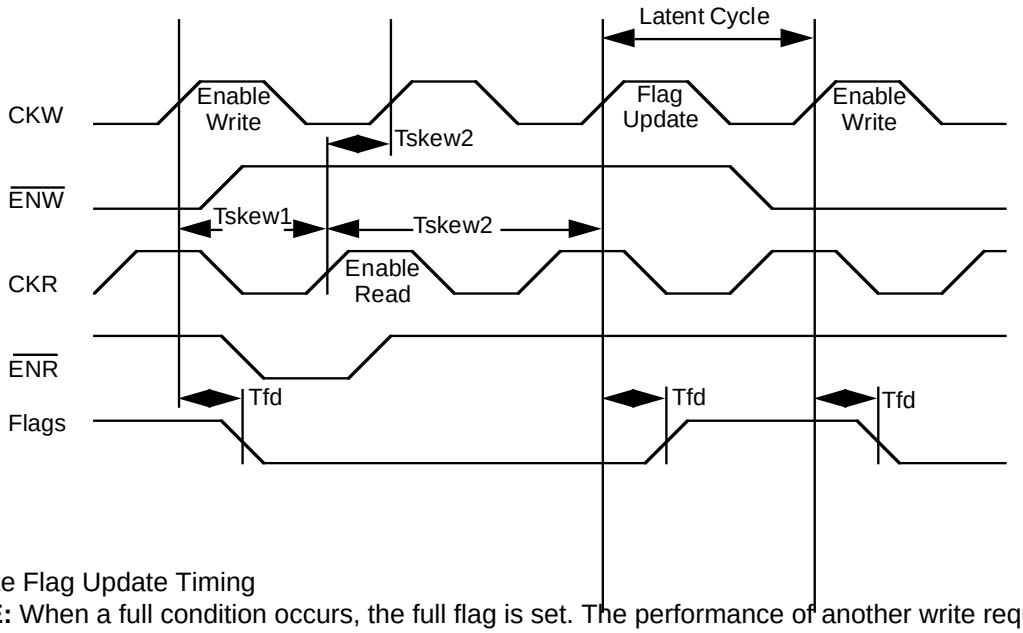


Figure 5. Write Flag Update Timing

NOTE: When a full condition occurs, the full flag is set. The performance of another write requires at least one read, one write clock to reset the full flag and then one enabled write clock.

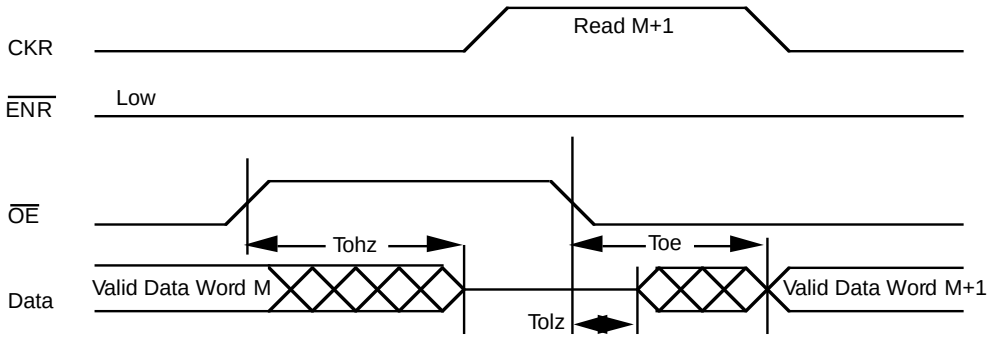


Figure 6. Output Enable Timing

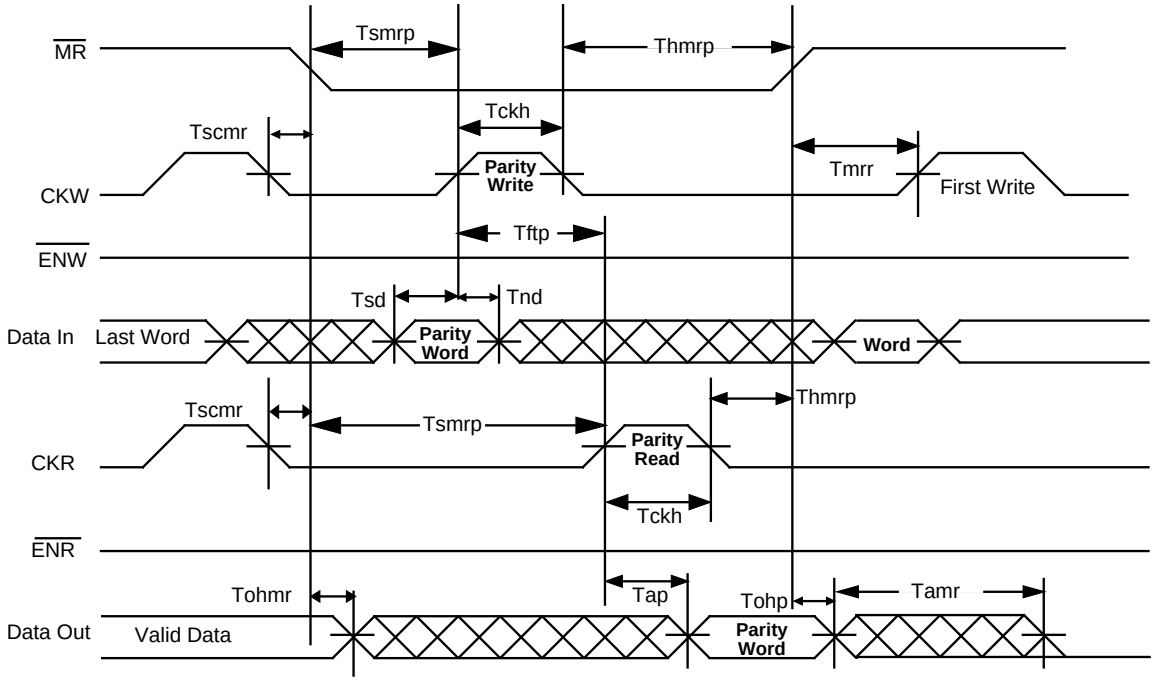
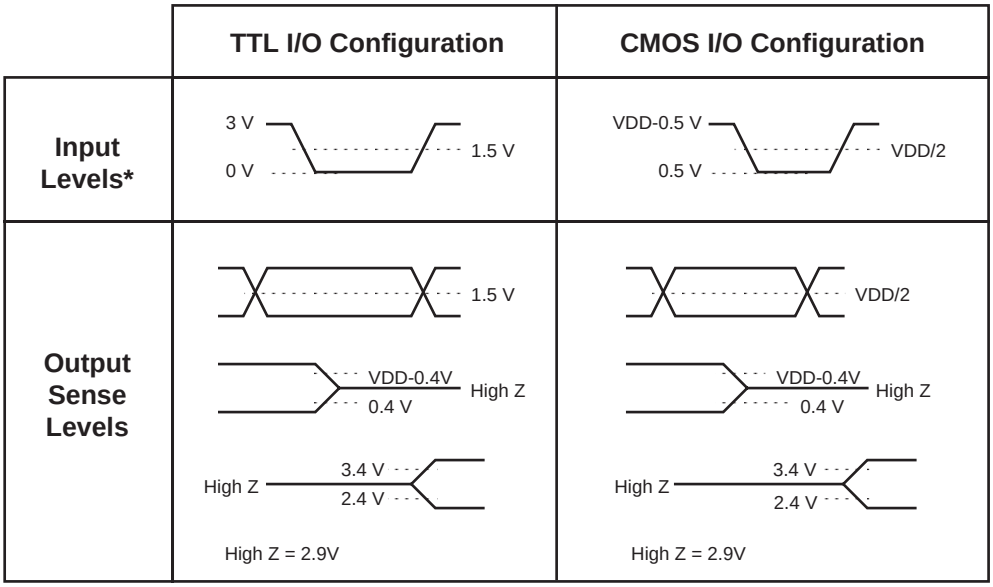


Figure 7. Parity Programming Mode

TESTER AC TIMING CHARACTERISTICS



* Input rise and fall times <1 ns/V

QUALITY AND RADIATION HARDNESS ASSURANCE

Honeywell maintains a high level of product integrity through process control, utilizing statistical process control, a complete “Total Quality Assurance System,” a computer data base process performance tracking system and a radiation hardness assurance strategy.

The radiation hardness assurance strategy starts with a technology that is resistant to the effects of radiation. Radiation hardness is assured on every wafer by irradiating test structures as well as SRAM product, and then monitoring key parameters which are sensitive to ionizing radiation. Conventional MIL-STD-883 TM 5005 Group E testing, which includes total dose exposure with Cobalt 60, may also be performed as required. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. “Engineering Devices” are available with limited performance and screening for breadboarding and/or evaluation testing. Hi-Rel Level B and S devices undergo additional screening per the requirements of MIL-STD-883. As a QML supplier, Honeywell also offers QML Class Q and V devices per MIL-PRF-38535 and are available per the applicable Standard Microcircuits Drawing (SMD). QML devices offer ease of procurement by eliminating the need to create detailed specifications and offer benefits of improved quality and cost savings through standardization.

RELIABILITY

Honeywell understands the stringent reliability requirements for space and defense systems and has extensive experience in reliability testing on programs of this nature. This experience is derived from comprehensive testing of VLSI processes. Reliability attributes of the RICMOS™ process were characterized by testing specially designed irradiated and non-irradiated test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure more reliable products.

In addition, the reliability of the RICMOS™ process and product in a military environment was monitored by testing irradiated and non-irradiated circuits in accelerated dynamic life test conditions. Packages are qualified for product use after undergoing Group B & D testing as outlined in MIL-STD-883, TM 5005, Class S. The product is qualified by following a screening and testing flow to meet the customer’s requirements. Quality conformance testing is performed as an option on all production lots to ensure the ongoing reliability of the product.

Pin List for HX6409

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	7	Q5	13	QT/TQF	19	ENR	25	D6	31	D0
2	Q0	8	Q6	14	HF	20	CKW	26	D5	32	VDD
3	Q1	9	Q7	15	EF	21	ENW	27	D4		
4	Q2	10	Q8	16	VSS	22	MR	28	D3		
5	Q3	11	OE	17	VDD	23	D8	29	D2		
6	Q4	12	EF_FAULT	18	CKR	24	D7	30	D1		

Pin List for HX6218

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CKR	13	D17	25	VSS	37	Q1	49	Q11	61	VSS
2	ENR	14	D16	26	D8	38	Q2	50	Q12	62	VDD
3	CKW	15	D15	27	D7	39	Q3	51	Q13	63	OE
4	ENW	16	D14	28	D6	40	Q4	52	VDD	64	EF_FAULT
5	MR	17	VDD	29	D5	41	Q5	53	VSS	65	QF/TQF
6	VDD	18	VSS	30	D4	42	Q6	54	Q14	66	HF
7	VSS	19	D13	31	D3	43	Q7	55	Q15	67	E?F
8	VSS	20	D12	32	D2	44	Q8	56	Q16	68	VDD
9	VSS	21	D11	33	D1	45	VSS	57	Q17		
10	VDD	22	D10	34	D0	46	VDD	58	VDD		
11	VDD	23	D9	35	VDD	47	Q9	59	VDD		
12	VDD	24	VDD	36	Q0	48	Q10	60	VDD		

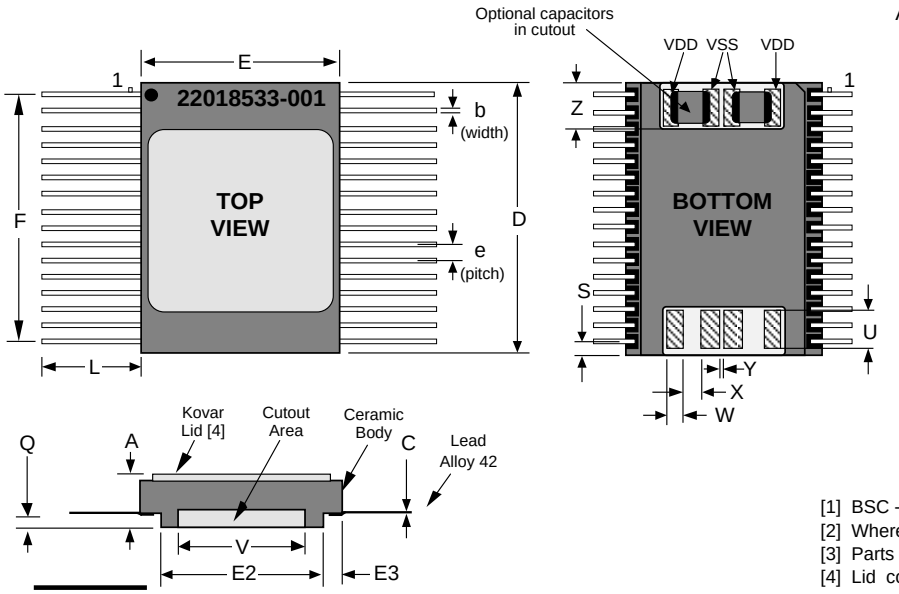
Pin List for HX6236

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	23	CKW	45	NC	67	VSS	89	Q2	111	Q19
2	NC	24	NC	46	D25	68	NC	90	NC	112	Q20
3	NC	25	ENW	47	NC	69	D8	91	Q3	113	NC
4	NC	26	NC	48	D24	70	D7	92	NC	114	Q21
5	OE	27	MR	49	VSS	71	D6	93	Q4	115	VDD
6	NC	28	NNC	50	VDD	72	NC	94	Q5	116	VSS
7	EF_FAULT	29	NC	51	D23	73	D5	95	Q6	117	Q22
8	QF/TQF	30	NC	52	D22	74	D4	96	Q7	118	Q23
9	HF	31	NC	53	D21	75	D3	97	Q8	119	Q24
10	NC	32	NC	54	D20	76	NC	98	NC	120	Q25
11	EF	33	VSS	55	D19	77	D2	99	VSS	121	Q26
12	NC	34	VDD	56	D18	78	NC	100	VDD	122	Q27
13	NC	35	D35	57	D17	79	D1	101	Q9	123	Q28
14	NC	36	D34	58	D16	80	NC	102	Q10	124	NC
15	NC	37	D33	59	D15	81	D0	103	Q11	125	Q29
16	VSS	38	D32	60	D14	82	VSS	104	Q12	126	Q30
17	VDD	39	D31	61	D13	83	VDD	105	Q13	127	Q31
18	NC	40	D30	62	D12	84	NC	106	Q14	128	Q32
19	CKR	41	D29	63	D11	85	Q0	107	Q15	129	Q33
20	NC	42	D28	64	D10	86	NC	108	Q16	130	Q34
21	ENR	43	D27	65	D9	87	Q1	109	Q17	131	Q35
22	NC	44	D26	66	VDD	88	NC	110	Q18	132	VDD

PACKAGING

The FIFO is offered in a 32-lead, 68-lead and a 132-lead flat pack, depending on the configuration. These packages are constructed of multilayer ceramic (Al_2O_3) and features internal power and ground planes. The flat packs also feature non-conductive ceramic tie bars. The tie bars allows electrical testing of the device, while preserving the lead integrity during shipping and handling, up to the point of lead forming and insertion.

PACKAGE DRAWING FOR 6409 (22018533-001)

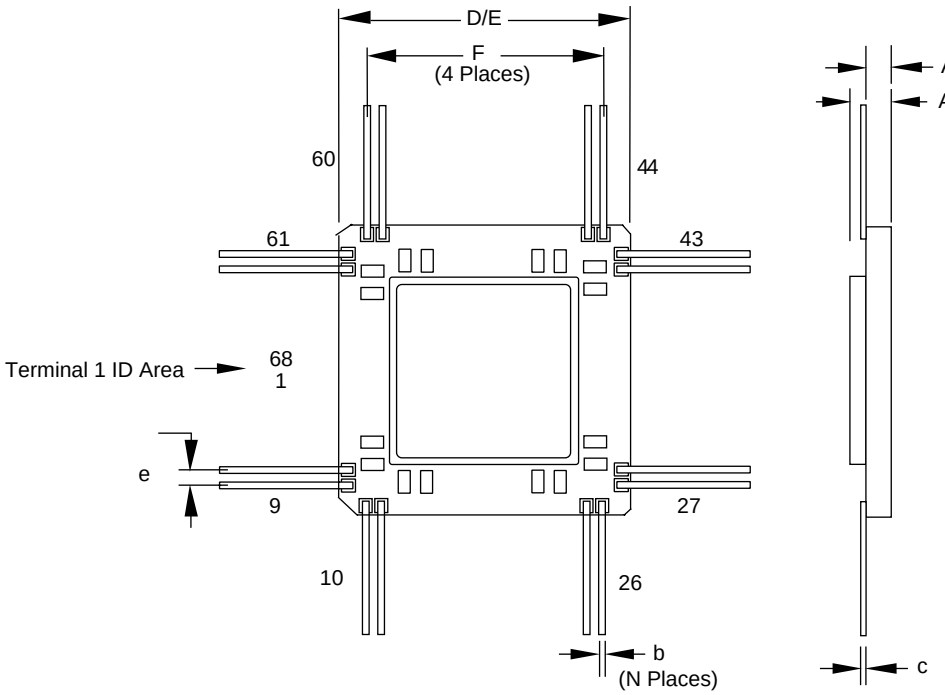


All dimensions in inches

A	0.135 ± 0.015
b	0.017 ± 0.002
C	0.004 to 0.009
D	0.820 ± 0.008
e	0.050 ± 0.005 [1]
E	0.600 ± 0.008
E2	0.500 ± 0.008
E3	0.040 ref
F	0.750 ± 0.005 [2]
L	0.295 min [3]
Q	0.026 to 0.045
S	0.035 ± 0.010
U	0.080 ref
V	0.380 ref
W	0.050 ref
X	0.075 ref
Y	0.010 ref
Z	0.135 ref

[1] BSC - Basic lead spacing between centers
[2] Where lead is brazed to package
[3] Parts delivered with leads unformed
[4] Lid connected to VSS

PACKAGE DRAWING FOR 6218 (22019075-001)

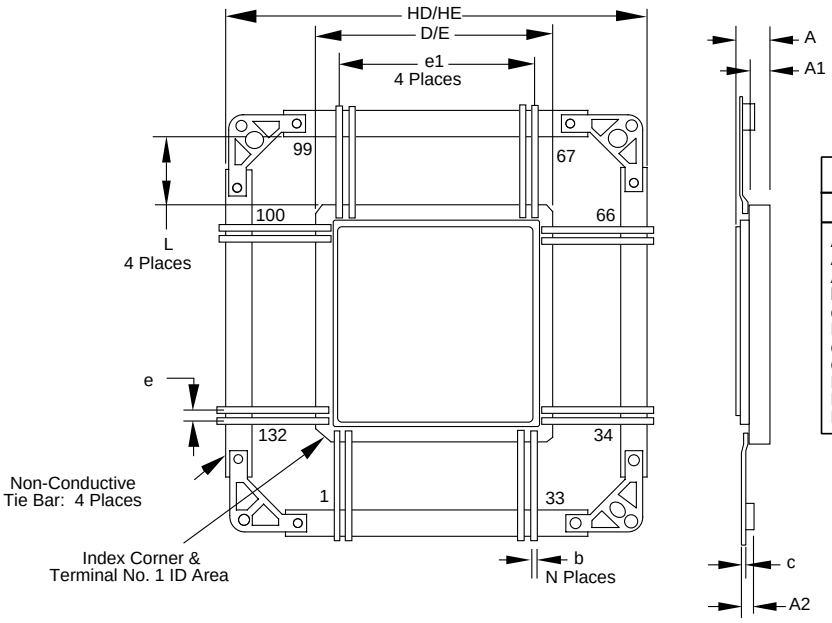


All dimensions in inches

A	0.092 ± 0.010
A1	0.080 ± 0.008
b	0.018 ± 0.002
c	0.010 ± 0.002
D/E	0.950 ± 0.015
e	0.050 ± 0.005 (1)
F	0.800 ± 0.008 (1)
N	68 ref.

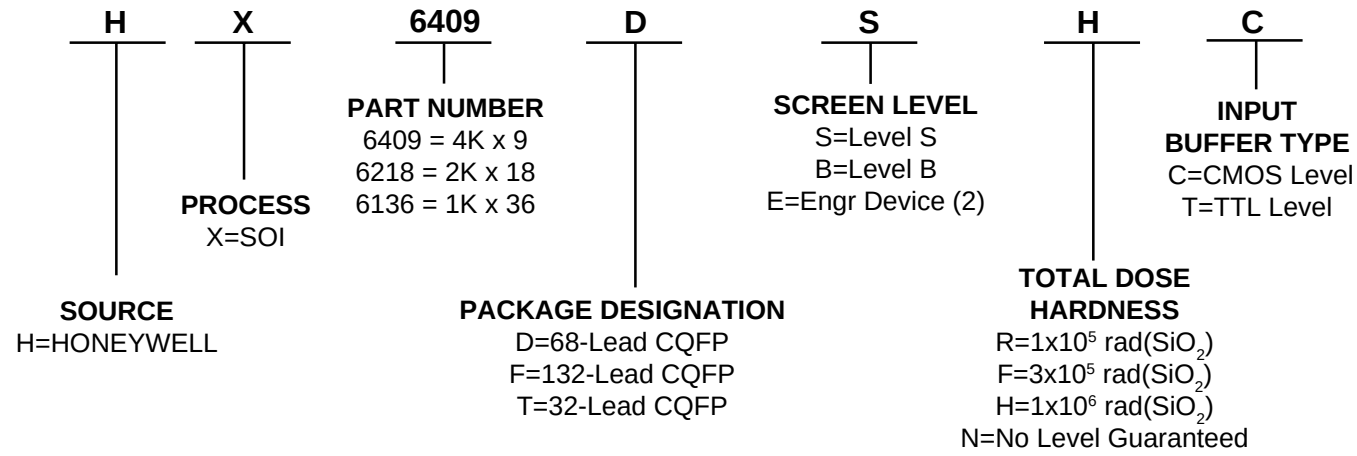
(1) BSC – Basic lead spacing between centers

PACKAGE DRAWING FOR 6136 (22018696-001)



Dimensions in inches	min	max
A	0.091	0.109
A1	0.057	0.063
A2	0.036	0.047
b	0.005	0.009
c	0.004	0.008
D/E	0.942	0.958
e	0.025 BSC	
e1	.800 BSC	
HD/HE	2.485	
L	0.575	2.505
N	132	Ref.

ORDERING INFORMATION (1)



(1) Orders may be faxed to 612-954-2051. Please contact our Customer Service Department at 612-954-2888 for further information.
(2) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, no radiation guaranteed.
Contact Factory with other needs.

To learn more about Honeywell Solid State Electronics Center,
visit our web site at http://www.ssec.honeywell.com