

DESCRIPTION

The HY5116100A is the new generation and fast dynamic RAM organized 16,777,216 x 1-bit. The HY5116100A utilizes Hyundai's CMOS silicon gate process technology as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5116100A to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of $5V \pm 10\%$ tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**

Max. battery back-up 3.3mW (L-part)

Max. CMOS standby 2.2mW (L-part)
5.5mW

Max. TTL standby 11.0mW

Max. operating

Speed	Power
50	605mW
60	495mW
70	440mW

- Single power supply of $5V \pm 10\%$
- TTL compatible inputs and outputs
- Fast access and cycle time

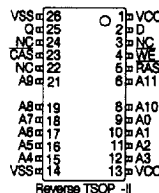
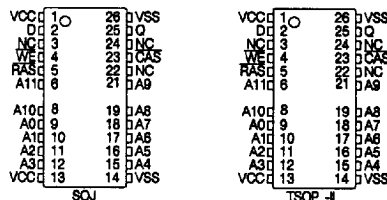
Speed	tRAC	tCAC	tPC
50	50ns	13ns	35ns
60	60ns	15ns	40ns
70	70ns	18ns	45ns

- Fast page mode operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh capability
- 4096 refresh cycles / 256ms (SL-part)
4096 refresh cycles / 64ms

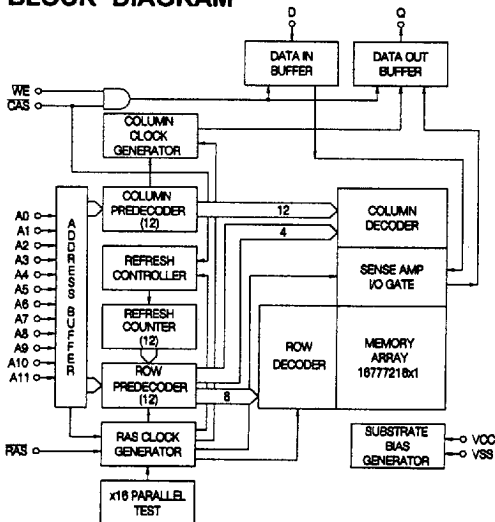
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A11	Address input
D	Data Input
Q	Data Output
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE: All Voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	$V_{SS} \leq V_{IN} \leq V_{CC}+1.0$, All other pins not under test = V_{SS}		-10	10	mA	
ILO	Output Leakage Current (High impedance State)	$V_{SS} \leq V_{OUT} \leq V_{CC}$ RAS & CAS at V_{IH}		-10	10	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	50 60 70	- - -	110 90 80	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at $V_{IH}(\text{min.})$, other inputs $\geq V_{SS}$		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	50 60 70	- - -	110 90 80	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	50 60 70	- - -	80 70 60	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS $\geq V_{CC}-0.2V$	SL-part	- -	1 0.4	mA	5
ICC6	VCC Supply Current, CAS-before- RAS refresh	trc = trc (min.)	50 60 70	- - -	110 90 80	mA	1,3
ICC7	VCC Supply Current, Battery Back up (SL-part only)	trc = 62.5μs, CAS = CBR cycling or 0.2V, WE = $V_{CC}-0.2V$, A0-A11= $V_{CC}-0.2V$ or 0.2V D= $V_{CC}-0.2V, 0.2V$, or open Q=open	trc $\leq$ 300ns trc $\leq$ 1μs	- -	350 600	μA	1,4,5
ICC8	VCC Supply Current, Self Refresh (SL-part only)	RAS & CAS $\leq 0.2V$ OE & WE & A0-A11= $V_{CC}-0.2V$ or 0.2V, D= $V_{CC}-0.2V, 0.2V$ or open, Q=open			300	μA	5
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5.0mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rates.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{\text{RAS}}=V_{IL}$ and $\overline{\text{CAS}}=V_{IH}$.
4. trc(max.)=1μs is only applied to refresh of battery backup but trc(max.)=10μs is applied to normal functional operation .
5. ICC5(max.) =0.4mA and ICC7 are applied to SL-parts only(HY5116100ASLJ, HY5116100ASLT and HY5116100ASLR).

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AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY5116100AJ/T/R/SLJ/SLT/SLR						UNIT	NOTE	
			- 50		- 60		- 70				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns		
2	tRWC	Read-Modify-Write Cycle Time	110	-	130	-	155	-	ns		
3	tPC	Fast Page Mode cycle Time	35	-	40	-	45	-	ns		
4	tPRWC	Fast Page Mode Read-Modify-Write cycle Time	55	-	60	-	70	-	ns		
5	tRAC	Access Time form $\overline{\text{RAS}}$	-	50	-	60	-	70	ns	4,9,10	
6	tCAC	Access Time from $\overline{\text{CAS}}$	-	13	-	15	-	18	ns	4,9	
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10	
8	tCPA	Access Time from $\overline{\text{CAS}}$ Precharge	-	30	-	35	-	40	ns	4	
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4	
10	tOFF	Output Buffer Turn-off Delay	0	10	0	13	0	15	ns	5	
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3	
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns		
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns		
14	tRASP	RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns		
15	tRSH	RAS Hold Time	13	-	15	-	18	-	ns		
16	tCSH	CAS Hold Time	50	-	60	-	70	-	ns		
17	tCAS	CAS Pulse width	13	10K	15	10K	18	10K	ns		
18	tRCD	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	13	37	20	45	20	52	ns	9	
19	tRAD	$\overline{\text{RAS}}$ to Column Address Delay Time	13	25	15	30	15	35	ns	10	
20	tCRP	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	-	5	-	5	-	ns		
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns		
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns		
23	tRAH	Row Address Hold time	10	-	10	-	10	-	ns		
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns		
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns		
26	tAR	Column Address Hold Time from $\overline{\text{RAS}}$	45	-	50	-	55	-	ns		
27	tRAL	Column Address to $\overline{\text{RAS}}$ Lead Time	25	-	30	-	35	-	ns		
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns		
29	tRCH	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	6	
30	tRRH	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	6	
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns		
32	tWCR	Write Command Hold Time from $\overline{\text{RAS}}$	50	-	55	-	60	-	ns		
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns		
34	tRWL	Write Command to $\overline{\text{RAS}}$ Lead Time	13	-	15	-	18	-	ns		
35	tCWL	Write Command to $\overline{\text{CAS}}$ Lead Time	13	-	15	-	18	-	ns		
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7	
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7	
38	tDHR	Data-In Hold Time Referenced to $\overline{\text{RAS}}$	50	-	55	-	60	-	ns		
39	tREF	Refresh Period (2048 cycles)	SL-part	-	64	-	64	-	64	ms	12
				-	256	-	256	-	256		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8	

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5116100AJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			- 50		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	13	-	15	-	18	-	ns	8
42	tRWD	RAS to WE Delay Time	50	-	60	-	70	-	ns	8
43	tAWD	Column Address to WE Delay Time	25	-	30	-	35	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	15	-	15	-	ns	
46	tRPC	RAS to CAS Precharge Time	0	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	
48	tCPWD	WE Delay Time from CAS Precharge	30	-	35	-	40	-	ns	
49	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	ns	8
50	tWRP	WE to RAS Precharge Time(CBR Cycle)	10	-	10	-	10	-	ns	
51	tWRH	WE to RAS Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
52	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
53	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
54	tRASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	ms	
55	tRPS	RAS Precharge Time (Self Refresh)	120	-	130	-	150	-	ns	
56	tCHS	CAS Hold Time (Self Refresh)	- 50	-	- 50	-	- 50	-	ns	

AC CHARACTERISTICS IN TEST MODE

NOTE 13

#	SYMBOL	PARAMETER	HY5116100AJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			- 50		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	115	-	135	-	160	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	60	-	65	-	75	-	ns	
5	tRAC	Access Time from RAS	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	20	-	23	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
13	tRAS	RAS Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	RAS Hold Time	18	-	20	-	23	-	ns	
16	tCSH	CAS Hold Time	55	-	65	-	75	-	ns	
17	tCAS	CAS Pulse Width	18	10K	20	10K	25	10K	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
41	tCWD	CAS to WE Delay Time	18	-	20	-	23	-	ns	8
42	tRWD	RAS to WE Delay Time	55	-	65	-	75	-	ns	8
43	tAWD	Column Address to WE Delay Time	30	-	35	-	40	-	ns	8

NOTE:

1. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle before proper device operation is achieved.
2. If $\overline{\text{RAS}}=\text{V}_{\text{SS}}$ during power-up, the device could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. $\text{V}_{\text{IH}}(\text{min.})$ and $\text{V}_{\text{IL}}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $\text{V}_{\text{IH}}(\text{min.})$ and $\text{V}_{\text{IL}}(\text{max.})$, and are assumed to be 5ns for all inputs.
4. Measured at $\text{V}_{\text{OH}}=2.4\text{V}$ and $\text{V}_{\text{OL}}=0.4\text{V}$ with a load equivalent to 2 TTL loads and 100pF.
5. $\text{t}_{\text{OFF}}(\text{max.})$ and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tr_{CH} or tr_{RH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. tw_{CS} , tr_{WD} , tc_{WD} , t_{AWD} and tc_{PWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{tw}_{\text{CS}} \geq \text{tw}_{\text{CS}}(\text{min.})$, the cycle is an early write cycle and data out put will remain open circuit (high impedance) through the entire cycle. If $\text{tr}_{\text{WD}} \geq \text{tr}_{\text{WD}}(\text{min.})$, $\text{tc}_{\text{WD}} \geq \text{tc}_{\text{WD}}(\text{min.})$, $\text{t}_{\text{AWD}} \geq \text{t}_{\text{AWD}}(\text{min.})$, and $\text{tc}_{\text{PWD}} \geq \text{tc}_{\text{PWD}}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indetermined.
9. Operation within the $\text{tr}_{\text{CD}}(\text{max.})$ limit insures that $\text{tr}_{\text{AC}}(\text{max.})$ can be met. $\text{tr}_{\text{CD}}(\text{max.})$ is specified as a reference point only. If tr_{CD} is greater than the specified $\text{tr}_{\text{CD}}(\text{max.})$ limit, then access time is controlled by tc_{AC} .
10. Operation within the $\text{tr}_{\text{AD}}(\text{max.})$ limit insures that $\text{tr}_{\text{AC}}(\text{max.})$ can be met. $\text{tr}_{\text{AD}}(\text{max.})$ is specified as a reference point only. If tr_{AD} is greater than the specified $\text{tr}_{\text{AD}}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $\text{t}_{\text{REF}}(\text{max.})=256\text{ms}$ is applied to SL-Parts(HY5116100ASLJ, HY5116100ASLT and HY5116100ASLR).
12. A burst of 4096 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 64ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the Test Mode.

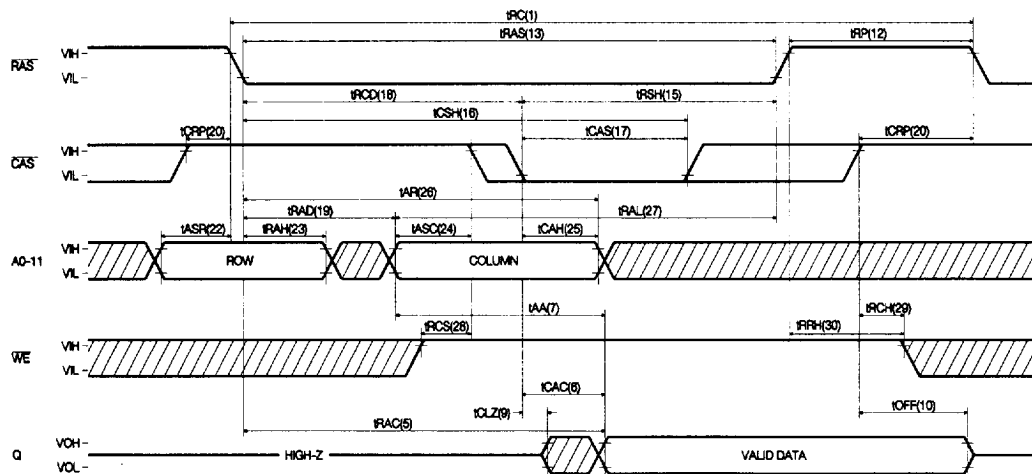
CAPACITANCE

($\text{T}_{\text{A}}=25^{\circ}\text{C}$, $\text{V}_{\text{CC}}=5\text{V} \pm 10\%$, $\text{V}_{\text{SS}}=0\text{V}$, $\text{f}=1\text{MHZ}$, unless otherwise noted.)

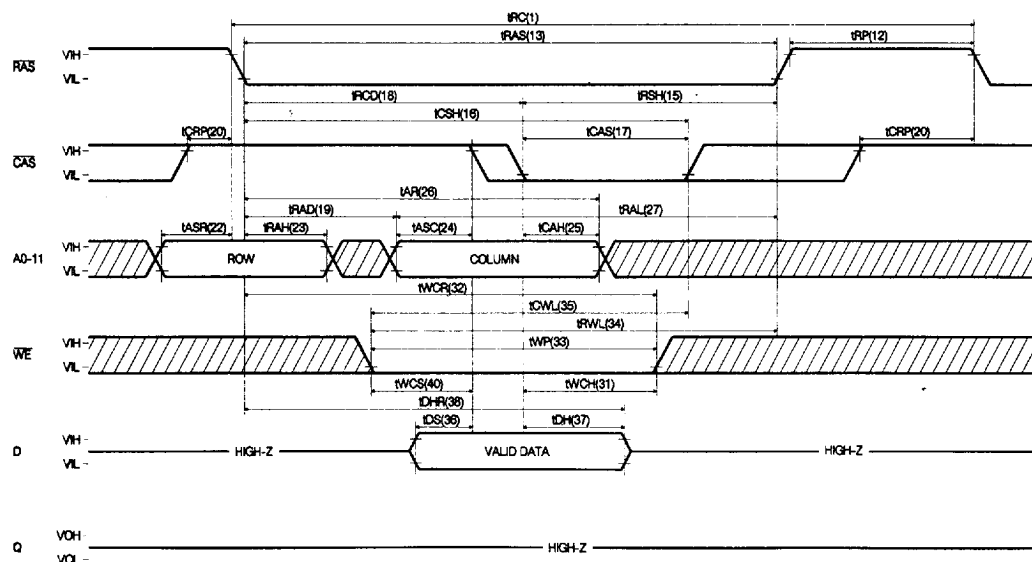
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A11, D)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	-	7	pF
C_{DQ}	Data Input/Output Capacitance (Q)	-	7	pF

TIMING DIAGRAM

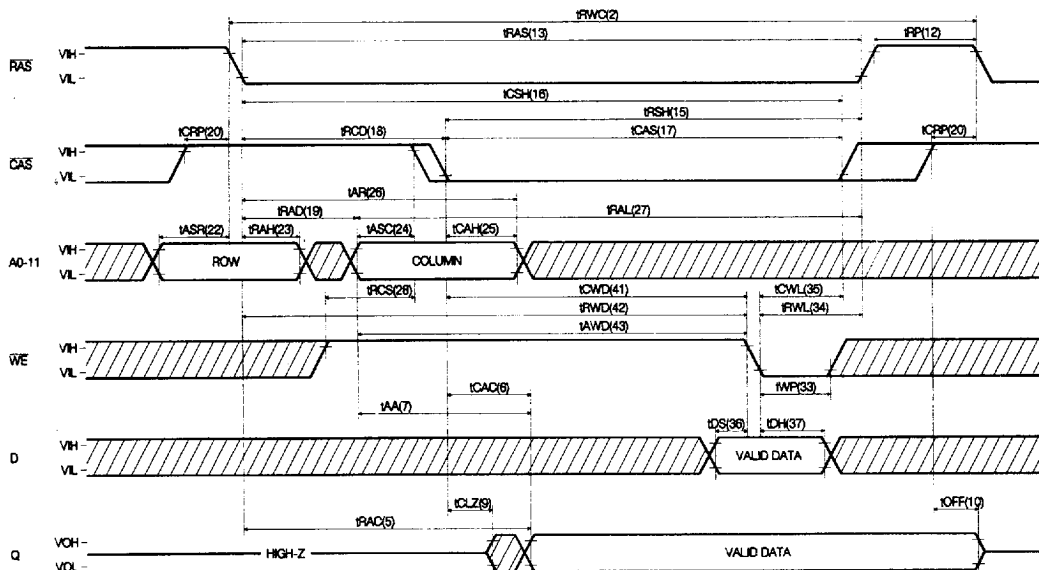
READ CYCLE



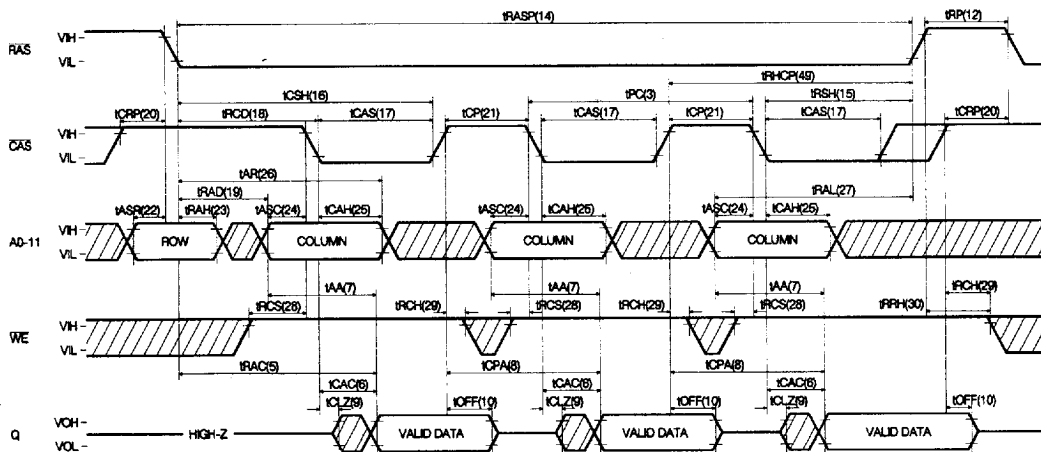
EARLY WRITE CYCLE



READ-MODIFY-WRITE CYCLE



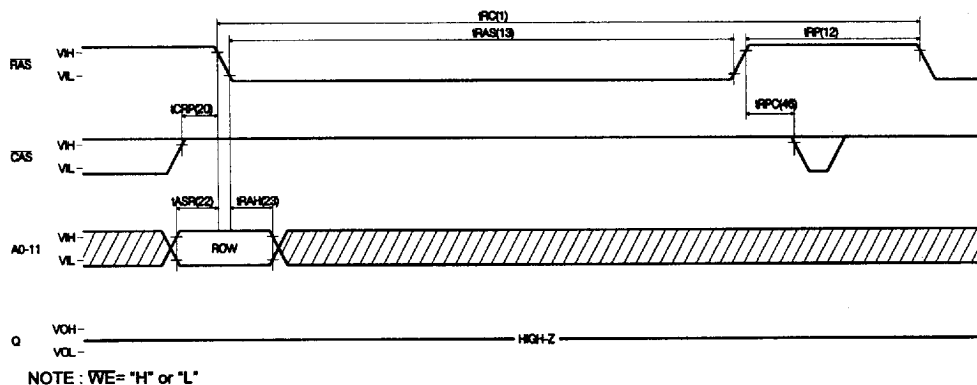
FAST PAGE MODE READ CYCLE



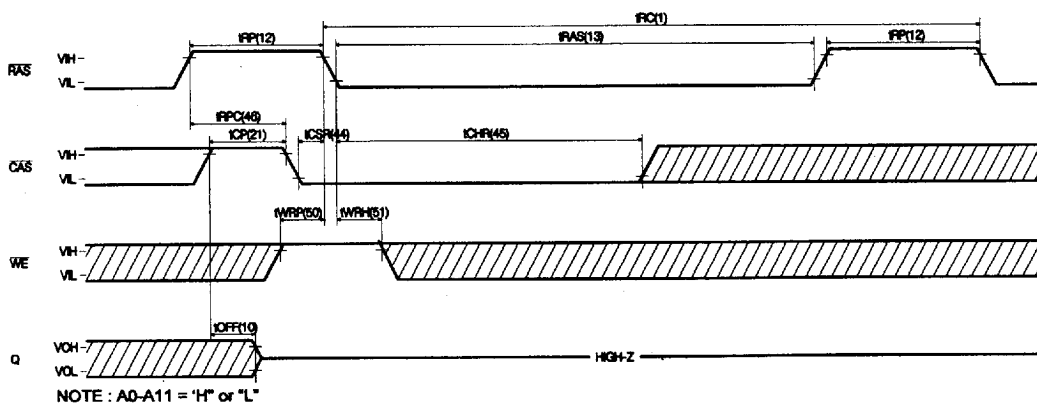
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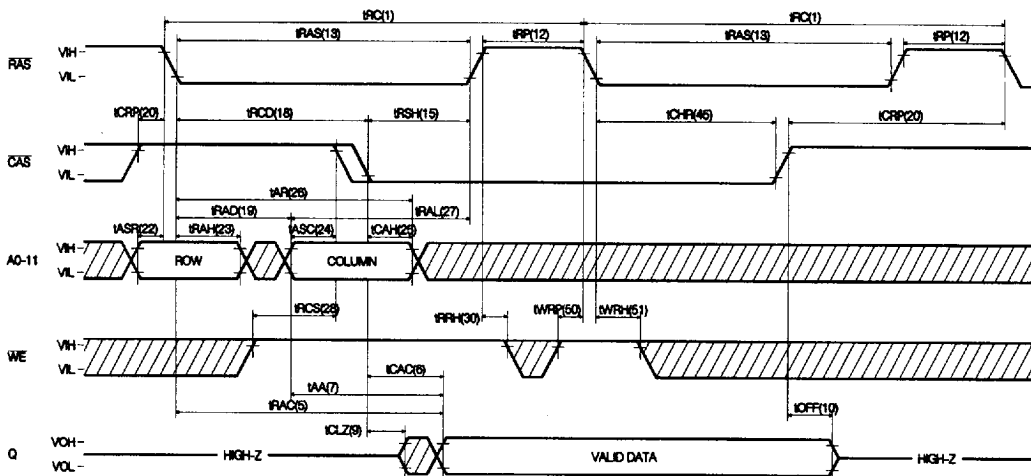
RAS-ONLY REFRESH CYCLE



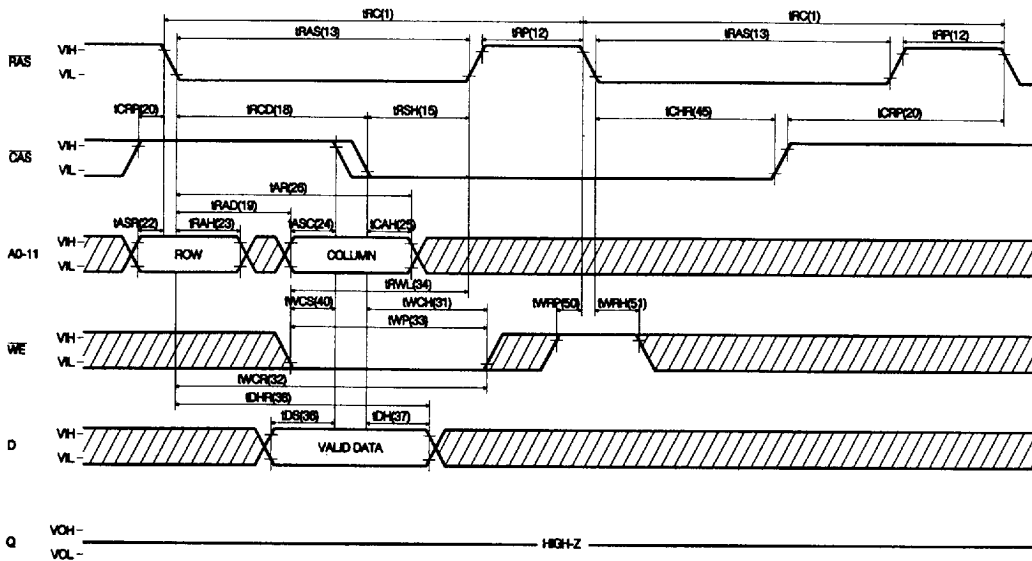
CAS-BEFORE-RAS REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

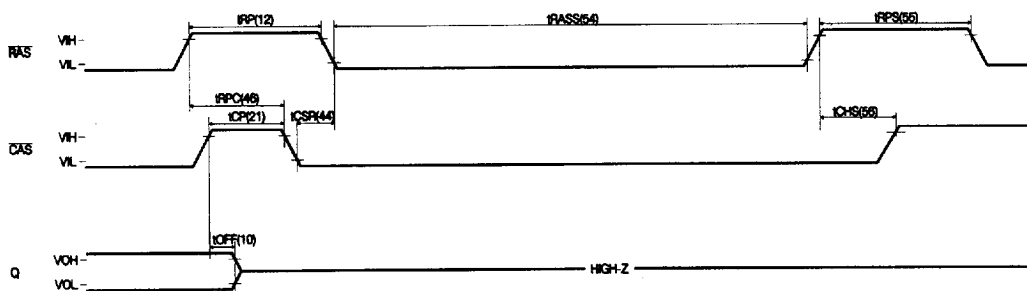


HIDDEN REFRESH CYCLE (WRITE)

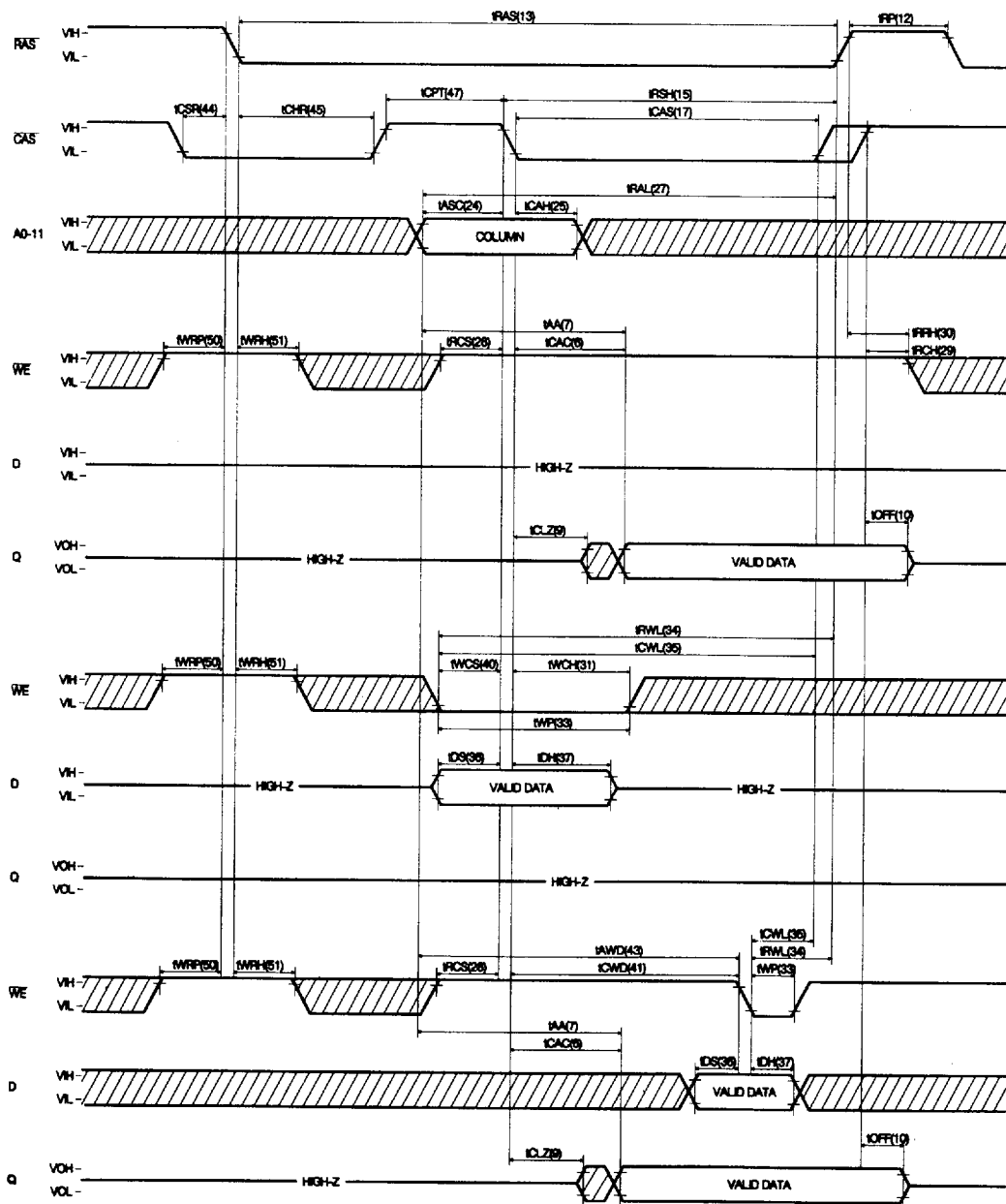


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CAS-BEFORE-RAS SELF REFRESH CYCLE



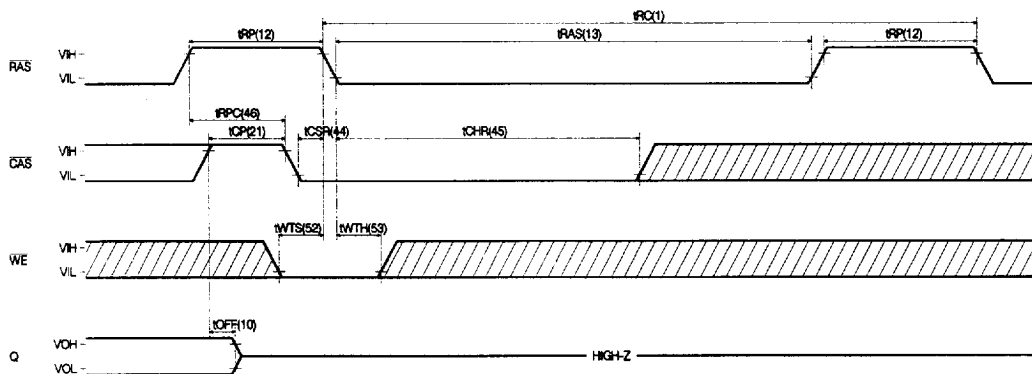
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TEST MODE

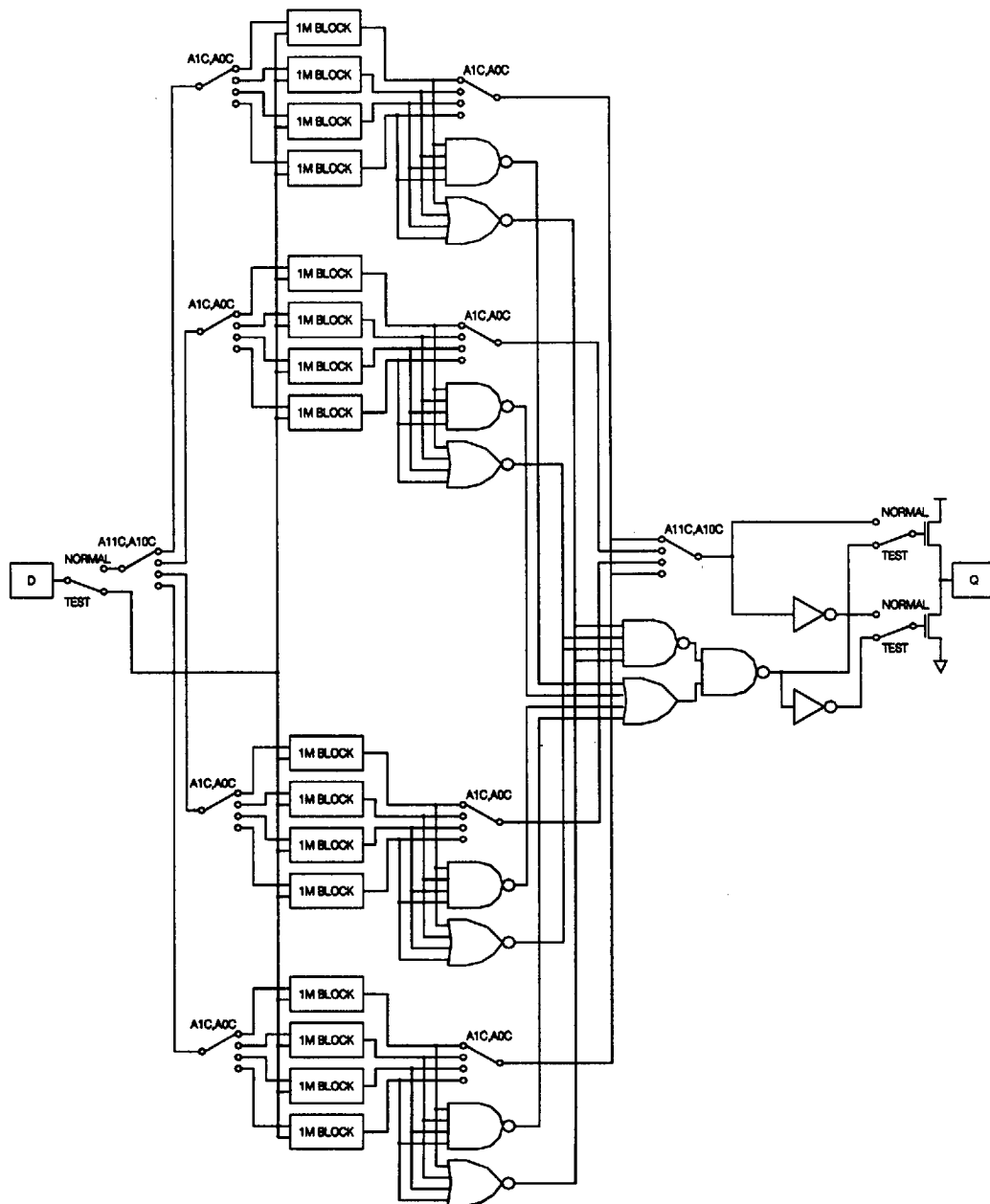
The HY5116100A is a DRAM organized 16,777,216 x 1-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0, A1, A10 and A11 are not used. If upon reading, all bits are equal (all "1"s or "0"s), the Q pin indicates a "1". If they are not equal, the Q pin indicates a "0". Belowing shows the timing diagram of the HY5116100A to enter Test Mode. In Test Mode, the 16M x 1DRAM can be tested as if it were a 1M x 1DRAM. WE, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY5116100A into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/16 in case of N test pattern).

TEST MODE IN CYCLE



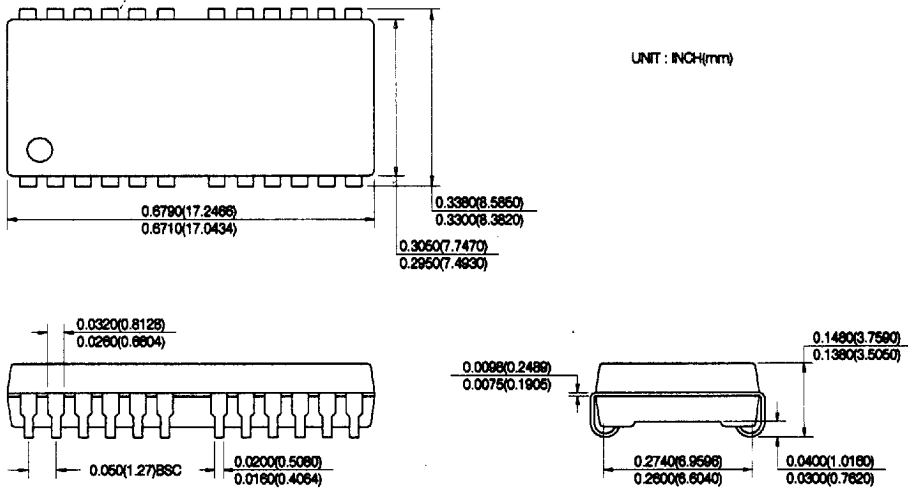
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BLOCK DIAGRAM IN TEST MODE

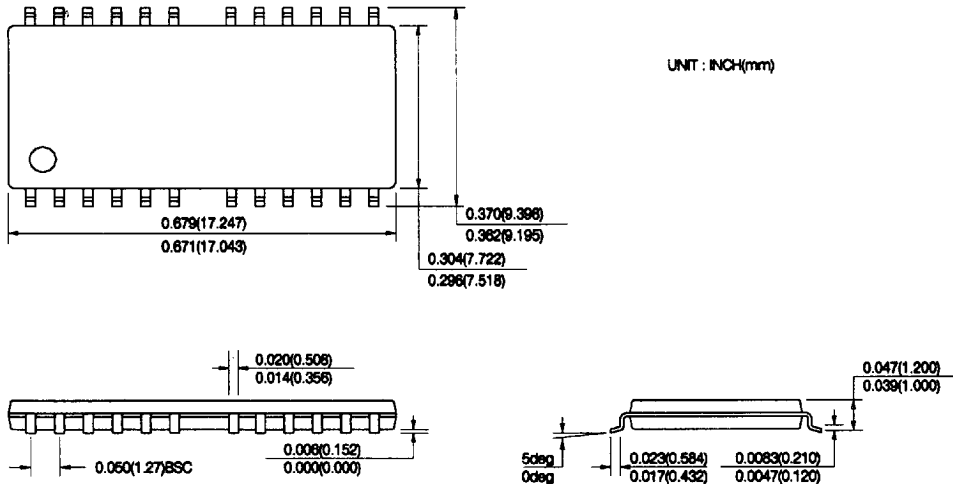


PACKAGE INFORMATION

300 mil 24/28 pin Small Outline J-form Package (J)



300 mil 24/28 pin Thin Small Outline Package (T) (R)



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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY5116100AJ	50/60/70		SOJ
HY5116100ASLJ	50/60/70	SL-part	SOJ
HY5116100AT	50/60/70		TSOP-II
HY5116100ASLT	50/60/70	SL-part	TSOP-II
HY5116100AR	50/60/70		TSOP-II(R)
HY5116100ASLR	50/60/70	SL-part	TSOP-II(R)