HY5116800 Series

2M x 8-bit CMOS DRAM

DESCRIPTION

The HY5116800 is the new generation and fast dynamic RAM organized 2,097,152 x 8-bit. The HY5116800 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5116800 to be packaged in standard 28/28 pin plastic SOJ, TSOP-II and Reverse TSOP-II.
The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V±10% tolerence and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. battery back-up 3.3mW (SL-part)
  Max. CMOS standby 2.2mW (SL-part)
  5.5mW
  Max. TTL standby 11.0mW
  Max. operating

Speed	Power
70	715mW
80	660mW
100	605mW

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access Time**

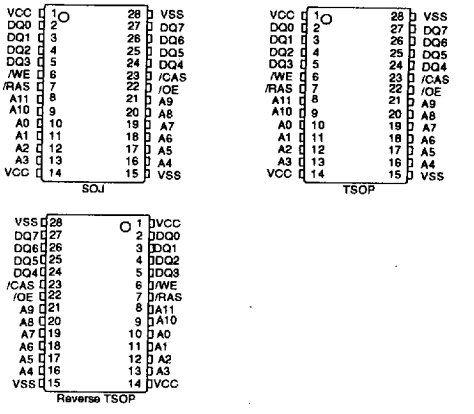
Speed	tRAC	tCAC	tPC
70	70ns	20ns	45ns
80	80ns	20ns	50ns
100	100ns	25ns	60ns

- **Fast page mode operation**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self Refresh**
- **4096 refresh cycles / 256ms (SL-part)**
  4096 refresh cycles / 64ms

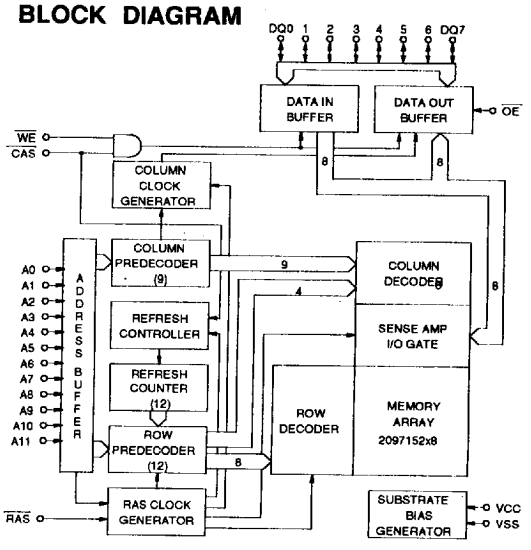
PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A11	Address Input
DQ0-DQ7	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	0.70	W
T_{SOLDER}	Soldering Temperature•Time	260•10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le V_{CC}$+1.0 All other pins not under test=V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}=t_{RC} (min.)	70 80 100	- - -	100 90 80	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs ≥ V_{SS}		-	2	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}=t_{RC} (min.)	70 80 100	- - -	100 90 80	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	t_{PC}=t_{PC} (min.)	70 80 100	- - -	100 90 80	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$≥V_{CC}- 0.2V	 SL-part	- -	1 0.4	mA	 5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}=t_{RC} (min.)	70 80 100	- - -	100 90 80	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (SL-Part only)	t_{RC}=62.5µs, $\overline{CAS}$=CBR cycling or 0.2V, $\overline{WE}$=V_{CC} - 0.2V, A0-A11=V_{CC} - 0.2V or 0.2V, DQ0-DQ7=V_{CC} - 0.2V, 0.2V or open	t_{RAS} ≤ 300ns	-	450	µA	1,4,5
			t_{RAS}≤ 1µs	-	600		
I_{CC8}	V_{CC} Supply Current, Self Refresh (SL-Part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V other pins same as I_{CC7}			500	µA	5
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=–5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Icc is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.
4. t_{RAS}(max.)=1µs is only applied to refresh of battery backup but t_{RAS}(max.)=10µs is applied to normal functional operating.
5. I_{CC5}(max.)=0.4mA and I_{CC7} and I_{CC8} are applied to SL-part only (HY5116800SLJC, HY5116800SLTC and HY51161800SLRC).

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V±10%, V_{SS} = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY5116800JC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-70		-80		-100			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	60	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	125	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	-	50	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	55	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100K	80	100K	100	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	10	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	15	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	20	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	55	-	60		75	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	20	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	55	-	60	-	75	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
39	tREF	Refresh Period (4096 cycles)	-	64	-	64	-	64	ms	12
		SL-part	-	256	-	256	-	256		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5116160JC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-70		-80		-100			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	-	50	-	60	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	-	110	-	135	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	65	-	70	-	85	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	15	-	15	-	20	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	40	-	40	-	50	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	20	-	20	-	20	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	20	-	20	-	25	ns	
50	tOED	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time	0	15	0	15	0	15	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	20	-	20	-	25	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	70	-	75	-	90	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	-	45	-	55	-	ns	
55	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	µs	
56	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	130	-	150	-	180	-	ns	
57	tCHS	$\overline{CAS}$ Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required.
2. If $\overline{RAS}$= Vss during power-up,the HY5116800 could begin an active cycle.This conditoin results in higher current than necessary current which is demanded from the power supply during power-up.It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at valid V_{IH} in order to minimize the power-up current.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals.Transition times are measured between V_{IH}(min.) and V_{IL}(max.),and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}=2.4V and V_{OL}=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.)=256ms is applied to SL-parts only (HY5116800SLJC, HY5116800SLTC and HY5116800SLRC).
12. A burst of 4096 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 64ms (256ms for SL-part) after exiting self refresh.

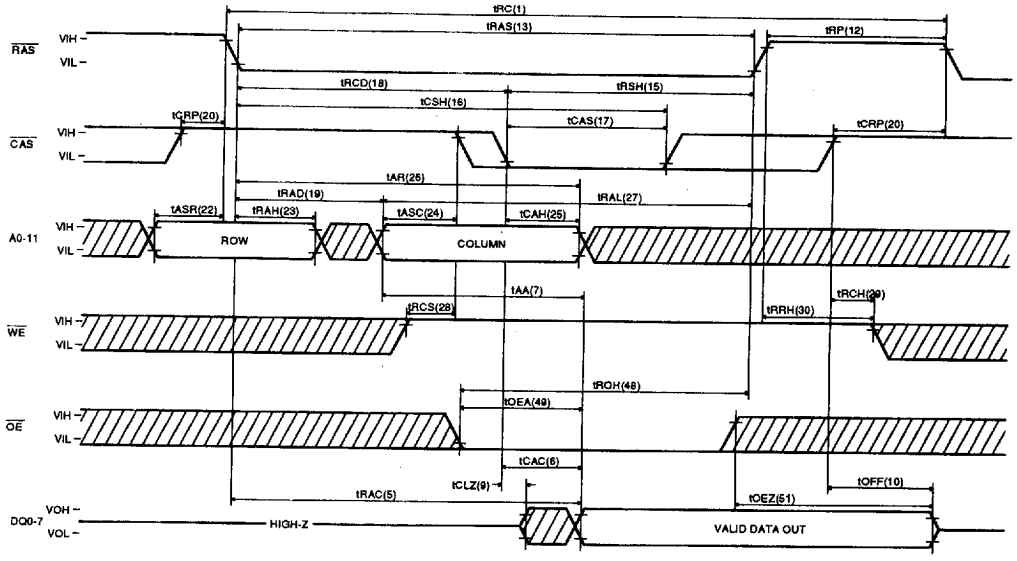
CAPACITANCE

(T_A=25°C, V_{CC}= 5V ±10%, V_{SS}=0V, f=1MHz, unless otherwise noted.)

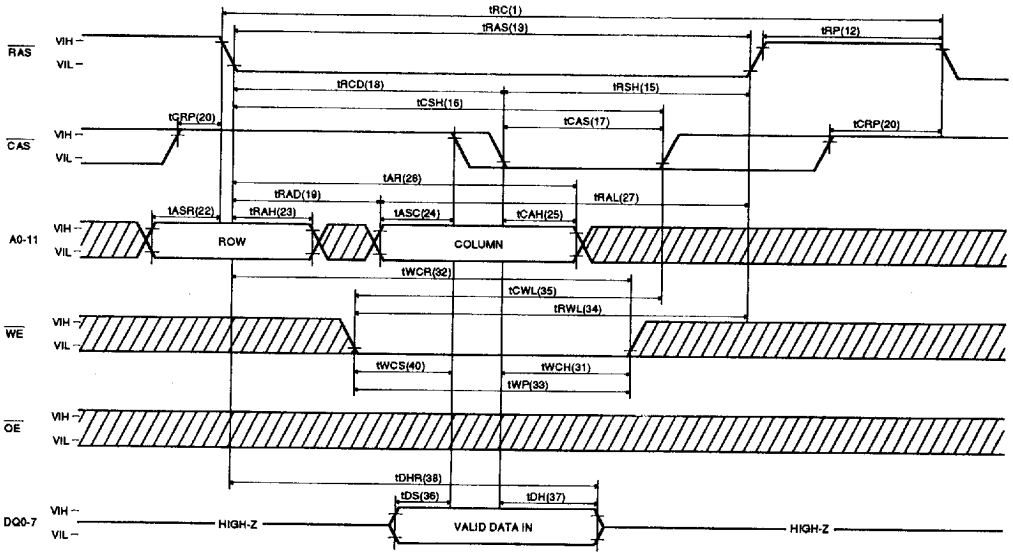
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A11)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	-	7	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ7)	-	7	pF

TIMING DIAGRAM

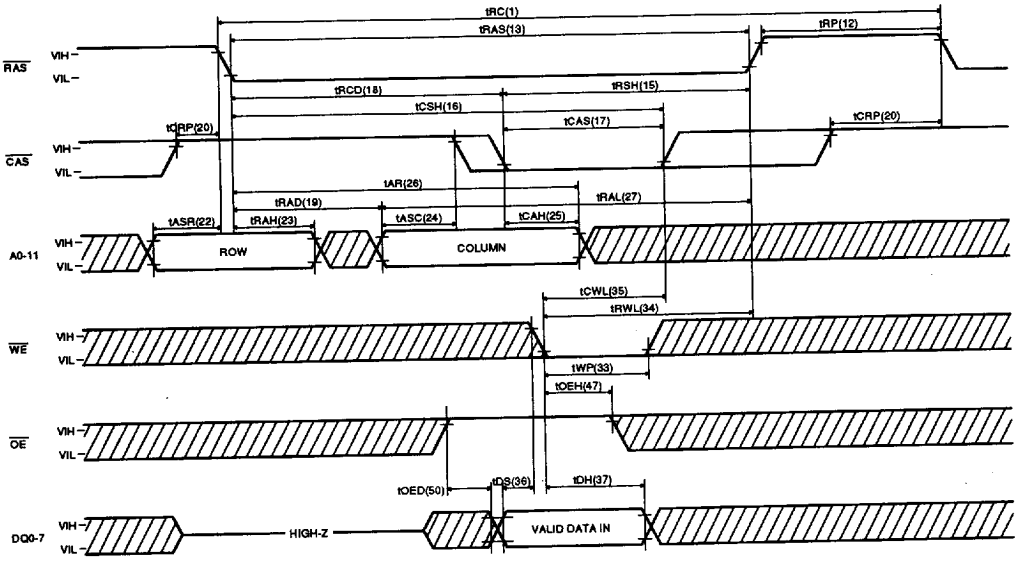
READ CYCLE



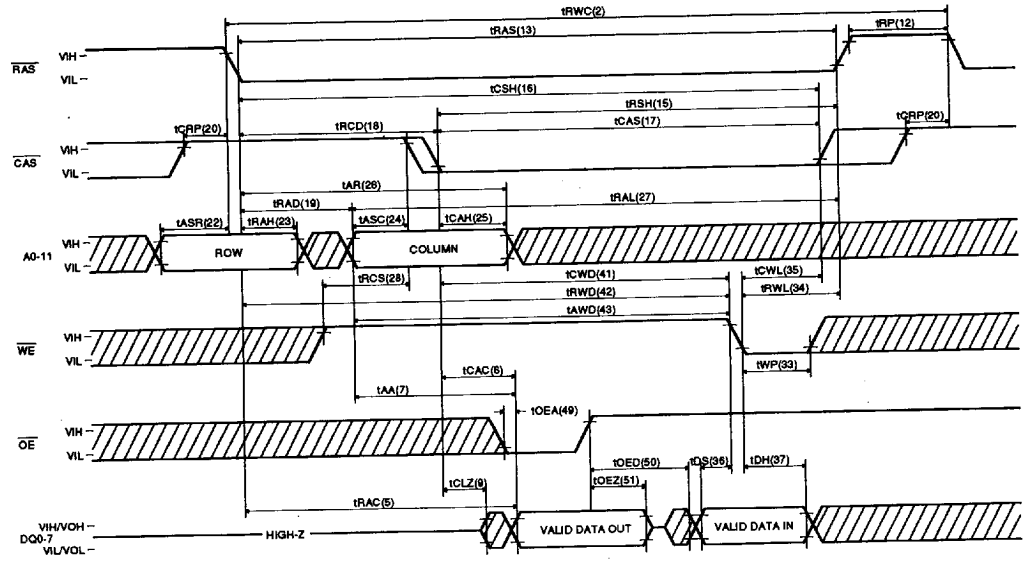
EARLY WRITE CYCLE



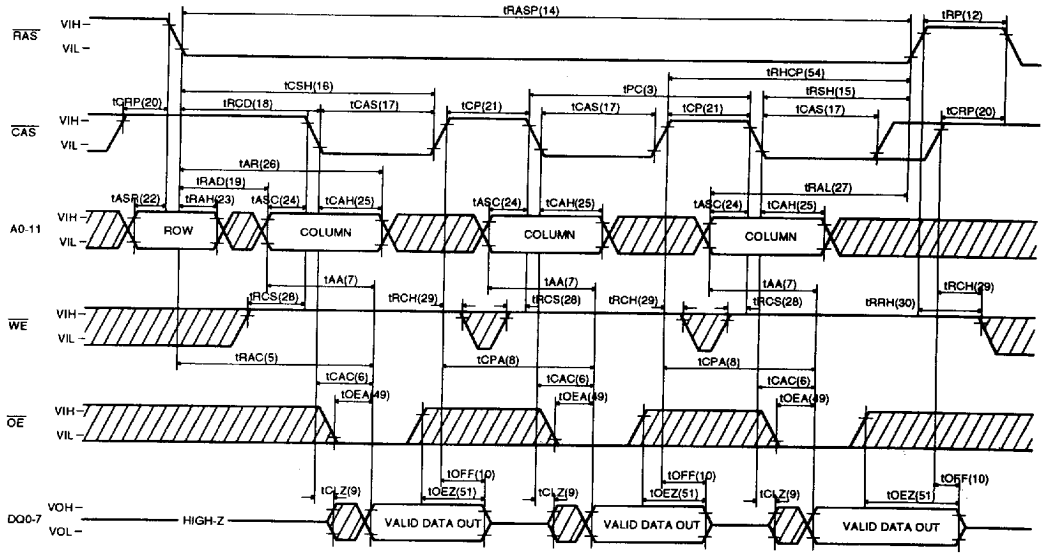
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



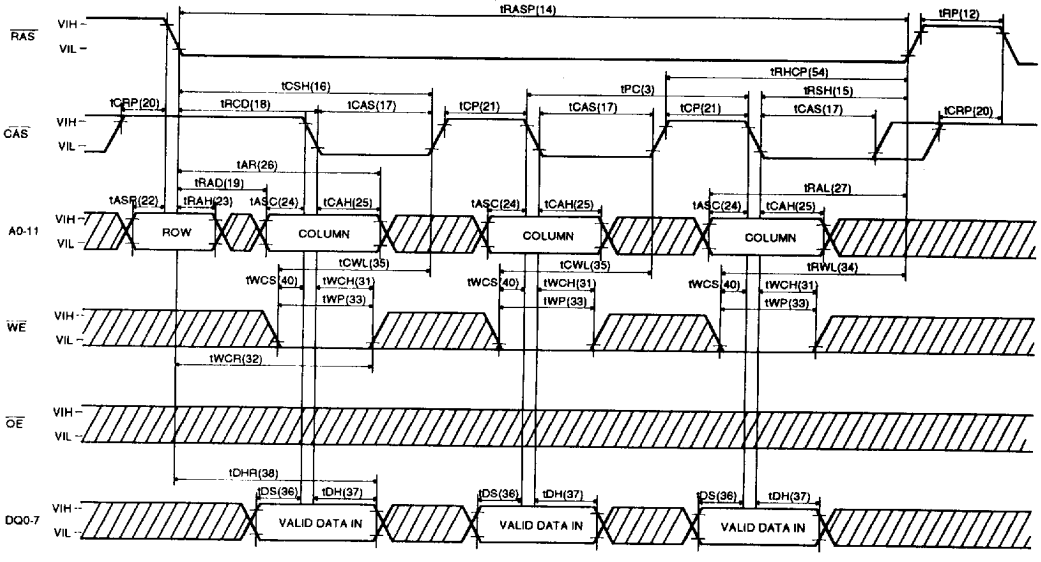
READ-MODIFY-WRITE CYCLE



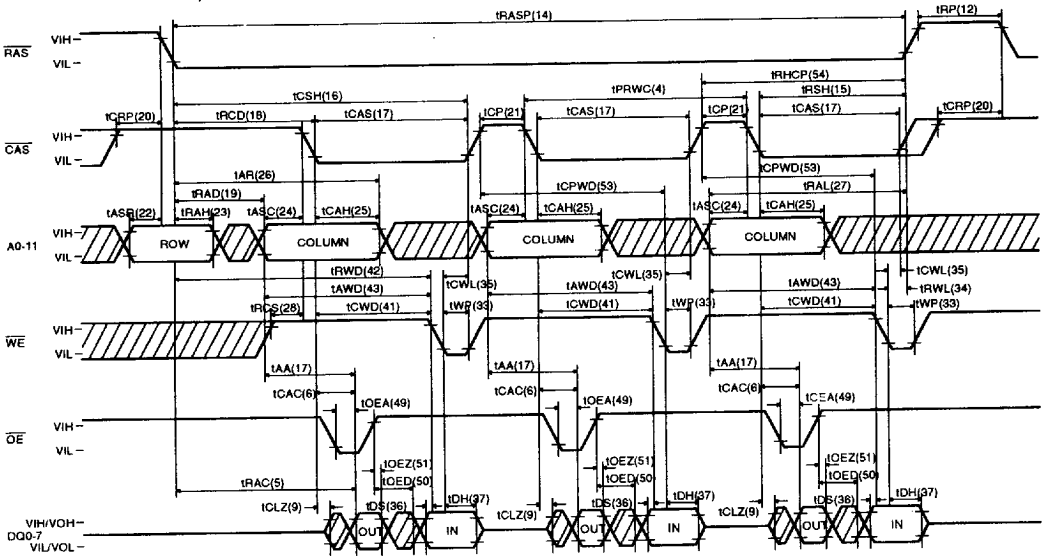
FAST PAGE MODE READ CYCLE



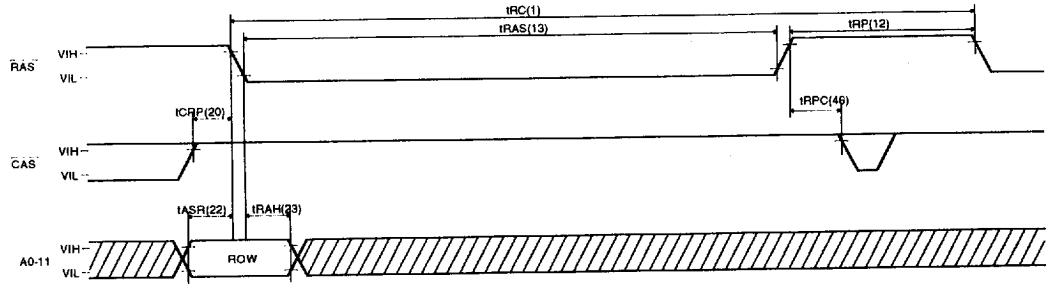
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

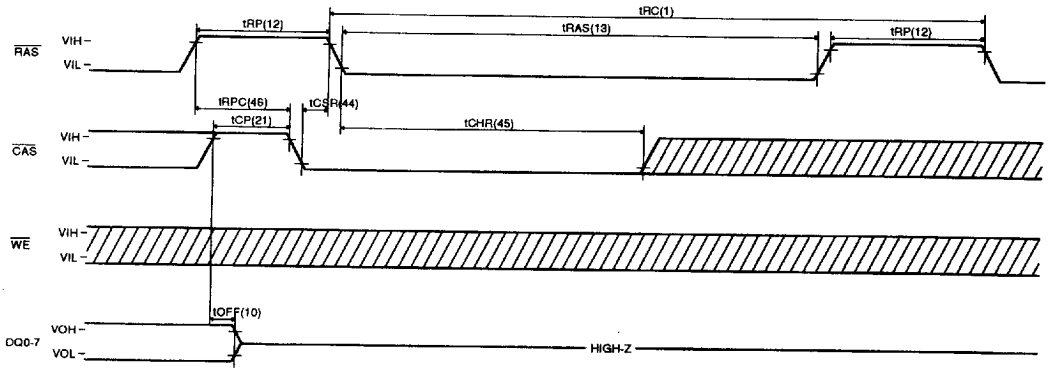


RAS-ONLY REFRESH CYCLE



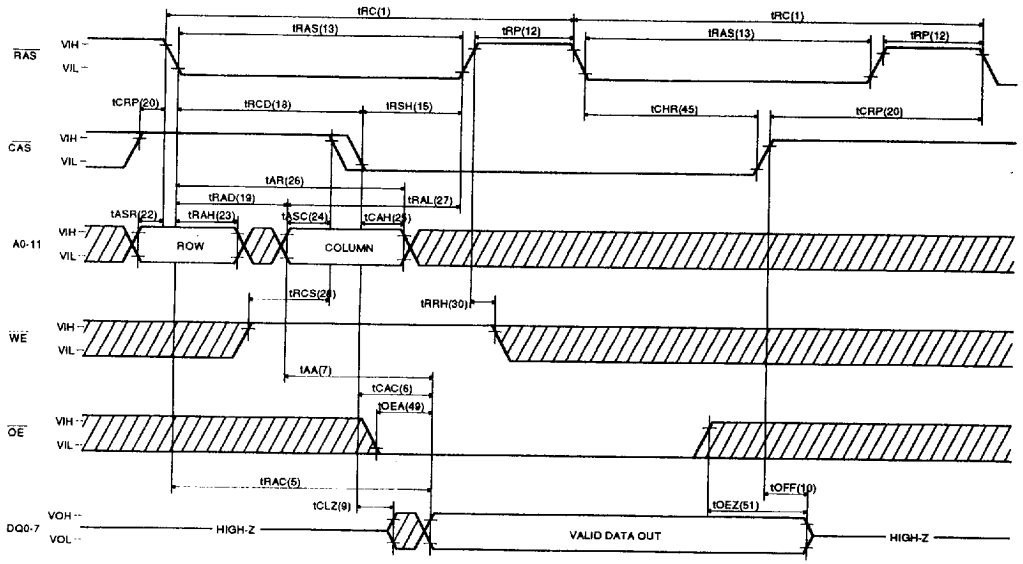
NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

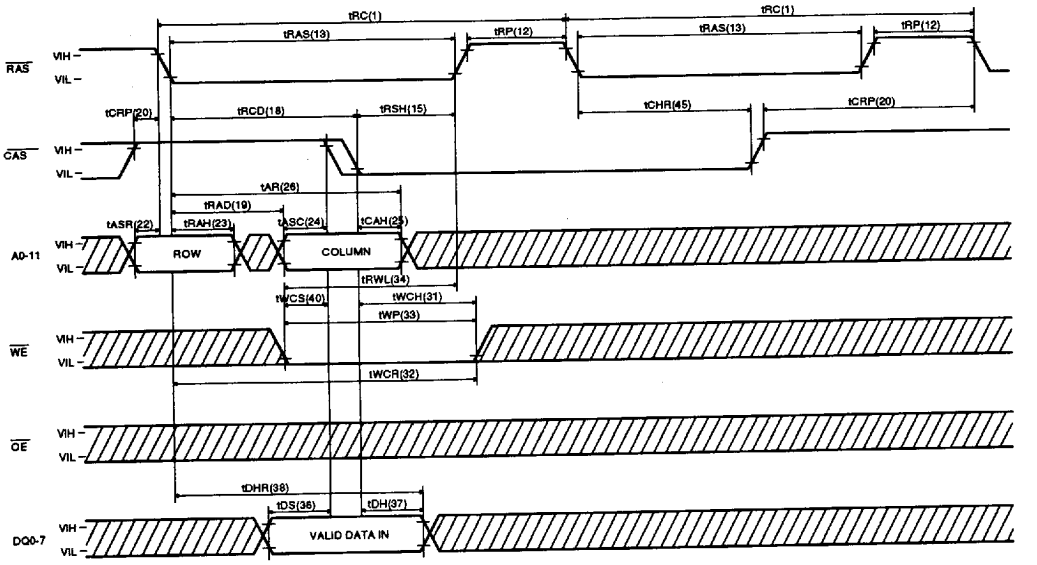


NOTE : A0-11 and $\overline{OE}$ = "H" or "L"

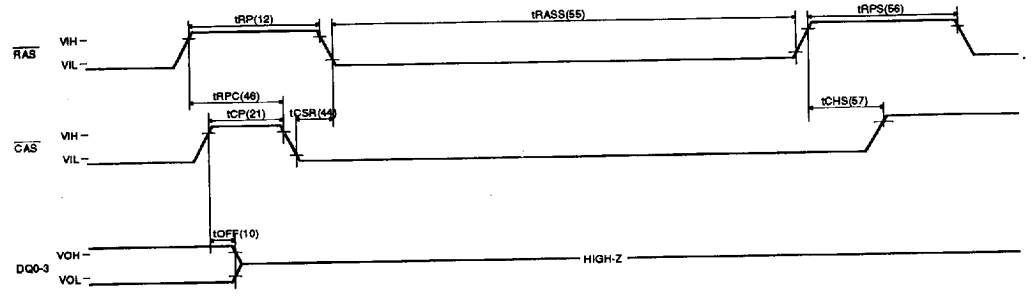
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

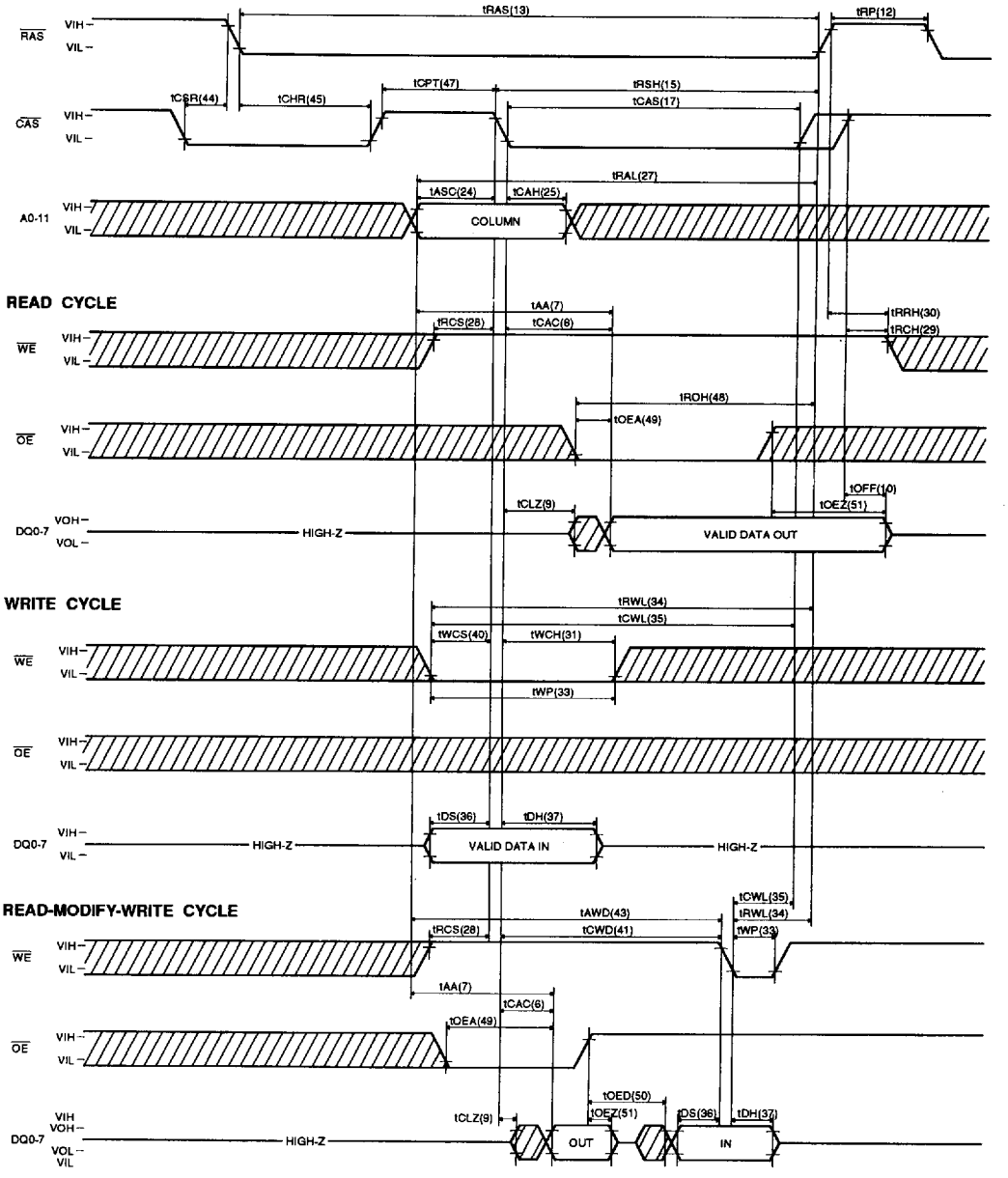


CAS-BEFORE-RAS SELF REFRESH CYCLE



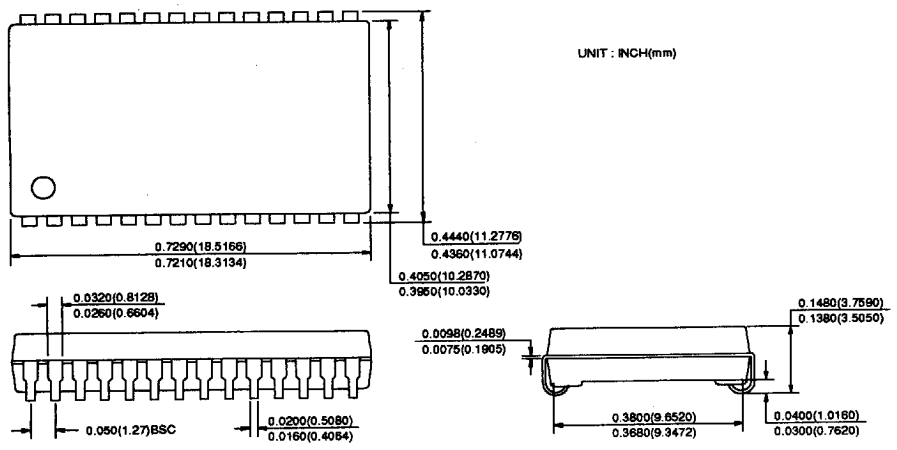
NOTE :A0-11, $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

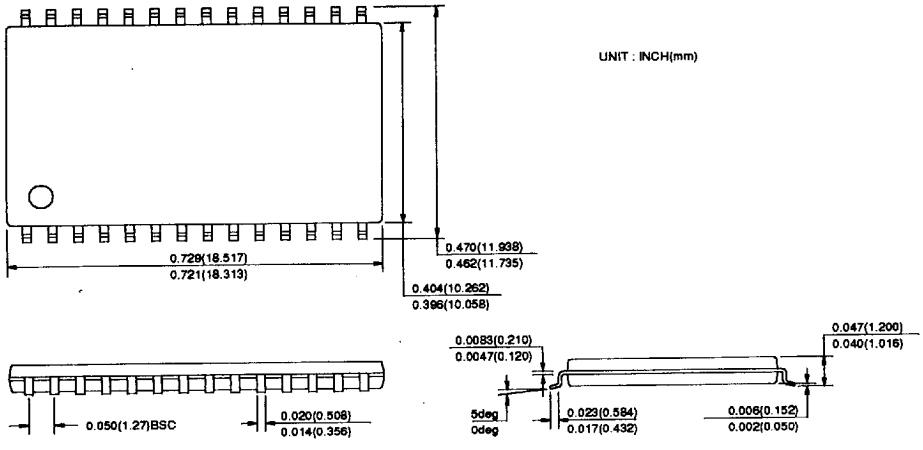


PACKAGE INFORMATION

400 mil 28/28 pin Small Outline J-form Package (JC)



400 mil 28/28 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY5116800JC	70/80/100		SOJ
HY5116800SLJC	70/80/100	SL-part	SOJ
HY5116800TC	70/80/100		TSOP-II
HY5116800SLTC	70/80/100	SL-part	TSOP-II
HY5116800RC	70/80/100		TSOP-II(R)
HY5116800SLRC	70/80/100	SL-part	TSOP-II(R)