

DESCRIPTION

The HY5117400 is the new generation and fast dynamic RAM organized 4,194,304 x 4-bit. The HY5117400 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5117400 to be packaged in standard 24/28 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V $\pm$ 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. battery back-up 2.75mW (L-part)
Max. CMOS standby 2.2mW (L-Part)
5.5mW
Max. TTL standby 11.0mW
Max. operating

Speed	Power
60	715mW
70	633mW
80	550mW

- Single power supply of 5V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

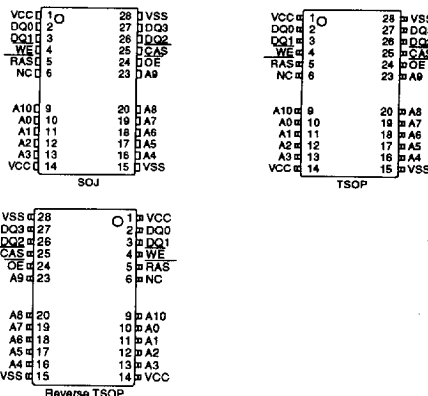
Speed	t _{RA}	t _{CAC}	t _{PC}
60	60ns	15ns	40ns
70	70ns	18ns	45ns
80	80ns	20ns	50ns

- Fast page mode operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh
- 2048 refresh cycles / 256ms (L-part)
- 2048 refresh cycles / 32ms

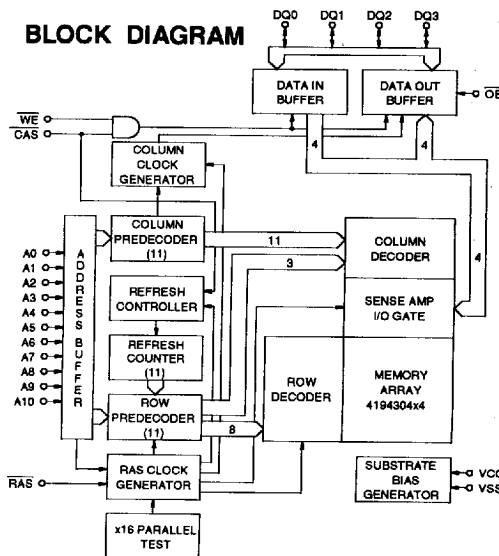
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A10	Address Input
DQ0-DQ3	Data Input/Output
VCC	Power (+ 5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
Pd	Power Dissipation	0.70	W
TSOLDER	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ VCC + 1.0V, All other pins not under test= VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	60 70 80	- - -	130 115 100	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	60 70 80	- - -	130 115 100	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tPC= tPC (min.)	60 70 80	- - -	70 65 60	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V	L-part	- -	1 0.4	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	60 70 80	- - -	130 115 100	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	tRC= 125μs, CAS= CBR cycling or 0.2V, OE & WE= VCC - 0.2V, A0-A10= VCC - 0.2V or 0.2V, DQ0-DQ3= 0.2V, VCC - 0.2V, or open	tRAS ≤ 300ns tRAS ≤ 1μs	- - -	300 500	μA	1,4,5
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS= VIL and CAS= VIH.
4. tRAS(max.)= 1μs is only applied to refresh of battery backup but tRAS(max.)= 10μs is applied to normal functional operating.
5. ICC5(max.)= 0.4mA and ICC7 are applied to L-part only (HYM5117400LJC, HYM5117400LTC and HY5117400LRC)

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

TA= 0°C to 70°C, VCC= 5V±10%, VSS= 0V, unless otherwise noted			HY5117400JC/TC/RC/LJC/LTC/LRC						UNIT	NOTE
#	SYMBOL	PARAMETER	-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,9,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	18	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	400K	70	400K	80	400K	ns	
15	tRSH	RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	18	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	52	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	11
		L-part	-	256	-	256	-	256	ms	
40	twCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5117400JC/TC/RC/LJC/LTC/LRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	40	-	45	-	45	-	ns	8
42	tRWD	RAS to WE Delay Time	85	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	55	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	15	-	15	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	15	-	15	-	ns	
49	tOEA	OE Access Time	0	15	0	18	0	20	ns	
50	tOED	OE to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	15	ns	
52	tOEH	OE Command Hold Time	15	-	15	-	15	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	60	-	65	-	70	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode during initialization.
2. AC measurements assume $t_T = 5$ ns.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in Read-Modify-Write cycles.
8. $t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}$ and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$, and $t_{CPWD} \geq t_{CPWD}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $t_{REF}(\text{max.}) = 256$ ms is applied to L-part only (HY5117400LJC, HY5117400LTC and HY5117400LRC).

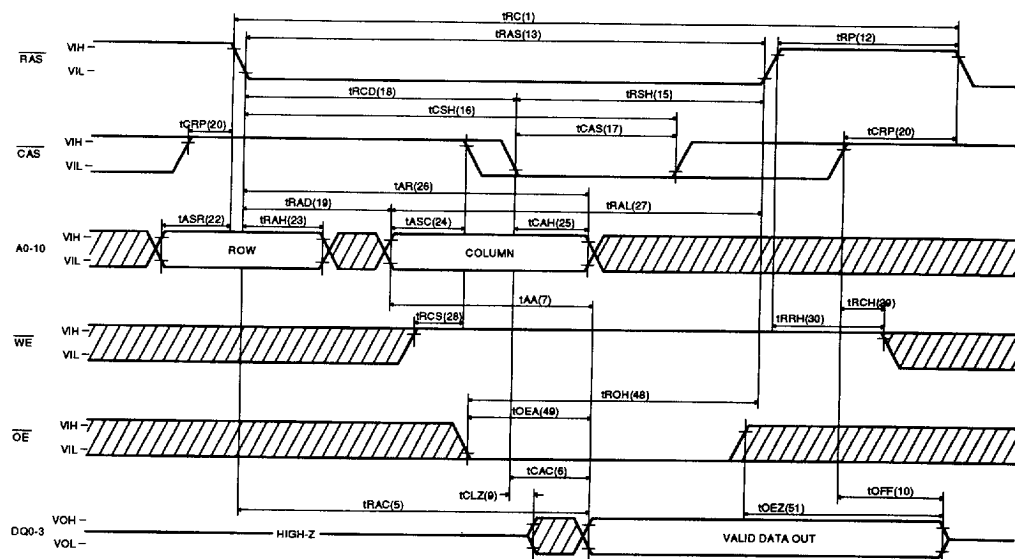
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

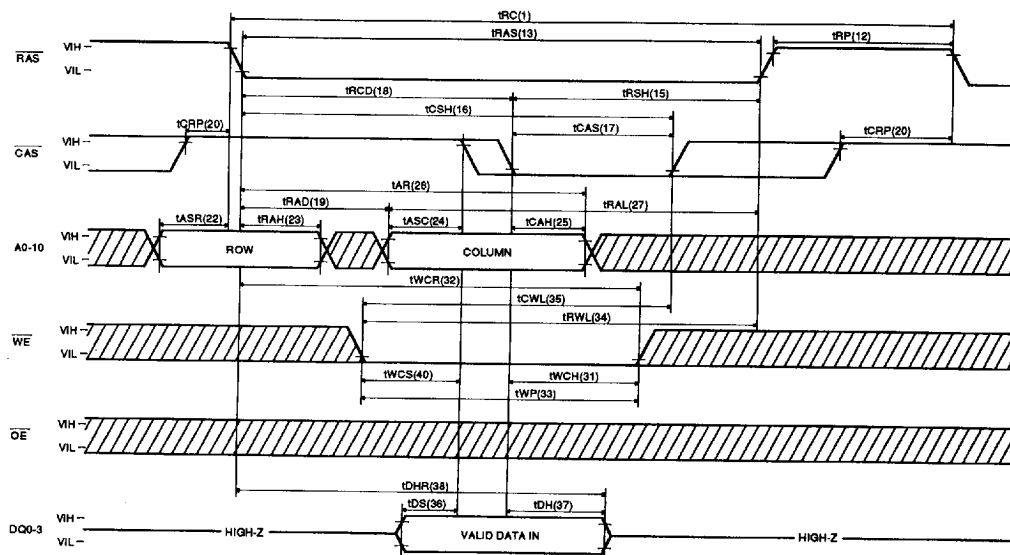
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	5	pF
CIN2	Input Capacitance (RAS, CAS, WE, OE)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ3)	-	7	pF

TIMING DIAGRAM

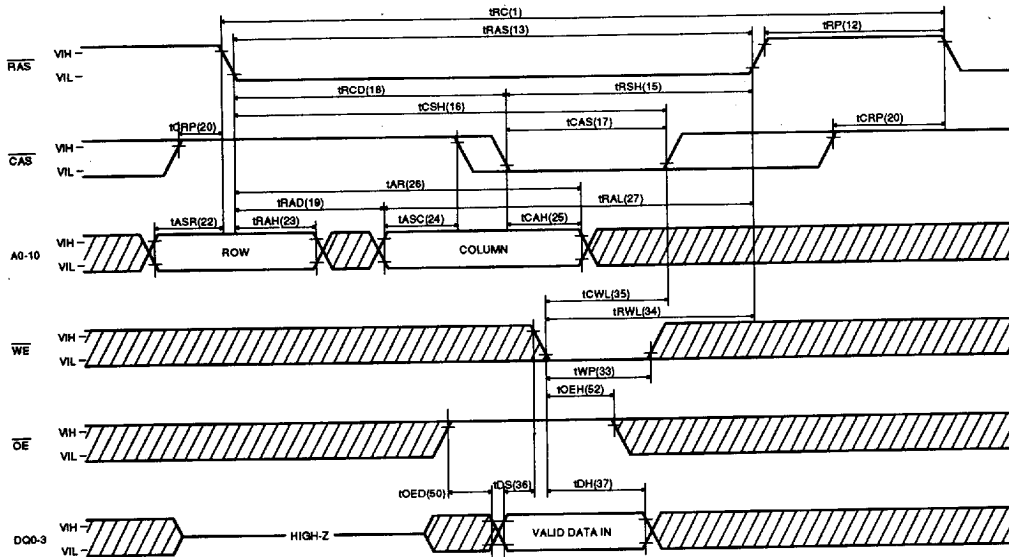
READ CYCLE



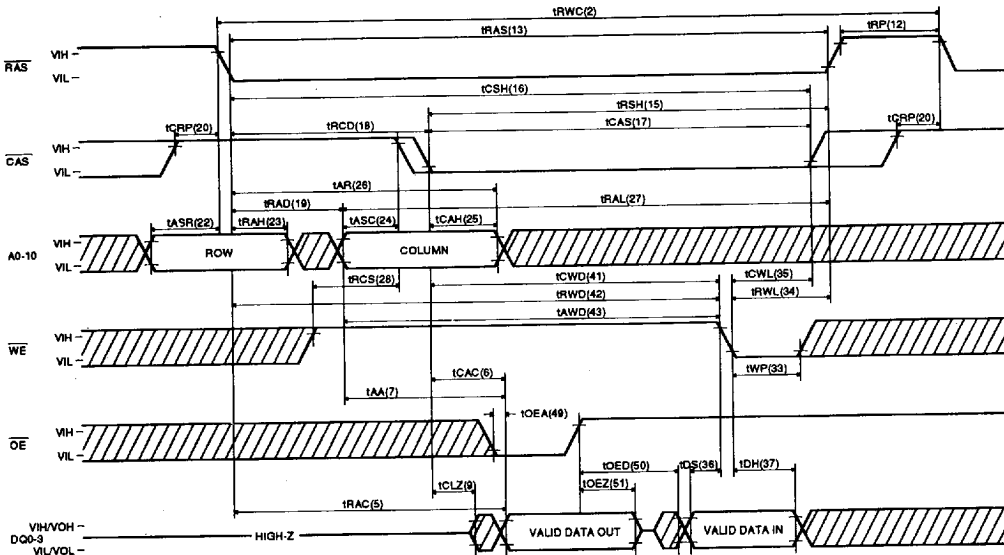
EARLY WRITE CYCLE



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



The timing diagram illustrates the relationship between the LCD controller's control signals and the data bus. The signals shown are:

- RAS**: Row Address Strobe, active low.
- CAS**: Column Address Strobe, active low.
- A0-10**: Address bus, with **ROW** and **COLUMN** periods indicated.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- DO0-3**: Data bus, with **VALID DATA OUT** periods indicated.

Key timing parameters are labeled throughout the diagram, including setup and hold times for RAS, CAS, and WE, and delay times for data output. For example, $t_{RASP}(14)$ is the RAS setup time, $t_{RSH}(15)$ is the RAS hold time, $t_{RCP}(20)$ is the RAS-to-CAS delay, and $t_{RCH}(29)$ is the RAS-to-output delay. Similar parameters are provided for CAS and WE signals.

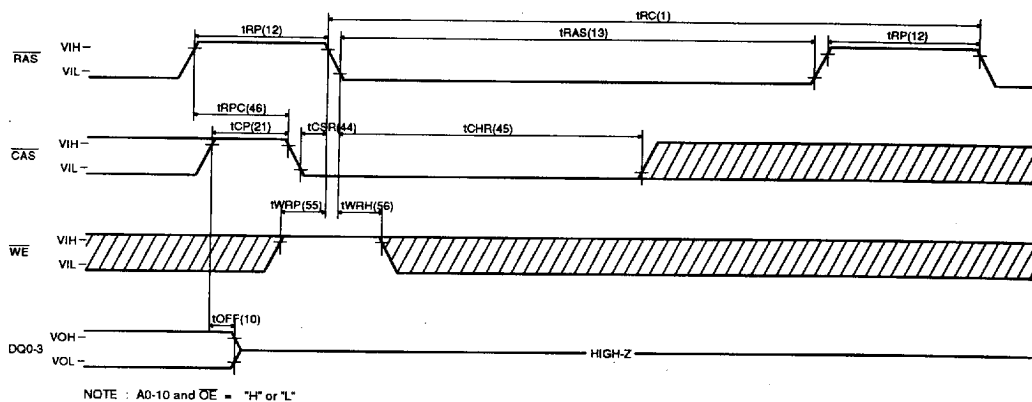
[illegible]

The diagram illustrates the timing relationships for RAS, CAS, and A0-10 signals. The RAS signal is shown as a high pulse, and the CAS signal is shown as a high pulse. The A0-10 signal is shown as a high pulse. The timing parameters are defined as follows:

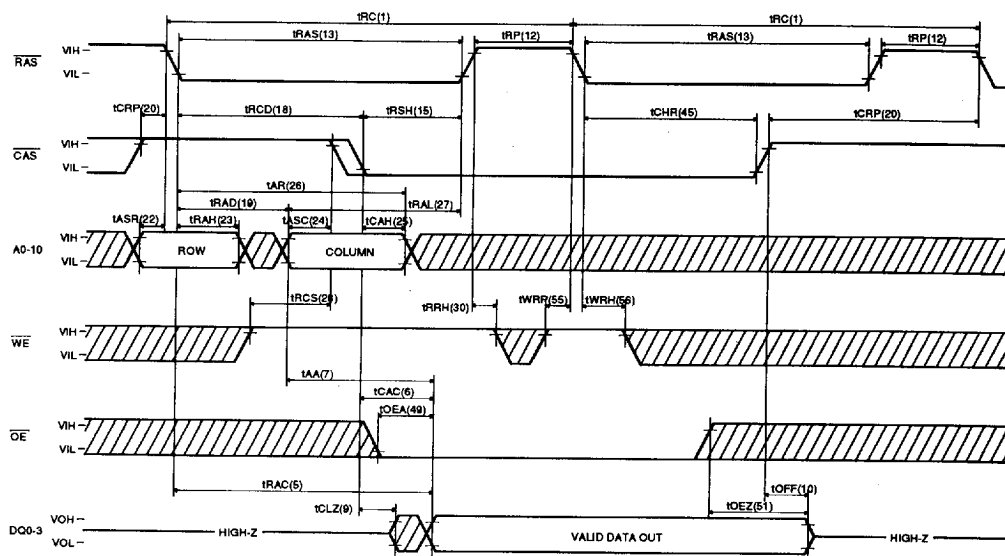
- $t_{RC}(1)$: RAS to CAS delay
- $t_{RAS}(13)$: RAS pulse width
- $t_{RP}(12)$: RAS precharge time
- $t_{RCP}(46)$: RAS to CAS delay (repeated)
- $t_{CRP}(20)$: CAS to RAS delay
- $t_{ASR}(22)$: Address to RAS delay
- $t_{RAH}(23)$: RAS to Address delay

NOTE : OE and WE = "H" or "L"

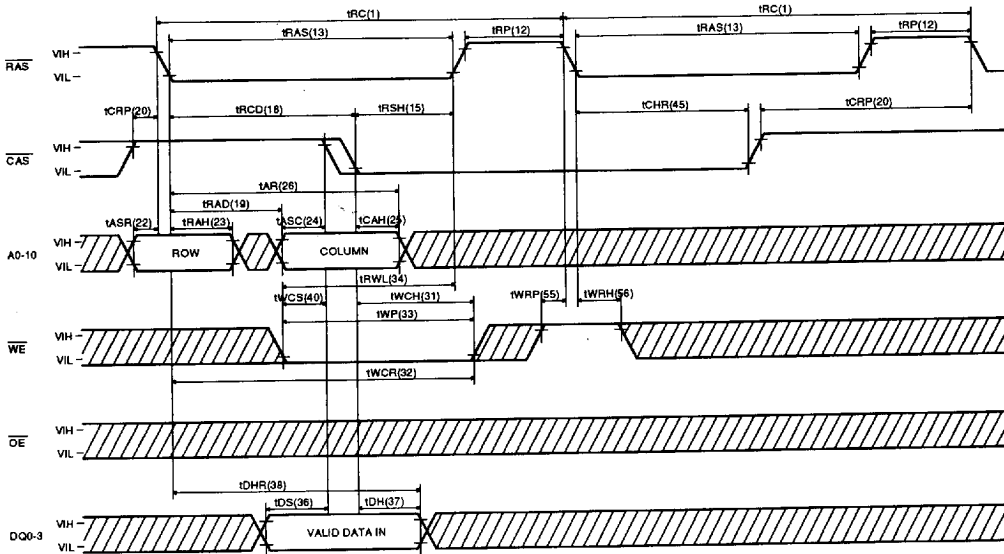
CAS-BEFORE-RAS REFRESH CYCLE



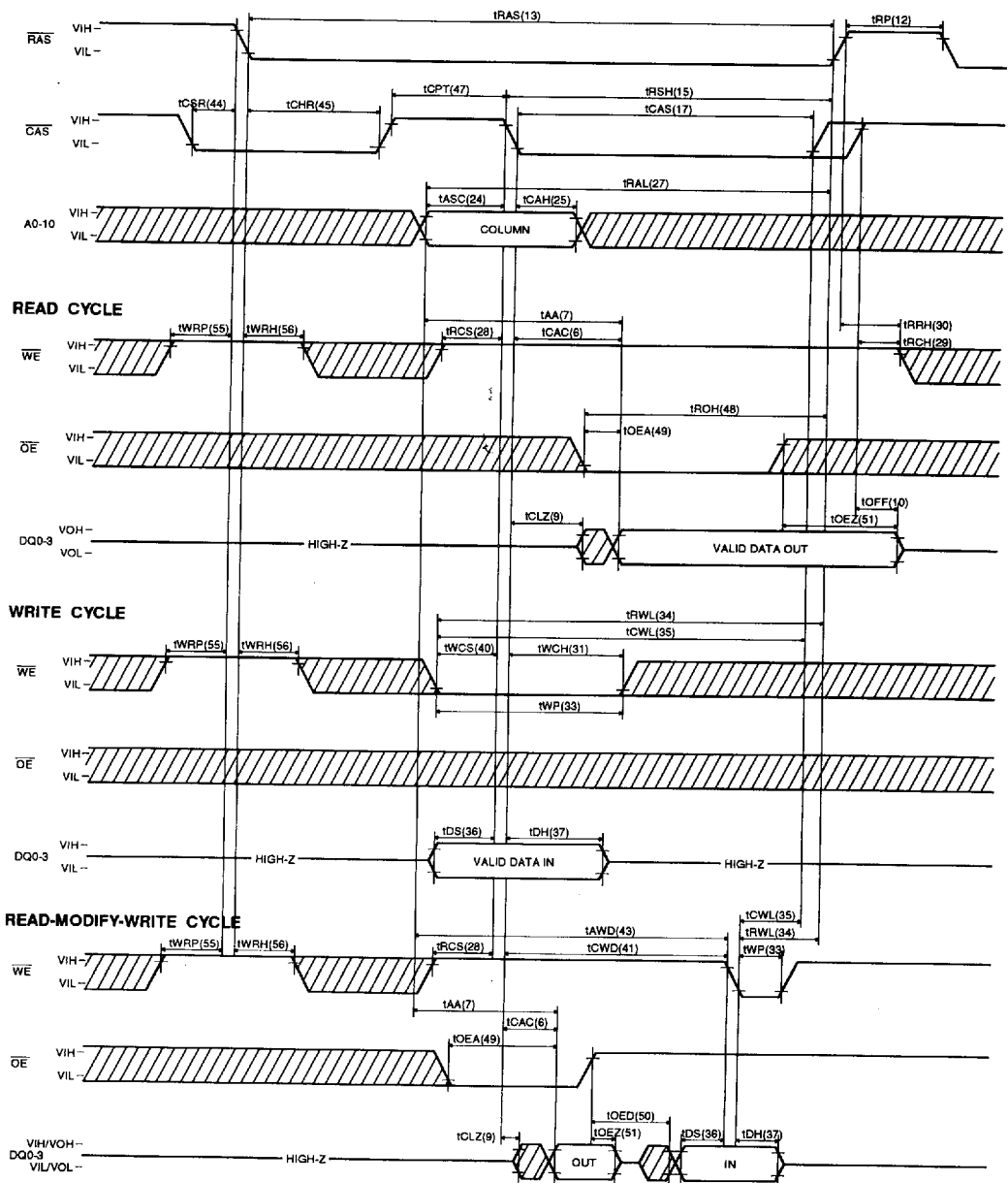
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



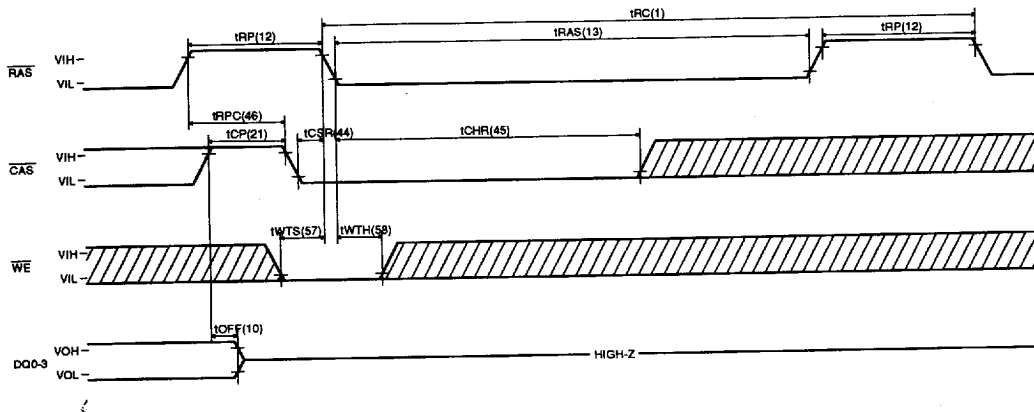
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



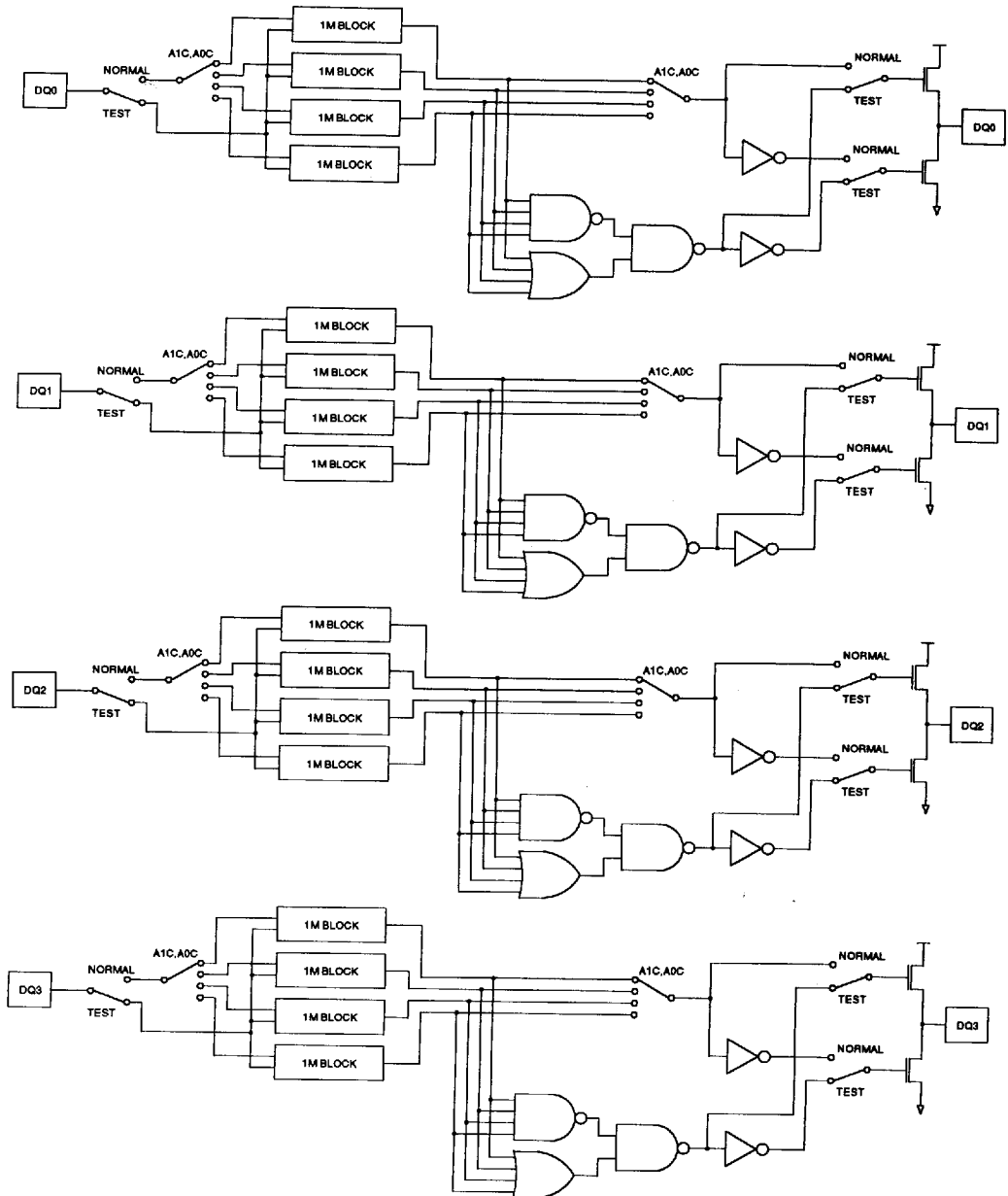
TEST MODE

The HY5117400 is a DRAM organized 4,194,304 x 4-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1"s or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Belowing shows the timing diagram of the HY5117400 to enter Test Mode. In Test Mode, the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM. WE, $\overline{\text{CAS}}$ -before-RAS cycle (Test Mode In Cycle) puts the HY5117400 into Test Mode and $\overline{\text{CAS}}$ -before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, $\overline{\text{CAS}}$ -before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/4 in case of N test pattern).

TEST MODE IN CYCLE

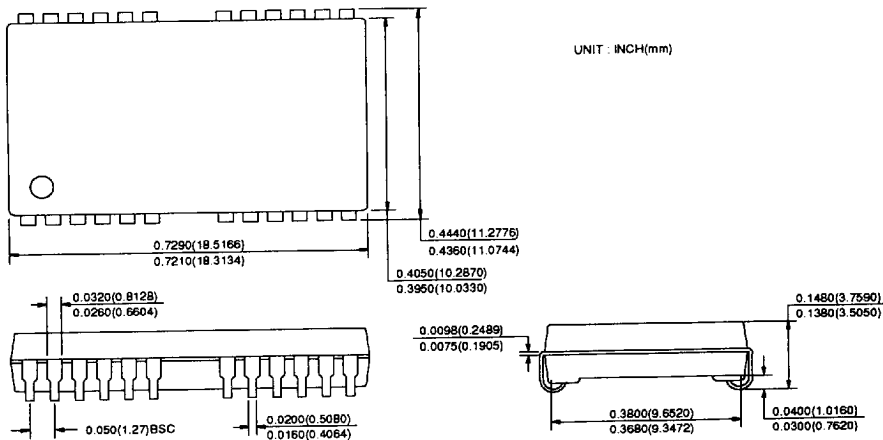


BLOCK DIAGRAM IN TEST MODE

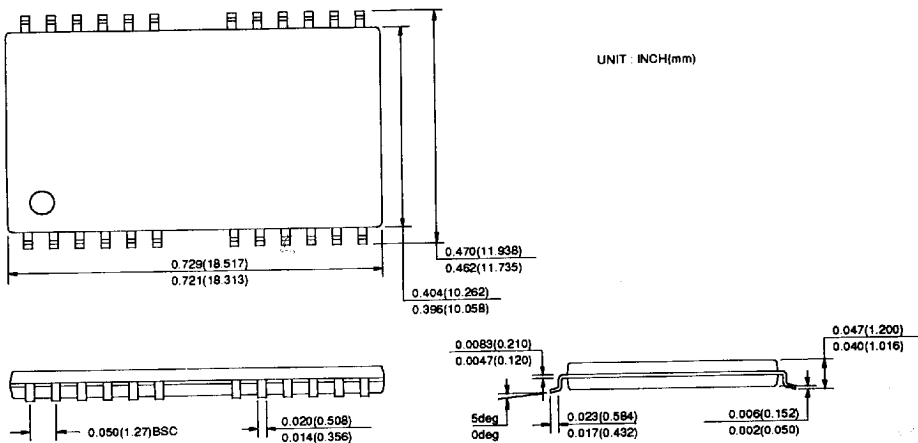


PACKAGE INFORMATION

400 mil 24/28 pin Small Outline J-form Package (JC)



400 mil 24/28 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY5117400JC	60/70/80		SOJ
HY5117400LJC	60/70/80	L-part	SOJ
HY5117400TC	60/70/80		TSOP-II
HY5117400LTC	60/70/80	L-part	TSOP-II
HY5117400RC	60/70/80		TSOP-II(R)
HY5117400LRC	60/70/80	L-part	TSOP-II(R)