

DESCRIPTION

The HY5117410A is the new generation and fast dynamic RAM organized 4,194,304 x 4-bit. The HY5117410A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5117410A to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. battery back-up 2.75mW (SL-part)
Max. CMOS standby 2.2mW (SL-part)
5.5mW

Max. TTL standby 11.0mW

Max. operating

Speed	Power
50	798mW
60	660mW
70	550mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access Time

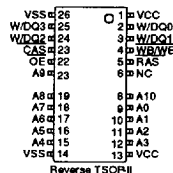
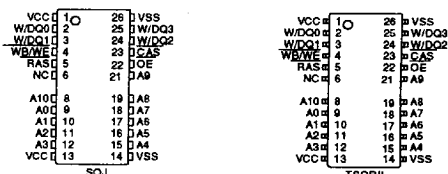
Speed	t _{TRC}	t _{CAS}	t _{PC}
50	50ns	13ns	35ns
60	60ns	15ns	40ns
70	70ns	18ns	45ns

- Fast page mode operation
- Write-Per-Bit and Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh
- 2048 refresh cycles / 256ms (SL-part)
2048 refresh cycles / 32ms

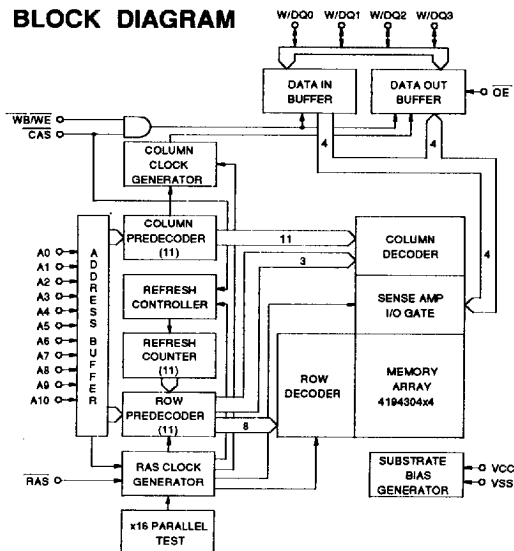
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WB/WE	Write-Per-Bit / Write Enable
OE	Output Enable
A0-A10	Address Input
W/DQ0-DQ3	Write mask / Data IO
VCC	Power (+5V)
VSS	Ground

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.02	W
TSOLDER	Soldering Temperature• Time	260• 10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ VCC+ 1.0, All other pins not under test= VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trC= trC (min.)	50	-	145	mA	1,2,3
			60	-	120		
			70	-	100		
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH(min.), other inputs ≥ VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	trC= trC (min.),	50	-	145	mA	1,3
			60	-	120		
			70	-	100		
ICC4	VCC Supply Current, Fast Page mode	tPC= tPC (min.),	50	-	90	mA	1,2,3
			60	-	80		
			70	-	70		
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V	SL-part	-	1 0.4	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	trC= trC (min.),	50	-	145	mA	1,3
			60	-	120		
			70	-	100		
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	trC= 125μs, CAS= CBR cycling or 0.2V, OE & WB/WE= VCC-0.2V, A0-A10= VCC-0.2V or 0.2V, W/DQ0-W/DQ3= VCC - 0.2V, 0.2V or open.	trAS≤ 300ns	-	300	μA	1,4,5
			trAS≤ 1μs	-	500		
ICC8	VCC Supply Current Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V OE & WB/WE & A0-A10= VCC-0.2V or 0.2V, W/DQ0-W/DQ3= VCC - 0.2V, 0.2V or open			300	μA	5
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS= VIH and CAS= VIH.
4. trAS(max.)= 1μs is only applied to refresh of battery backup but trAS(max.)= 10μs is applied to normal functional operating.
5. ICC5(max.)= 0.4mA and ICC7 and ICC8 are applied to SL-part only (HY5117410ASLJ, HY5117410ASLT and HY5117410ASLR).

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

			HY5117410AJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
#	SYMBOL	PARAMETER	-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{RC}	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	t _{RWC}	Read-Modify-Write Cycle Time	140	-	160	-	180	-	ns	
3	t _{PC}	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	t _{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	80	-	85	-	90	-	ns	
5	t _{RAC}	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10
6	t _{CAC}	Access Time from CAS	-	13	-	15	-	18	ns	4,9
7	t _{AA}	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	t _{CPA}	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4
9	t _{CLZ}	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	t _{OFF}	Output Buffer Turn-off Delay	0	10	0	13	0	15	ns	
11	t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	t _{RP}	RAS Precharge Time	30	-	40	-	50	-	ns	
13	t _{RAS}	RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	t _{RASP}	RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	t _{RSH}	RAS Hold Time	13	-	15	-	18	-	ns	
16	t _{CSH}	CAS Hold Time	50	-	60	-	70	-	ns	
17	t _{CAS}	CAS Pulse Width	13	10K	15	10K	18	10K	ns	
18	t _{RCD}	RAS to CAS Delay	18	37	20	45	20	52	ns	9
19	t _{RAD}	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	t _{CRP}	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	t _{CP}	CAS Precharge Time	8	-	10	-	10	-	ns	
22	t _{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	t _{RAH}	Row Address Hold Time	8	-	10	-	10	-	ns	
24	t _{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	t _{CAH}	Column Address Hold Time	10	-	10	-	10	-	ns	
26	t _{AR}	Column Address Hold Time from RAS	50	-	50	-	55	-	ns	
27	t _{RAL}	Column Address to RAS Lead Time	25	-	30	-	35	-	ns	
28	t _{RCS}	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	t _{RCH}	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	t _{RRH}	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	t _{WCH}	Write Command Hold Time	8	-	10	-	10	-	ns	
32	t _{WCR}	Write Command Hold Time from RAS	45	-	55	-	60	-	ns	
33	t _{WP}	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	t _{RWL}	Write Command to RAS Lead Time	13	-	15	-	18	-	ns	
35	t _{CWL}	Write Command to CAS Lead Time	13	-	15	-	18	-	ns	
36	t _{DS}	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	t _{DH}	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	t _{DHR}	Data-In Hold Time Referenced to RAS	50	-	50	-	55	-	ns	
39	t _{REF}	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	12
		SL-part	-	256	-	256	-	256	ms	11
40	t _{WCS}	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY51V17410AJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	38	-	43	-	45	-	ns	8
42	tRWD	RAS to WE Delay Time	83	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	53	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	RAS Hold Time Reference to OE	0	-	0	-	0	-	ns	
49	tOEA	OE Access Time	-	15	-	18	-	20	ns	
50	tOED	OE to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time	0	13	0	15	0	15	ns	
52	tOEH	OE Command Hold Time	10	-	10	-	10	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	35	-	40	-	45	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	twBS	Write-Per-Bit Set-up Time (Test Mode In)	0		0		0		ns	
60	twBH	Write-Per-Bit Hold Time (Test Mode In)	10		10		10		ns	
61	twDS	Write-Per-Bit Selection Set-up Time (Test Mode In)	0		0		0		ns	
62	twDH	Write-Per-Bit Selection Hold Time (Test Mode In)	10		10		10		ns	
63	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
64	tRPS	RAS Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
65	tCHS	CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	

AC CHARACTERISTICS IN TEST MODE NOTE 13

#	SYMBOL	PARAMETER	HY5117410AJ/T/R/SLJ/SLT/SLR/						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	115	-	135	-	160	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	60	-	65	-	75	-	ns	
5	tRAC	Access Time from RAS	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from CAS	-	18	-	20	-	23	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
13	tRAS	RAS Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	RAS Hold Time	18	-	20	-	23	-	ns	
16	tCSH	CAS Hold Time	55	-	65	-	75	-	ns	
17	tCAS	CAS Pulse Width	18	10K	20	10K	23	10K	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
41	tCWD	CAS to WE Delay Time	18	-	20	-	23	-	ns	8
42	tRWD	RAS to WE Delay Time	55	-	65	-	75	-	ns	8
43	tAWD	Column Address to WE Delay Time	30	-	35	-	40	-	ns	8
49	tOEA	OE Access Time	-	20	-	20	-	25	ns	
50	tOED	OE to Data Delay	20	-	20	-	25	-	ns	
52	tOEH	OE Command Hold Time	20	-	20	-	25	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by any 8 RAS only or CAS-before-RAS refresh cycle before proper device operation is achieved.
2. If RAS=Vss during power-up, the HY5117410A could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured at VOH=2.4V and VOL=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. toFF(max.) and toEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WB/WE leading edge in Read-Modify-Write cycles.
8. twCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD tRWD(min.), tCWD tCWD(min.), tAWD tAWD(min.), and tCPWD tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indetermined.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=256ms is applied to SL-Parts (HY5117410ASLJ, HY5117410ASLT and HY5117410ASLR).
12. A burst of 2048 CAS-before-RAS refresh cycles must be executed within 64ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the test Mode.

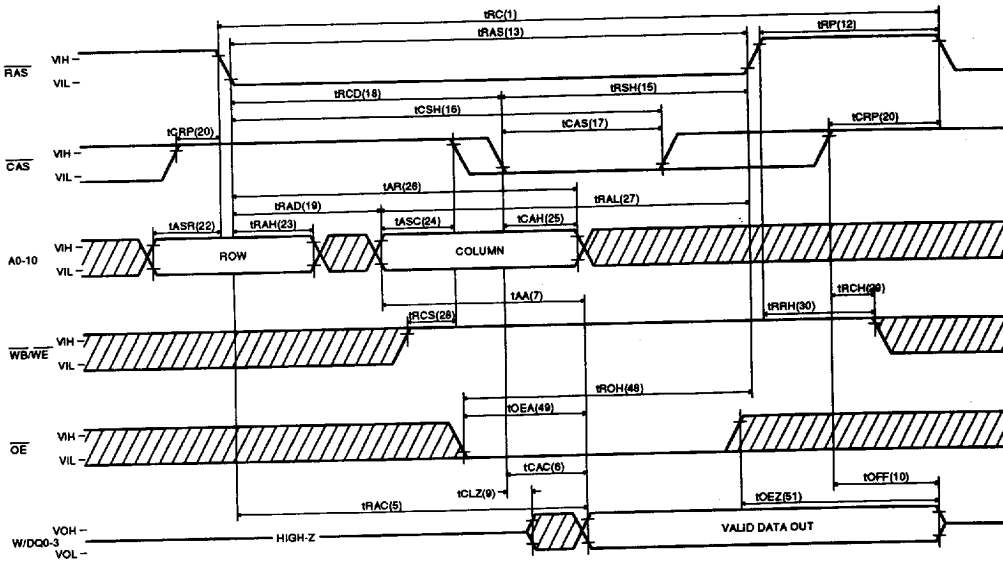
CAPACITANCE

(TA=25°C, VCC=5V 10%, VSS=0V, f=1MHz, unless otherwise noted.)

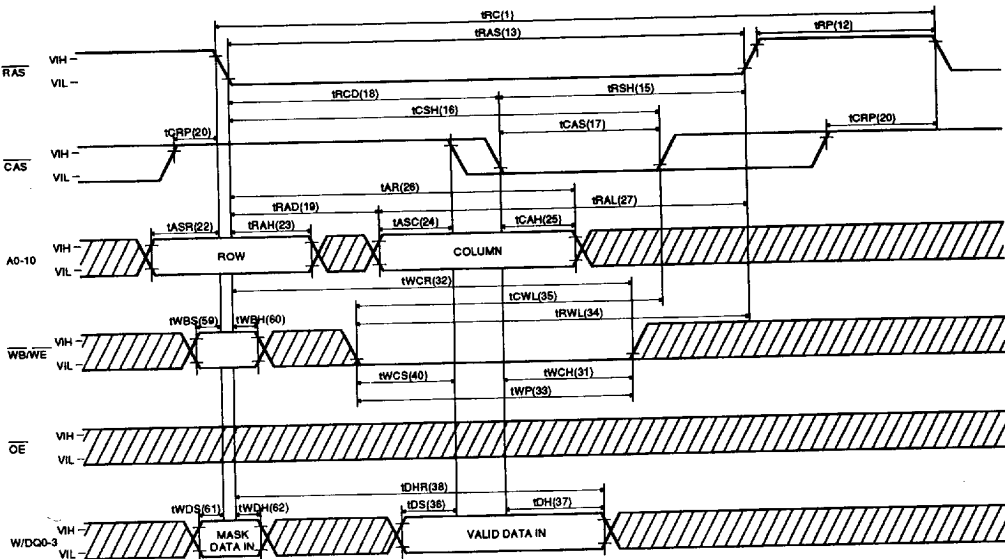
SYMBOL	PARAMETER	TYR.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	5	pF
CIN2	Input Capacitance (RAS, CAS, WB/WE, OE)	-	7	pF
CDQ	Write Mask / Data I/O Capacitance (W/DQ0-W/DQ3)	-	7	pF

TIMING DIAGRAM

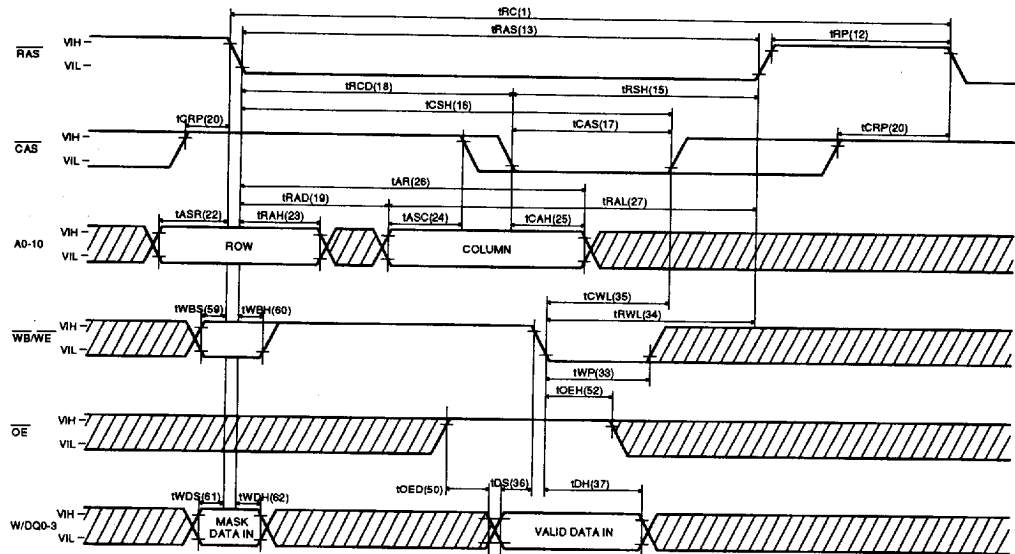
READ CYCLE



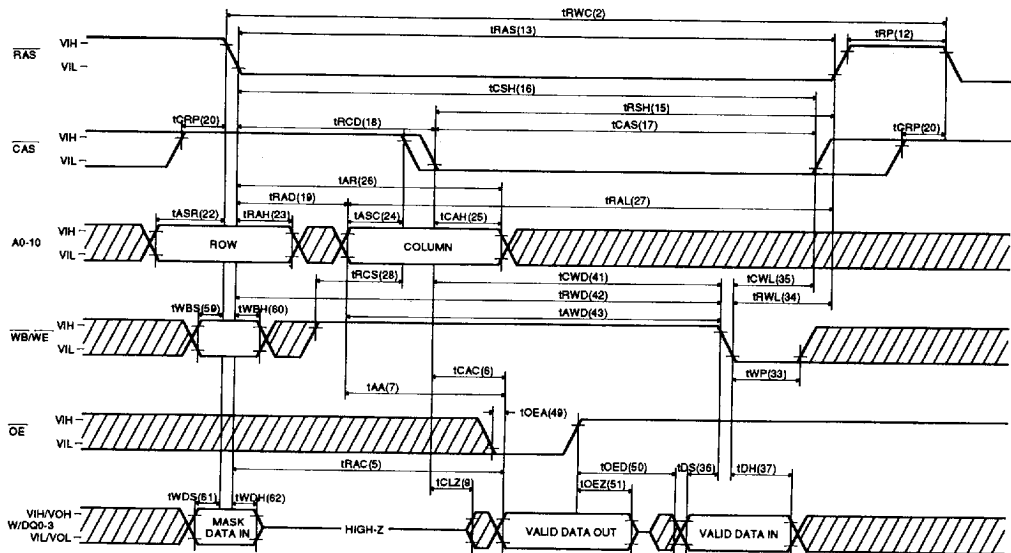
EARLY WRITE CYCLE



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



[illegible]

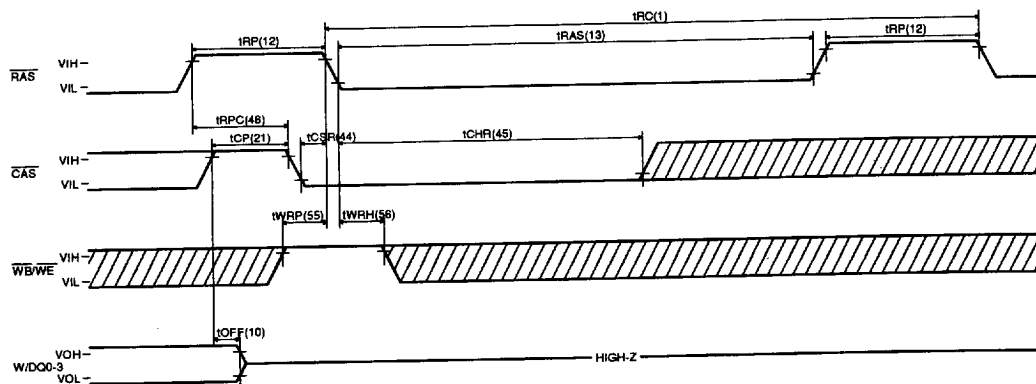
The timing diagram shows the following signals and their transitions:

- RAS**: High Voltage Input (VIH), Low Voltage Input (VIL). Transitions are labeled at the top.
- CAS**: High Voltage Input (VIH), Low Voltage Input (VIL). Transitions are labeled at the top.
- A0-10**: Address Bus. Shaded regions indicate valid address periods. Labels include ROW, COLUMN, and various address strobes like tRSH(15), tCAS(17), tCPWD(53), tRAL(27), tICLZ(9), tDS(36), tDH(37).
- WBWE**: Write Enable. Shaded regions indicate active periods. Labels include tWBS(59), tWBH(60), tRS(28), tCWD(41), tWP(33), tAA(17), tCAC(6), tOE(49), tOEZ(51), tOED(50).
- OE**: Output Enable. Shaded regions indicate active periods. Labels include tOEZ(51), tOED(50).
- V/H/VOL**: Data Bus. Shaded regions indicate valid data periods. Labels include tWDS(61), tWDH(62), tRAC(5), tICLZ(9), tDS(36), tDH(37).

The diagram also includes labels for various internal delays and setup times, such as tRSP(12), tCRP(20), tCSH(16), tRCD(18), tCAS(17), tCP(21), tCAS(17), tCPWD(53), tRSH(15), tCAS(17), tICRP(20), tIAR(26), tRAD(19), tIAH(23), tASC(24), tCAH(25), tIASQ(22), tIASC(24), tCAH(25), tIAL(27), tIRWD(42), tAWD(43), tCWL(35), tAWD(43), tCWL(35), tIRWL(34), tRWP(33), tIOWB(59), tIWBH(60), tIRS(28), tICWD(41), tIWP(33), tIAA(17), tCAC(6), tIOEA(49), tIOEZ(51), tIOED(50), tIDH(37), tIDL(37), tIDS(36), tIDH(37), tIDL(37), tIDS(36), tIDH(37), tIDL(37), tIDS(36), tIDH(37), tIDL(37), tIDS(36), tIDH(37), tIDL(37).

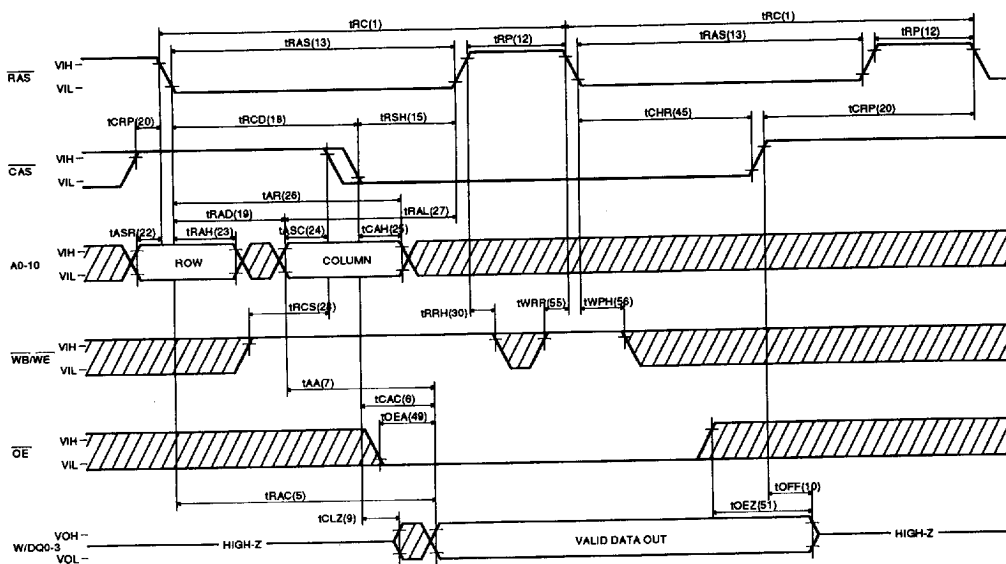
NOTE : OE and WE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

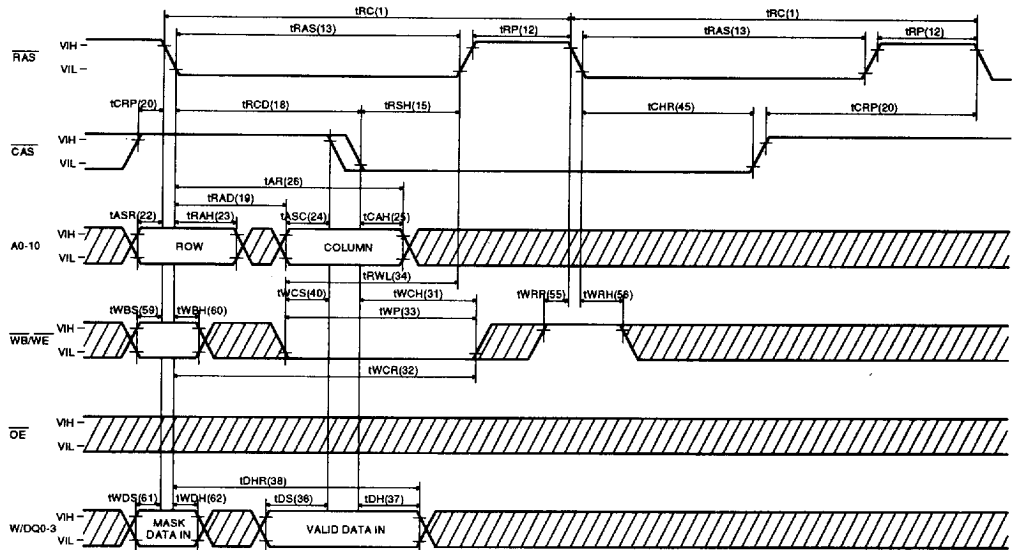


NOTE : A0-10 and OE = "H" or "L"

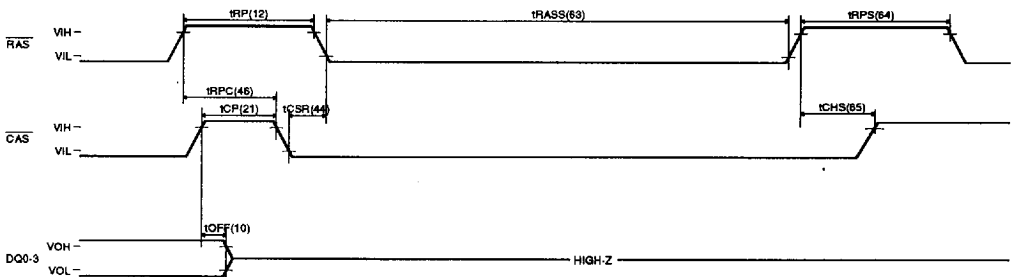
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

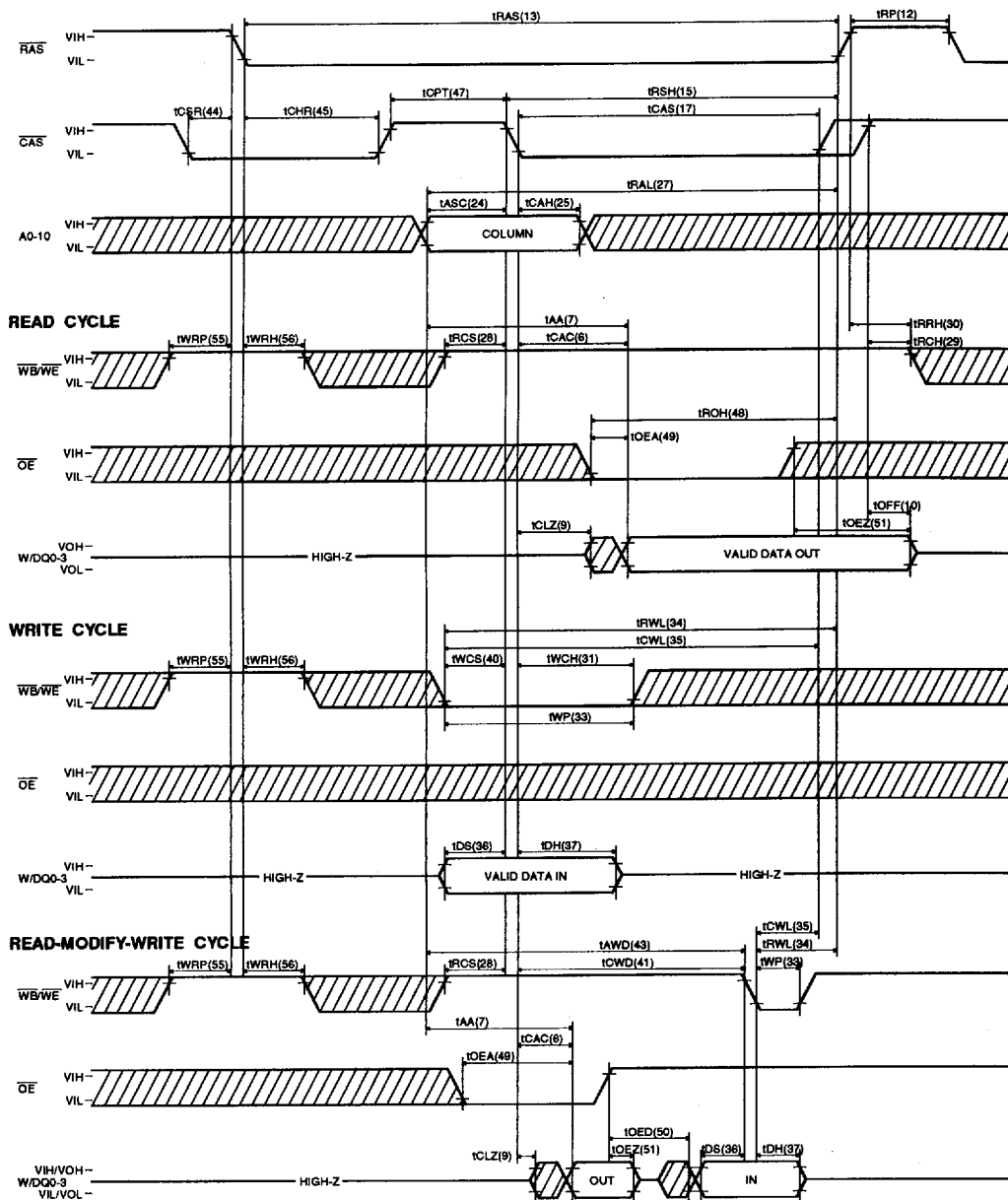


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE A0-10, OE and WE = "H" or "L"

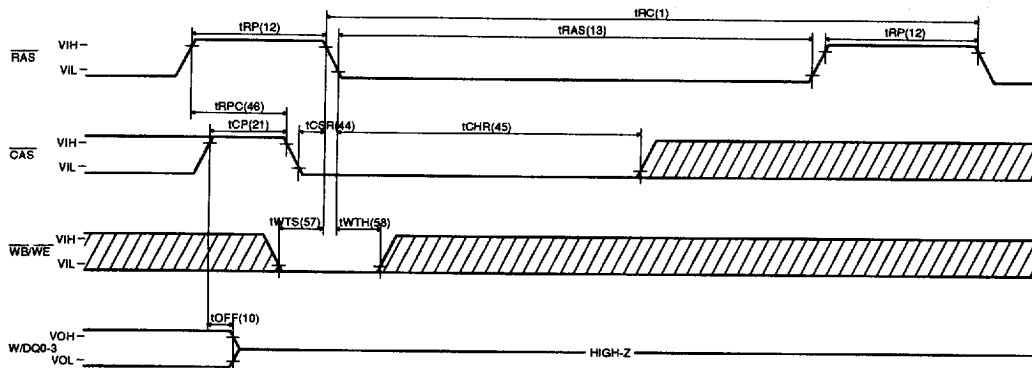
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



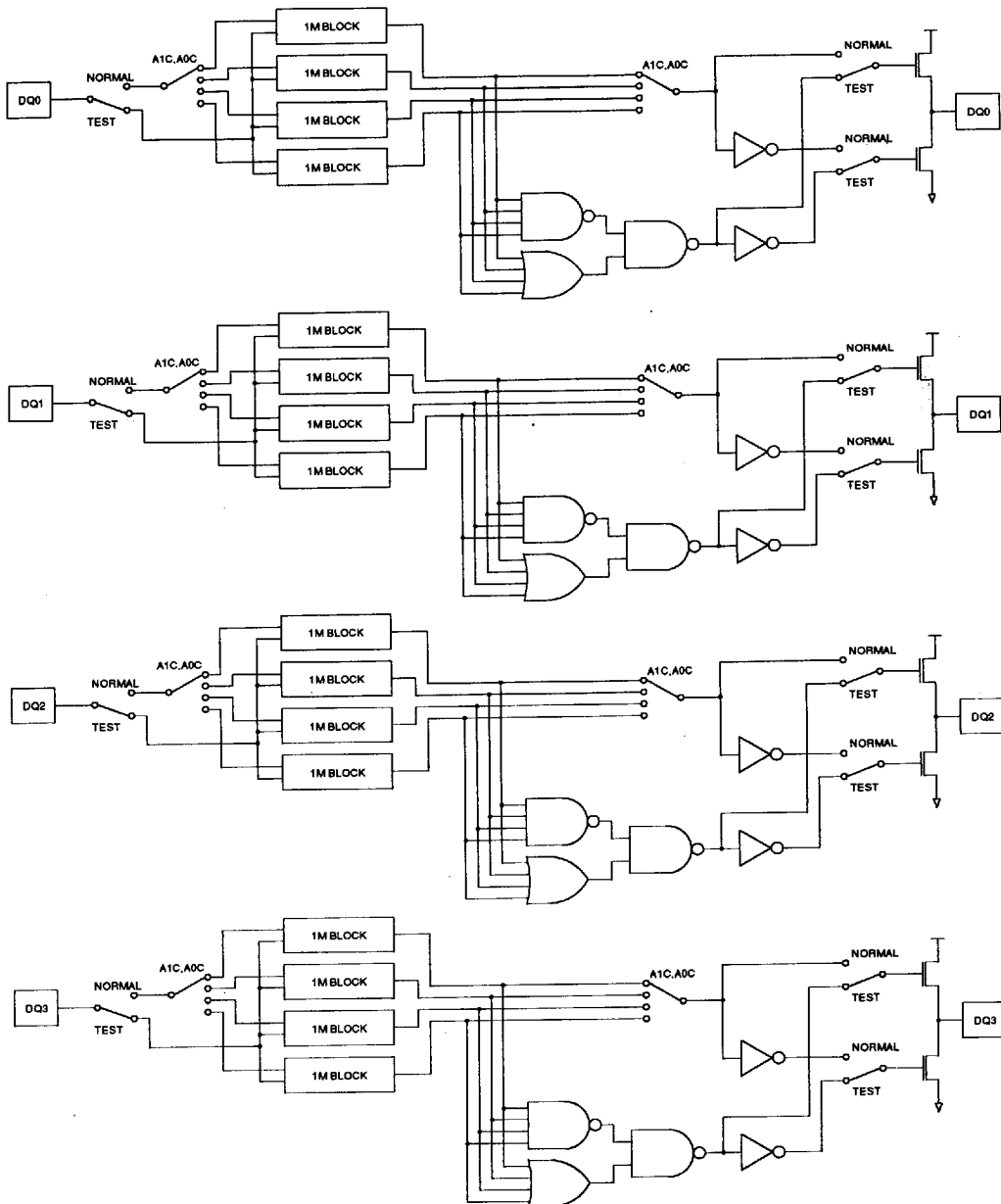
TEST MODE

The HY5117410A is a DRAM organized 4,194,304 x 4-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1"s or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Belowing shows the timing diagram of the HY5117410A to enter Test Mode. In Test Mode, the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM. WE, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY5117410A into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/4 in case of N test pattern).

TEST MODE IN CYCLE

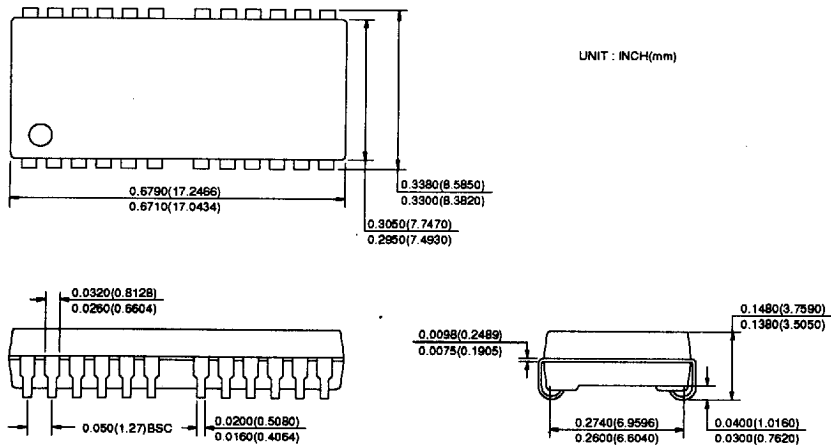


BLOCK DIAGRAM IN TEST MODE

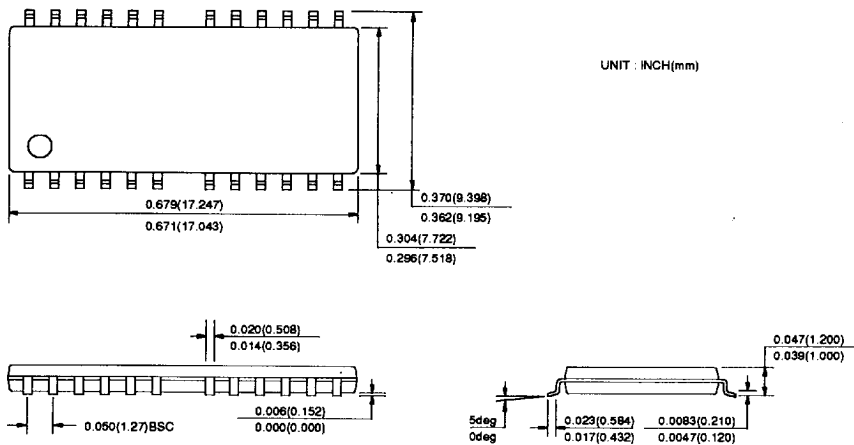


PACKAGE INFORMATION

300 mil 24/26 pin Small Outline J-form Package (J)



300 mil 24/26 pin Thin Small Outline Package (T) (R)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY5117410AJ	50/60/70		SOJ
HY5117410ASLJ	50/60/70	SL-part	SOJ
HY5117410AT	50/60/70		TSOP-II
HY5117410ASLT	50/60/70	SL-part	TSOP-II
HY5117410AR	50/60/70		TSOP-II(R)
HY5117410ASLR	50/60/70	SL-part	TSOP-II(R)