

DESCRIPTION

The HY512260 is the new generation and fast dynamic RAM organized 131,072 x 16-bit configuration employing advanced submicron CMOS process technology and advanced circuit design technique to achieve fast access time. Independant read and write of upper and lower byte is controlled by 2 separate CAS inputs.

Refresh control is provided through RAS-only, CAS-before-RAS, hidden refresh and self refresh modes. Multiplexed address inputs permit the HY512260 to be packaged in a 400mil 40pin SOJ and 40/44pin TSOP-II and reverse TSOP-II packages.

FEATURES

- Low power dissipation
 - Max. battery back-up 2.2mW (L-part)
 - Max. CMOS standby 1.1mW (L-part)
 - 5.5mW
 - Max. TTL standby 11.0mW
 - Max. Self refresh 2.2mW(SL-part)

Speed	Power
50	605.0mW
60	550.0mW
70	495.0mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access and cycle time

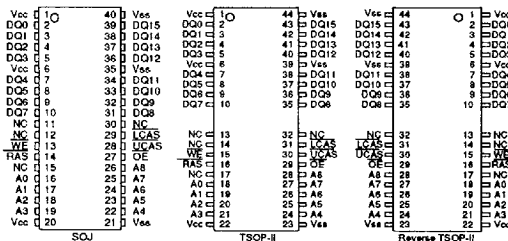
Speed	t _{TRAC}	t _{CAC}	t _{PC}
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Fast page mode operation
- 2 CAS inputs for upper and lower byte control
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh
- 512 refresh cycles / 128ms (L-part)
- 512 refresh cycles / 8ms

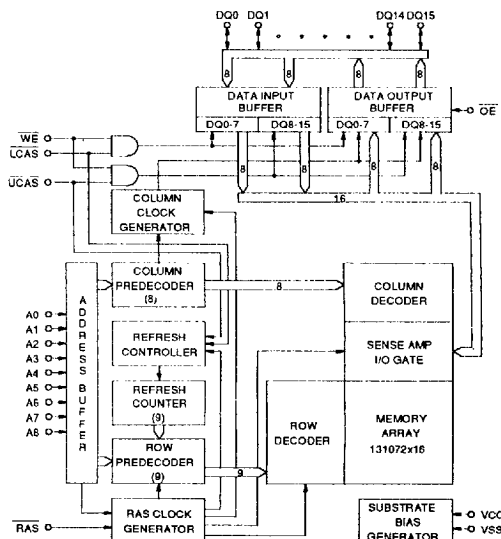
PIN DESCRIPTION

RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A8	Address Input
DQ0-DQ15	Data Input/Output
Vcc	Power (+5V)
VSS	Ground

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	0.90	W
TSOLDER	Soldering Temperature•Time	260•10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS≤VIN≤6.5V, All other pins not under test=VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS≤VOUT≤5.5V, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC=tRC (min.)	50 60 70	- - -	110 100 90	mA	1,2,3,7
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs≥VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC=tRC (min.)	50 60 70	- - -	110 100 90	mA	1,3,7
ICC4	VCC Supply Current, Fast Page mode	tPC=tPC (min.)	50 60 70	- - -	80 70 60	mA	1,2,3,7
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥VCC-0.2V	L-part	-	1 200	mA μA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC=tRC (min.)	50 60 70	- - -	100 100 90	mA	1,3,7
ICC7	VCC Supply Current, Battery Back Up (L-part only)	tRC=125μs, tRAS≤1μs CAS=CBR cycling or 0.2V OE & WE=VCC-0.2V A0-A8=VCC-0.2V or 0.2V DQ0-DQ15 =0.2V, VCC-0.2V or open		-	400	μA	1,4,5
ICC8	VCC Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7			400	μA	6
VOL	Output Low Voltage	IOL=4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH=-5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1, ICC3, ICC4 and ICC6 are dependent on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while RAS=VIL. ICC4, Address can be changed maximum once while CAS=VIH.
4. Only tRAS(max.)=1μs is applied to refresh of battery backup but tRAS(max.)=10μs is applied to normal functional operation.
5. ICC5(max.)=200μA and ICC7 are applied to L-parts (HY512260LJ, HY512260LT, HY512260LR, HY512260SLJ, HY512260SLT, and HY512260SLR.)
6. ICC8 is applied to SL-parts only (HY512260SLJ, HY512260SLT and HY512260SLR).
7. Operating Condition for 50ns Part is VCC=5V±5%, Cout=30pF.

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.) NOTE : 1, 2, 3, 13, 18

#	SYMBOL	PARAMETER	HY512260J/T/R/LJ/LT/LR/ SLJ/SLT/SLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	130	-	155	-	185	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns	
5	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	15	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4,15
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	50	100K	60	100K	70	100K	ns	
15	tRSH	RAS Hold Time	15	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	CAS Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	15	35	20	45	20	50	ns	9
19	tRAD	RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	14
26	tAR	Column Address Hold Time from RAS	40	-	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	14
32	tWCR	Write Command Hold Time from RAS	40	-	45	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	15	-	20	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	40	-	50	-	55	-	ns	
39	tREF	Refresh Period (512 cycles)	-	8	-	8	-	8	ms	12
		L-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,14

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AC CHARACTERISTICS

(continued)

Continued/

#	SYMBOL	PARAMETER	HY512260J/T/R/LJ/LT/LR/ SLJ/SLT/SLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	35	-	40	-	50	-	ns	8
42	tRWD	RAS to WE Delay Time	70	-	85	-	100	-	ns	8
43	tAWD	Column Address to WE Delay Time	45	-	55	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	trPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	14
47	tcPT	CAS Precharge Time (CBR Counter Test)	20	-	20	-	25	-	ns	17
48	tROH	RAS Hold Time Referenced to OE	0	-	0	-	0	-	ns	
49	toEA	OE Access Time	-	15	-	15	-	20	ns	
50	toED	OE to Data Delay	15	-	15	-	20	-	ns	
51	toEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	20	ns	5
52	toEH	OE Command Hold Time	15	-	15	-	20	-	ns	
53	tcPWD	WE Delay Time from CAS Precharge	50	-	55	-	65	-	ns	8
54	trHCP	RAS Hold Time from CAS Precharge	35	-	35	-	40	-	ns	
55	trASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	ns	
56	trPS	RAS Precharge Time (Self Refresh)	120	-	130	-	150	-	ns	
57	tCHS	CAS Hold Time from RAS (Self Refresh)	-50	-	-50	-	-50	-	ns	

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NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ -only refresh cycles are required.
2. If $\overline{\text{RAS}}=\text{Vss}$ during power-up, the HY512260 could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with Vcc during power-up or be held at a valid Vih in order to minimize the power-up current.
3. $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$ are reference levels for measuring timing of input signals. Transition times are measured between $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$, and are assumed to be 5ns for all inputs.
4. Measured at $\text{Voh}=2.0\text{V}$ and $\text{Vol}=0.8\text{V}$ with a load equivalent to 2 TTL loads and 100pF for 60ns, 70ns part and measured at $\text{Voh}=2.0\text{V}$ and $\text{Vol}=0.8\text{V}$ with a load equivalent to 2TTL loads and 30pF for 50ns part..
5. $\text{toff}(\text{max.})$ and toez define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trch or trrh must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. twcs , trwd , tcwd , tawd and tcpwd are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{twcs} \geq \text{twcs}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{min.})$, $\text{tcwd} \geq \text{tcwd}(\text{min.})$, $\text{tawd} \geq \text{tawd}(\text{min.})$, and $\text{tcpwd} \geq \text{tcpwd}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $\text{trcd}(\text{max.})$ limit insures that $\text{trac}(\text{max.})$ can be met. $\text{trcd}(\text{max.})$ is specified as a reference point only. If trcd is greater than the specified $\text{trcd}(\text{max.})$ limit, then access time is controlled by tcac .
10. Operation within the $\text{trad}(\text{max.})$ limit insures that $\text{trac}(\text{max.})$ can be met. $\text{trad}(\text{max.})$ is specified as a reference point only. If trad is greater than the specified $\text{trad}(\text{max.})$ limit, then access time is controlled by taa .
11. $\text{tREF}(\text{max.})=128\text{ms}$ is applied to L-parts (HY512260LJC, HY512260LTC, HY512260LRC, HY512260SLJC, HY512260SLTC and HY512260SLRC).
12. A burst of 512 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 8ms (128ms for L-part) after exiting self refresh.
13. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ must be transited simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
15. These parameters are determined by the later rising edge of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$.
16. tcwl must be satisfied by both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ for 16-bits access cycles.
17. tcp and tcpt are measured when both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are high state.
18. Operating Condition for 50ns Part is $\text{Vcc}=5\text{V} \pm 5\%$, $\text{Cout}=30\text{pF}$.

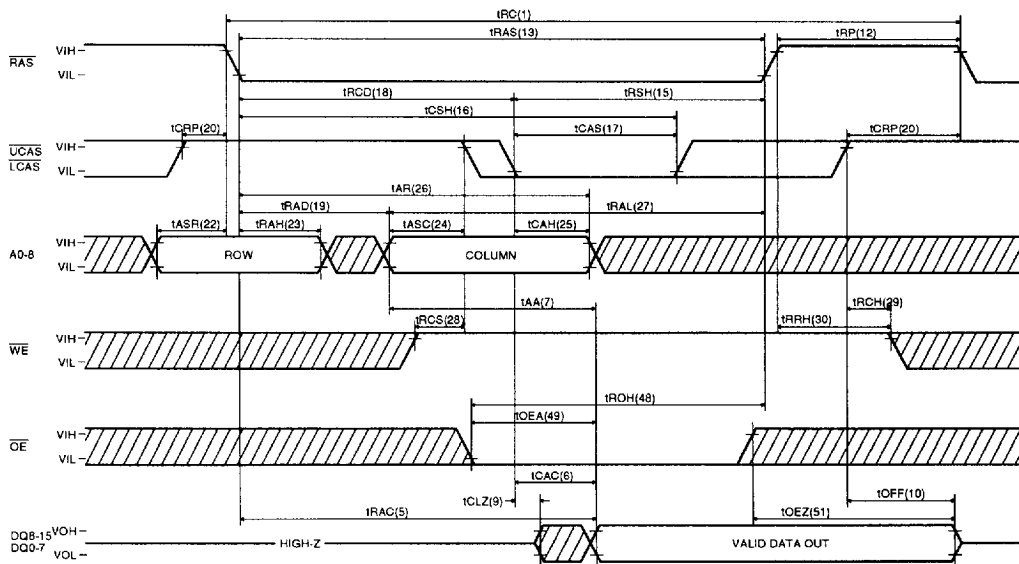
CAPACITANCE

($\text{TA}=25^\circ\text{C}$, $\text{Vcc}=5\text{V} \pm 10\%$, $\text{Vss}=0\text{V}$, $f=1\text{MHz}$, unless otherwise noted.)

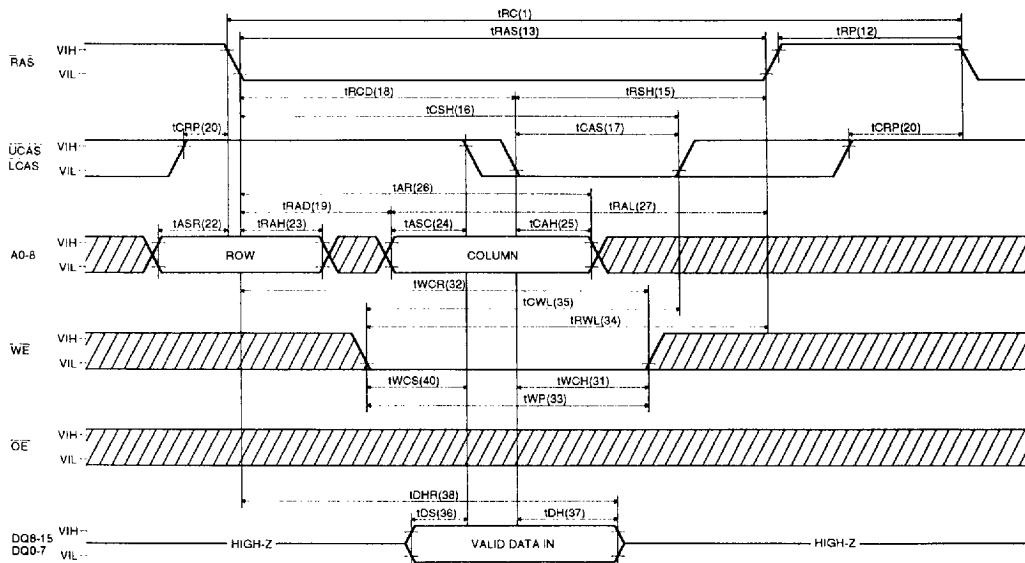
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
Cin1	Input Capacitance (A0-A8)	-	5	pF
Cin2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ15)	-	7	pF

TIMING DIAGRAM

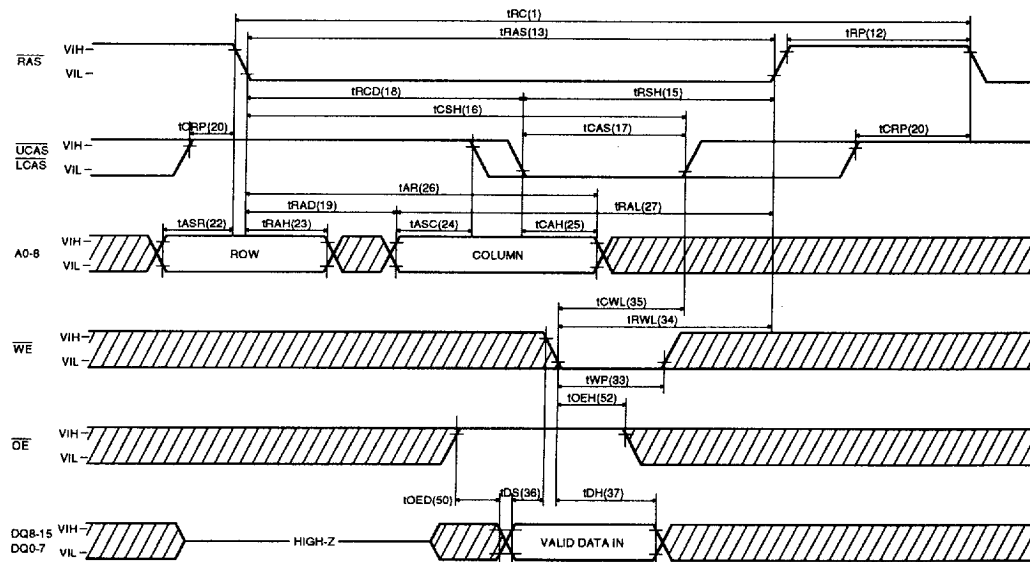
READ CYCLE



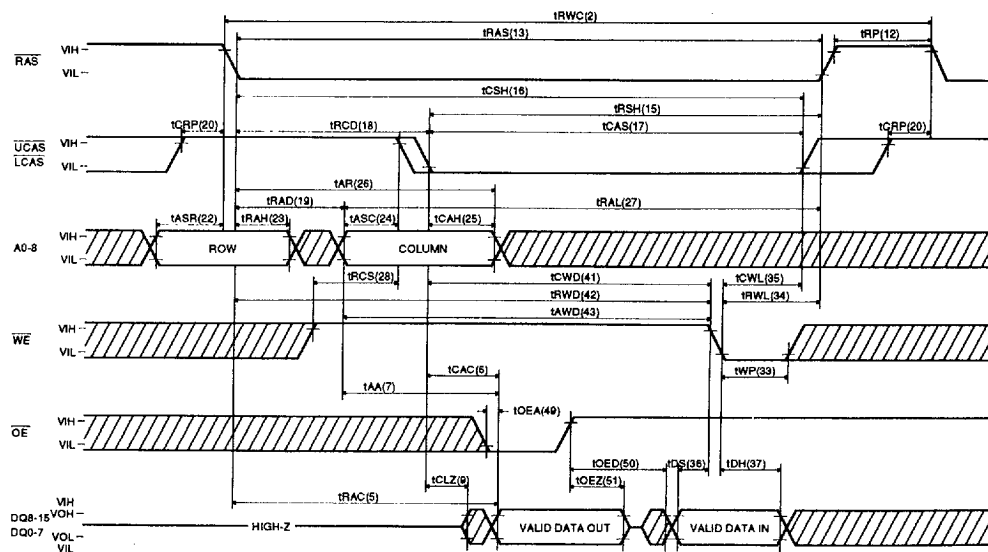
EARLY WRITE CYCLE



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

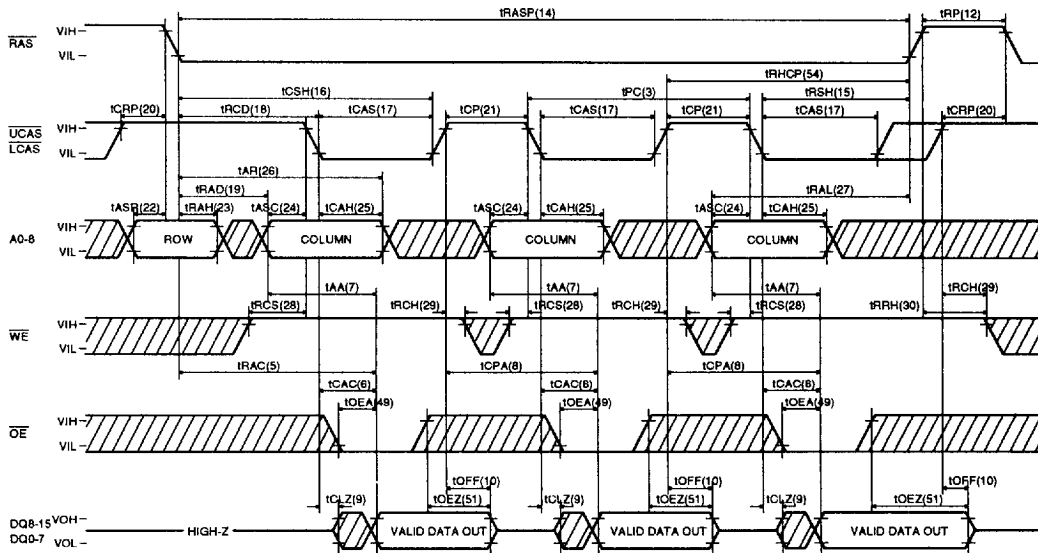


READ-MODIFY-WRITE CYCLE

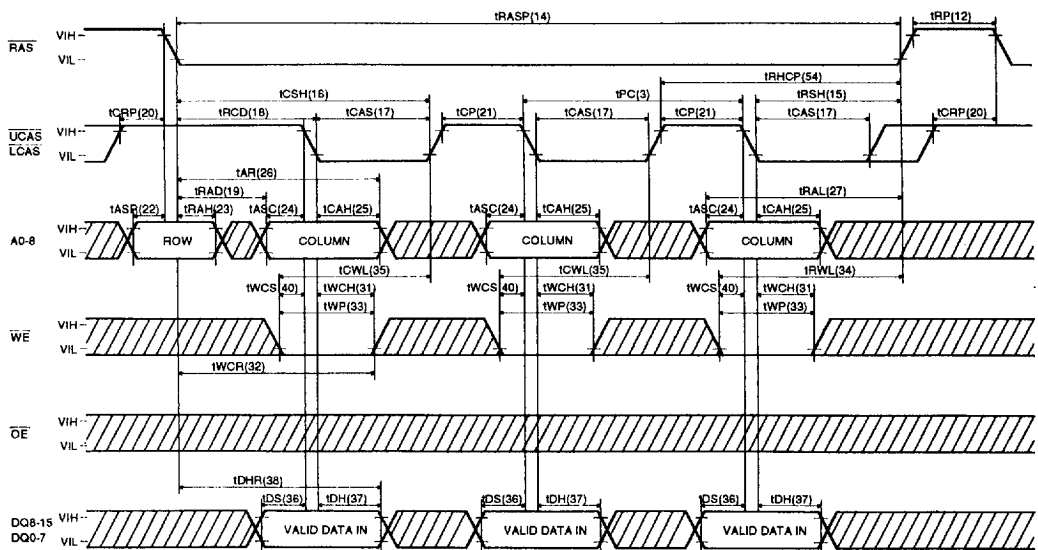


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FAST PAGE MODE READ CYCLE



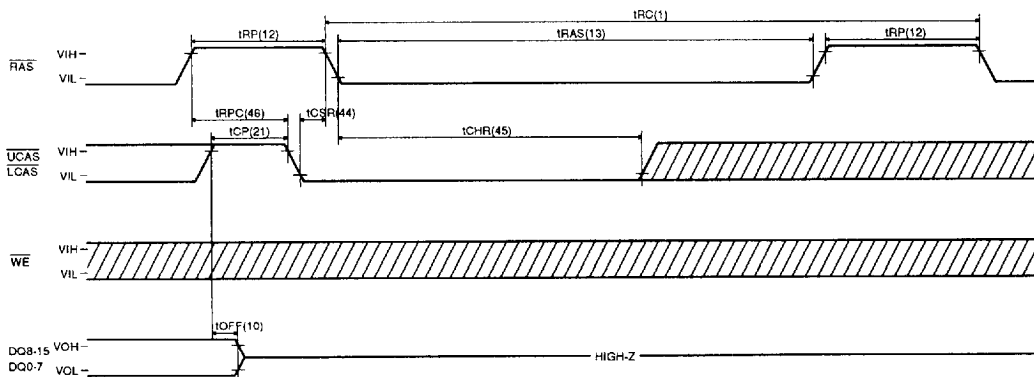
FAST PAGE MODE EARLY WRITE CYCLE



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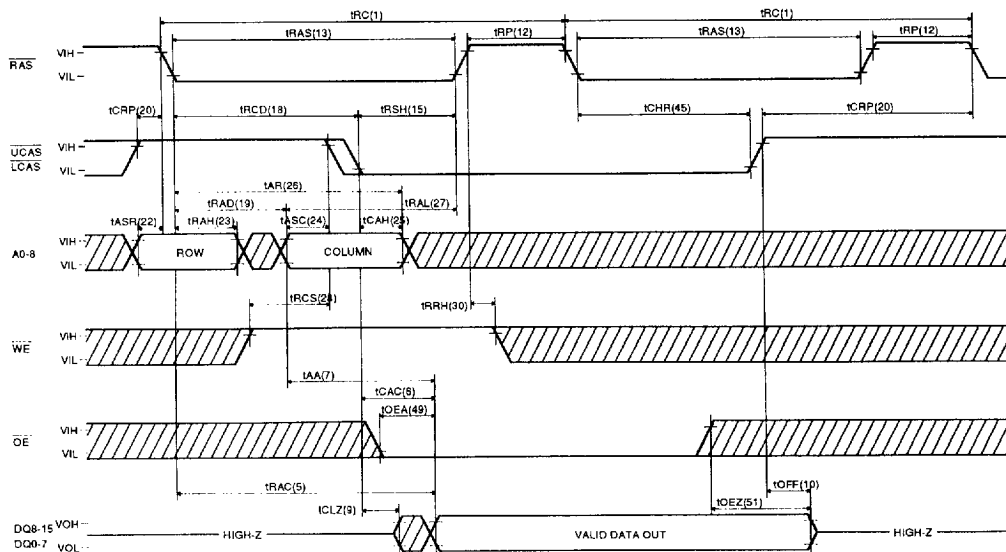
50

CAS-BEFORE-RAS REFRESH CYCLE



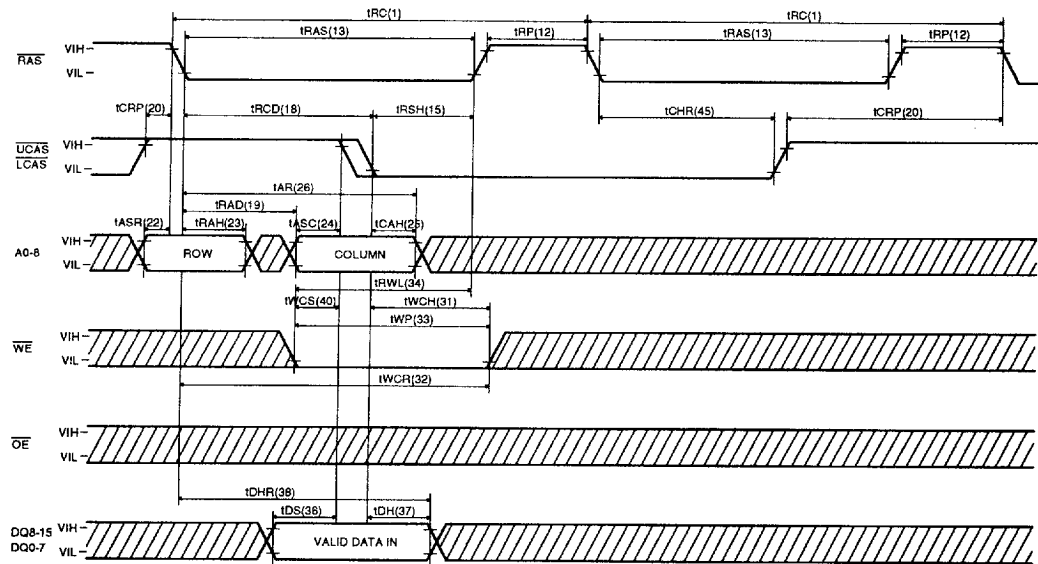
NOTE : A0-8 and OE = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

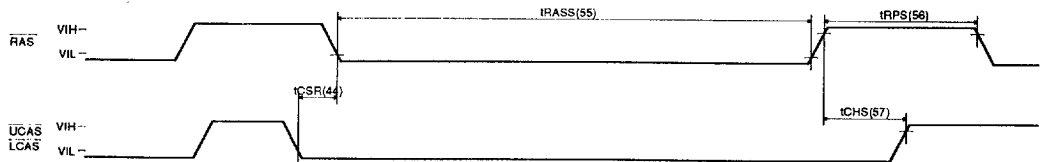


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HIDDEN REFRESH CYCLE (WRITE)

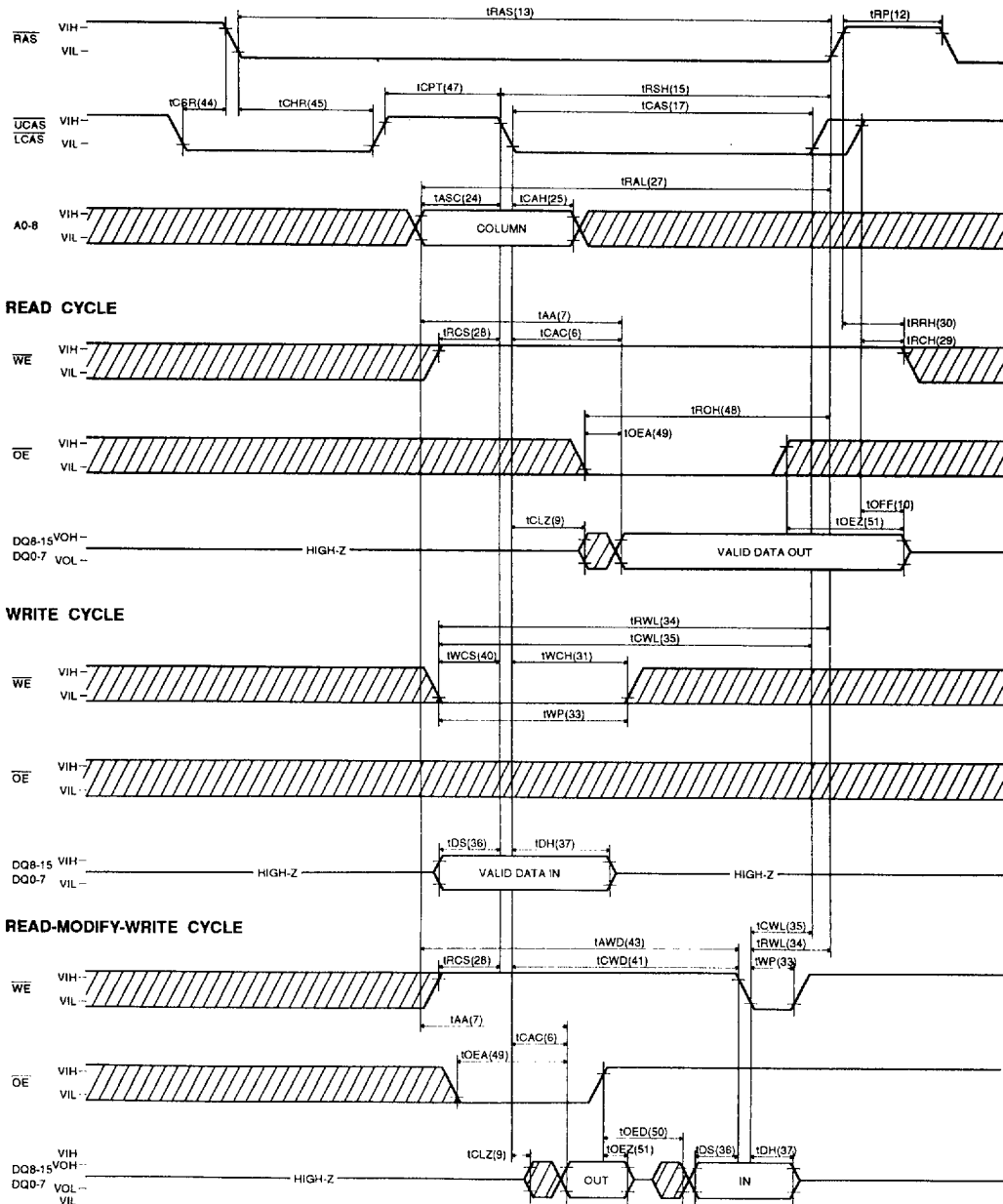


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-8, WE and OE = "H" or "L"

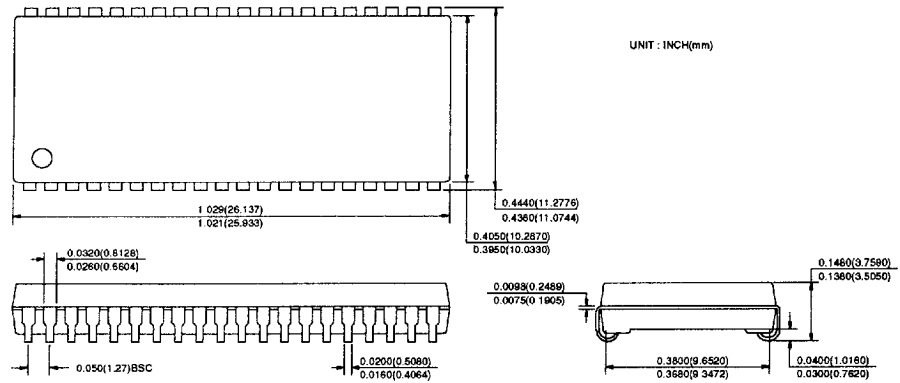
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



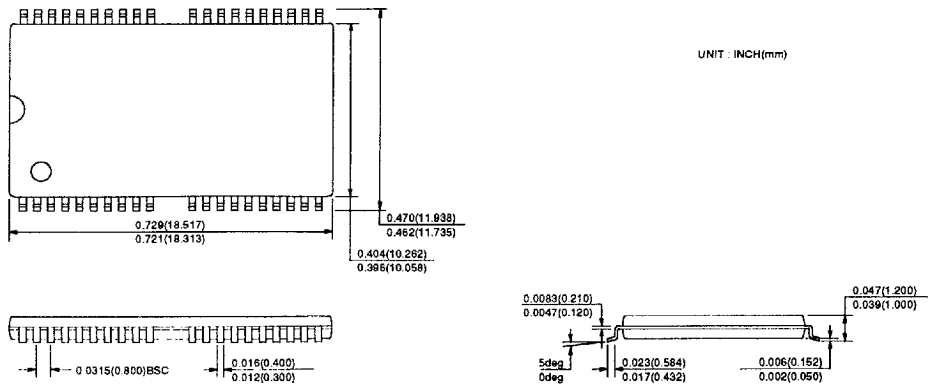
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PACKAGE INFORMATION

400 mil 40 pin Small Outline J-form Package (JC)



400 mil 40/44 pin Thin Small Outline Package (TC) (RC)



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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY512260JC	50/60/70		SOJ
HY512260LJC	50/60/70	L-part	SOJ
HY512260SLJC	50/60/70	SL-part	SOJ
HY512260TC	50/60/70		TSOP-II
HY512260LTC	50/60/70	L-part	TSOP-II
HY512260SLTC	50/60/70	SL-part	TSOP-II
HY512260RC	50/60/70		TSOP-II(R)
HY512260LRC	50/60/70	L-part	TSOP-II(R)
HY512260SLRC	50/60/70	SL-part	TSOP-II(R)