

DESCRIPTION

The HY514410B is the new generation and fast dynamic RAM organized 1,048,576 x 4-bit with function of Write-Per-Bit. The HY514410B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY514410B to be packaged in a standard 20/26 pin plastic SQJ, TSOP-II and Reverse TSOP-II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V± 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
 - Max. battery back-up 1.1mW (L-part)
 - Max. CMOS standby 0.825mW (L-part)
 - 5.5mW
 - Max. TTL standby 11.0mW
 - Max. Self refresh 1.1mW (SL-part)
 - Max. operating

Speed	Power
50	550.0mW
60	495.0mW
70	440.0mW

- Single power supply of 5V± 10%
- TTL compatible inputs and outputs
- Fast access Time

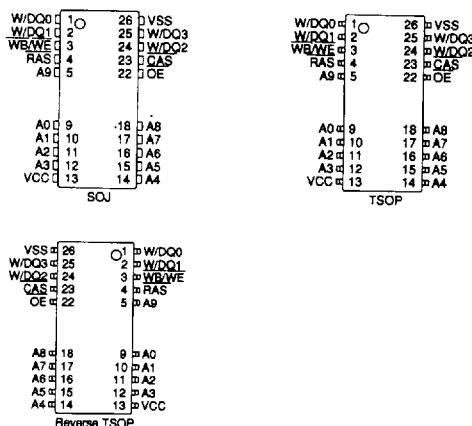
Speed	t _{TRC}	t _{CAC}	t _{PC}
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Fast page mode operation
- Write-Per-Bit and Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self refresh
- 1024 refresh cycles / 128ms (L-part)
- 1024 refresh cycles / 16ms

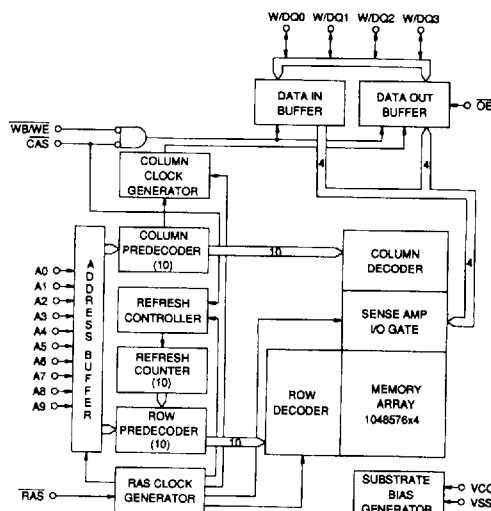
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WB/WE	Write-Per-Bit/Write Enable
OE	Output Enable
A0-A9	Address Input
W/DQ0-W/DQ3	Write Mask/Data IO
Vcc	Power (+ 5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	0.90	W
TSOLDER	Soldering Temperature• Time	260• 10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ 6.5V, All other pins not under test= VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ 5.5V, RAS & CAS at VIH		-10	10	μA	
Icc1	VCC Supply Current, Operating	trC= trC (min.)	50 60 70	- - -	100 90 80	mA	1,2,3
Icc2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	1	mA	
Icc3	VCC Supply Current, RAS-only refresh	trC= trC (min.)	50 60 70	- - -	100 90 80	mA	1,3
Icc4	VCC Supply Current, Fast Page mode	tPC= tPC (min.)	50 60 70	- - -	70 60 50	mA	1,2,3
Icc5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-part	-	1 0.15	mA	5
Icc6	VCC Supply Current, CAS-before-RAS refresh	trC= trC (min.)	50 60 70	- - -	100 90 80	mA	1,3
Icc7	VCC Supply Current, Battery Back Up (L-part only)	trC= 125μs, trAS ≤ 1μs CAS= CBR cycling or 0.2V OE & WE= VCC-0.2V, A0-A9= VCC-0.2V or 0.2V W/DQ0-W/DQ3= 0.2V, VCC-0.2V or open		-	200	μA	1,4,5
Icc8	VCC Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as Icc7		-	200	μA	6
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

- Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
- Icc1, Icc3, Icc4 and Icc6 are dependent on output loading. Specified values are obtained with the output open.
- Icc is specified as average current. Icc1, Icc3, Icc6, Address can be changed maximum two times while RAS= VIH. Icc4, Address can be changed maximum once while CAS= VIH.
- Only trAS(max.)= 1μs is applied to refresh of battery backup but trAS(max.)= 10μs is applied to normal functional operation.
- Icc5(max.)= 0.15mA and Icc7 are applied to L-parts (HY514410BLJ, HY514410BLT, HY514410BLR, HY514100BSLJ, HY514100BSLT, and HY514100BSLR).
- Icc8 is applied to SL-parts only (HY514410BSLJ, HY514410BSLT and HY514410BSLR)

AC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.) NOTE : 1, 2, 3, 13

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE 1, 2, 3, 15										
#	SYMBOL	PARAMETER	HY514410B/J/BT/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	130	-	150	-	180	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns	
5	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	15	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4,15
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	RAS Hold Time	15	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	CAS Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	15	35	15	45	20	50	ns	9
19	tRAD	RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	14
26	tAR	Column Address Hold Time from RAS	40	-	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	14
32	tWCR	Write Command Hold Time from RAS	40	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	15	-	20	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	40	-	50	-	55	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	12
		L-part	-	128	-	128	-	128		11
40	twCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,14

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY514410BJ/BJT/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	35	-	35	-	40	-	ns	8
42	tRWD	RAS to WE Delay Time	70	-	80	-	95	-	ns	8
43	tAWD	Column Address to WE Delay Time	45	-	50	-	60	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	14
47	tCPT	CAS Precharge Time (CBR Counter Test)	25	-	30	-	35	-	ns	17
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	15	-	15	-	20	ns	
50	tOED	OE to Data Delay	15	-	15	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	20	ns	5
52	tOEH	OE Command Hold Time	15	-	15	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	50	-	55	-	65	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	twBS	Write-Per-Bit Set-up Time	0	-	0	-	0	-	ns	
60	twBH	Write-Per-Bit Hold Time	10	-	10	-	10	-	ns	
61	twDS	Write-Per-Bit Selection Set-up Time	0	-	0	-	0	-	ns	
62	twDH	Write-Per-Bit Selection Hold Time	10	-	10	-	10	-	ns	
63	trASS	RAS Pulse Width(Self Refresh)	100	-	100	-	100	-	μs	
64	trPS	RAS Precharge Time(Self Refresh)	120	-	130	-	150	-	ns	
65	tCHS	CAS Hold Time from RAS(Self Refresh)	-50	-	-50	-	-50	-	ns	

AC CHARACTERISTICS IN TEST MODE NOTE 18

#	SYMBOL	PARAMETER	HY514410BJ/BJT/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	135	-	155	-	185	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	85	-	100	-	ns	
5	tRAC	Access Time from RAS	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
13	tRAS	RAS Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	RAS Hold Time	20	-	20	-	25	-	ns	
16	tCSH	CAS Hold Time	55	-	65	-	75	-	ns	
17	tCAS	CAS Pulse Width	20	10K	20	10K	25	10K	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
41	tCWD	CAS to WE Delay Time	40	-	40	-	50	-	ns	8
42	tRWD	RAS to WE Delay Time	75	-	85	-	100	-	ns	8
43	tAWD	Column Address to WE Delay Time	50	-	55	-	65	-	ns	8
49	tOEA	OE Access Time	-	20	-	20	-	25	ns	
50	tOED	OE to Data Delay	20	-	20	-	25	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	20	ns	5
52	tOEH	OE Command Hold Time	20	-	20	-	25	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by any 8 RAS only or CAS-before-RAS refresh cycle before proper device operation is achieved.
2. If RAS= Vss during power-up, the HY514410B could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured at VOH= 2.4V and VOL= 0.4V with a load equivalent to 2 TTL loads and 100pF.
5. toFF(max.) and toEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WB/WE leading edge in Read-Modify-Write cycles.
8. twCS, trWD, tcWD, tAWD and tcpWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If trWD $\geq$ trWD(min.), tcWD $\geq$ tcWD(min.), tAWD $\geq$ tAWD(min.), and tcpWD $\geq$ tcpWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)= 128ms is applied to L-Parts (HY514410BLJ/BSLJ, HY514410BLT/BSLT and HY514410BLR/BSLR).
12. A burst of 1024CAS-before-RAS refresh cycles must be executed within 16ms(128ms for L-part) after exiting self refresh.
13. When CAS goes low, 4-bits data are written into the device.
14. These parameters are determined by the earlier falling edge of CAS.
15. These parameters are determined by the later rising edge of CAS.
16. tcWL must be satisfied by CAS for 4-bits access cycles.
17. tCP and tCPT are measured when CAS is high state.
18. These specifications are applied to the test Mode.

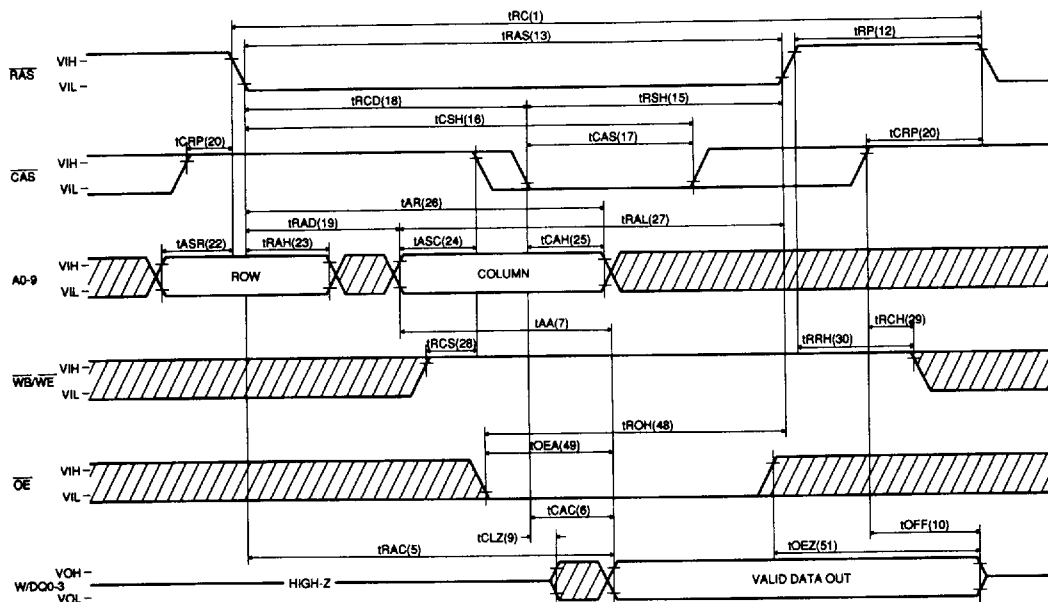
CAPACITANCE

(TA= 25°C, VCC= 5V $\pm$ 10%, VSS= 0V, f= 1MHz, unless otherwise noted.)

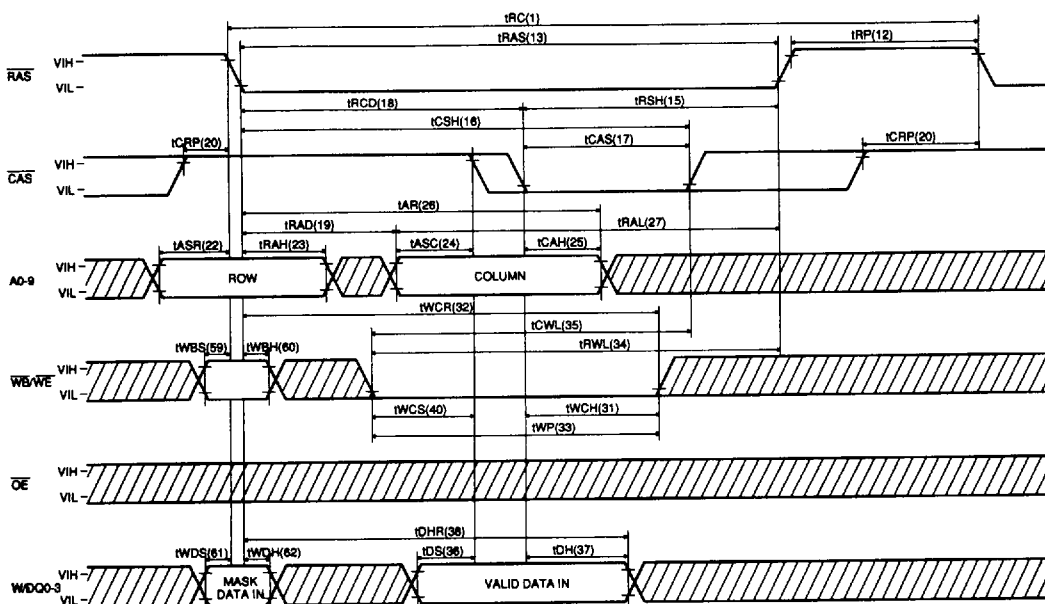
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	5	pF
CIN2	Input Capacitance (RAS, CAS, WB/WE, OE)	-	7	pF
CdQ	Data Input/Output Capacitance (W/DQ0-W/DQ3)	-	7	pF

TIMING DIAGRAM

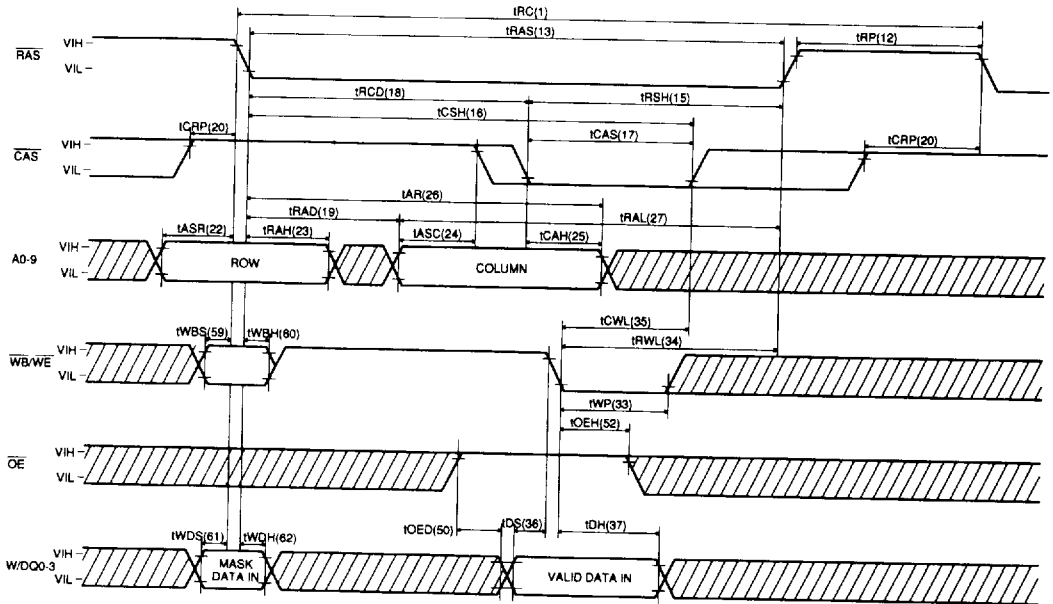
READ CYCLE



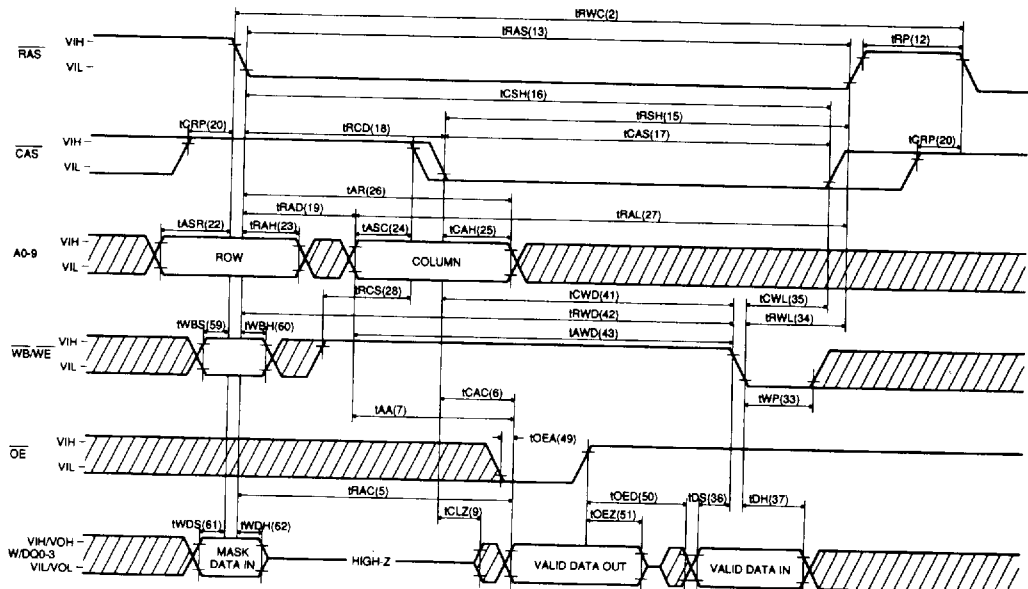
EARLY WRITE CYCLE



WRITE CYCLE (OE CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



The timing diagram illustrates the relationship between several input signals and the internal state of the 74VHC00-3 device. The signals shown are:

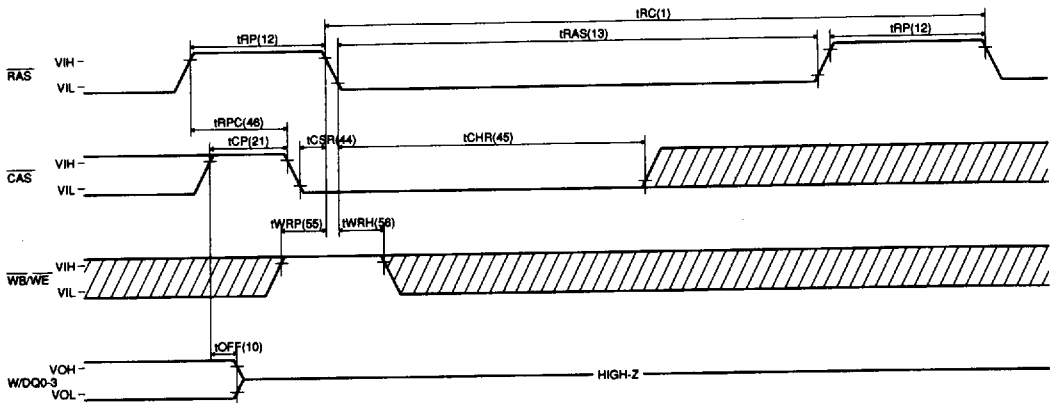
- RAS**: Random Access Strobe, active low.
- CAS**: Column Address Strobe, active low.
- A0-9**: Data bus address lines.
- WB/WE**: Write Buffer/Write Enable, active low.
- OE**: Output Enable, active low.
- VIH/VOH**: High-level voltage inputs/outputs.
- VIL/VOL**: Low-level voltage inputs/outputs.
- MASK DATA IN**: Mask data input signal.
- OUT**: Output signal.
- IN**: Input signal.

The diagram includes numerous timing parameters labeled with t and a subscript indicating the specific transition or condition. Key parameters include:

- tRSP(14)**: RAS pulse width.
- tIRP(12)**: RAS precharge time.
- tICSH(18)**: CAS-to-RAS setup time.
- tICSD(18)**: CAS-to-RAS delay time.
- tCAS(17)**: CAS pulse width.
- tICP(21)**: CAS-to-output propagation delay.
- tIGAS(17)**: CAS-to-output gate delay.
- tIPWC(4)**: CAS-to-output precharge delay.
- tIRSH(15)**: RAS-to-output setup time.
- tICAS(17)**: RAS-to-output delay time.
- tICRP(20)**: RAS-to-output recovery time.
- tAR(26)**: Address-to-output delay time.
- tRAD(19)**: Row Address Delay.
- tIAH(23)**: Internal Address Hold.
- tASC(24)**: Address-to-column select delay.
- tCAH(25)**: Column Address Hold.
- tIWD(42)**: Word Delay.
- tAWD(43)**: Array Word Delay.
- tCWL(35)**: Column Word Latency.
- tIW(33)**: Input Word Delay.
- tAA(7)**: Address-to-array access delay.
- tCAC(8)**: Column Access Delay.
- tIOEA(48)**: Input/Output Enable-to-array access delay.
- tIOEZ(51)**: Input/Output Enable-to-output enable delay.
- tIOED(50)**: Input/Output Enable-to-output delay.
- tWDS(61)**: Write Data Setup.
- tWDH(62)**: Write Data Hold.
- tCLZ(9)**: Column Latency.
- tDS(36)**: Data Setup.
- tDH(37)**: Data Hold.
- tICLZ(9)**: Input Column Latency.

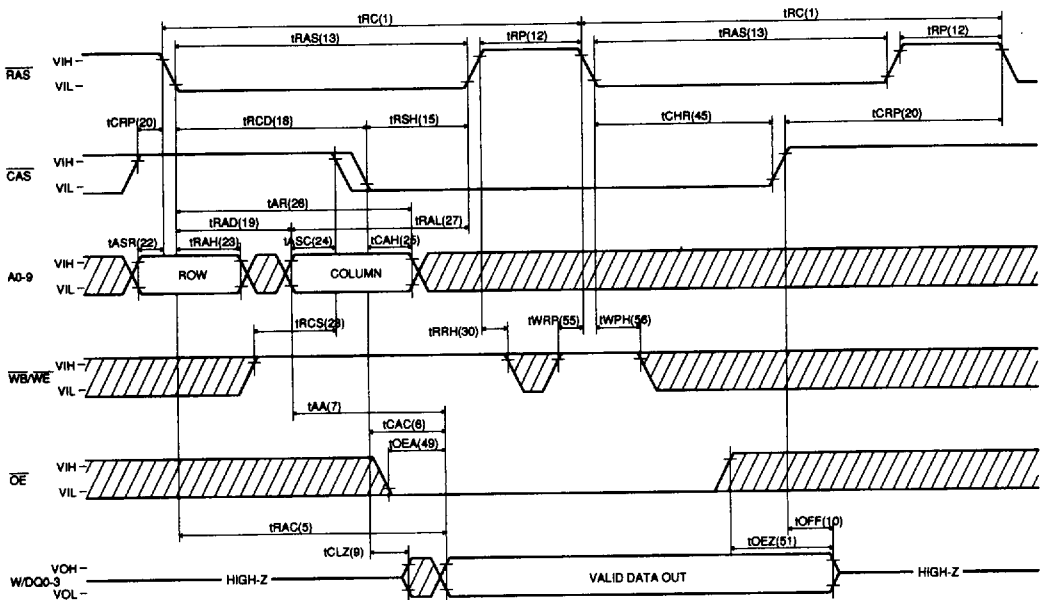
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CAS-BEFORE-RAS REFRESH CYCLE

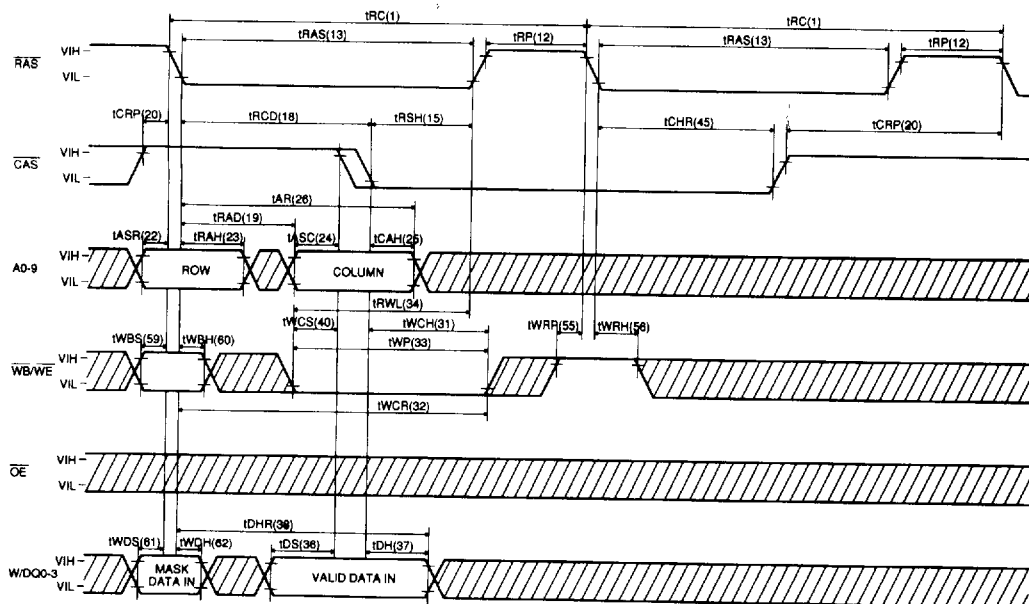


NOTE : A0-9 and OE = "H" or "L"

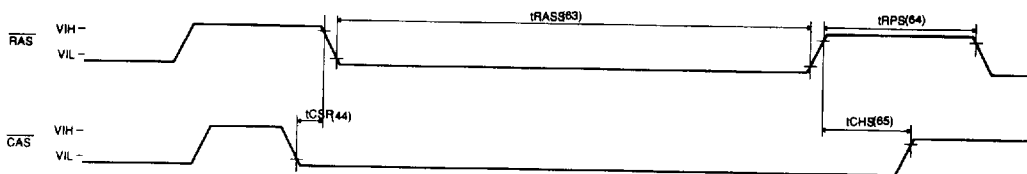
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

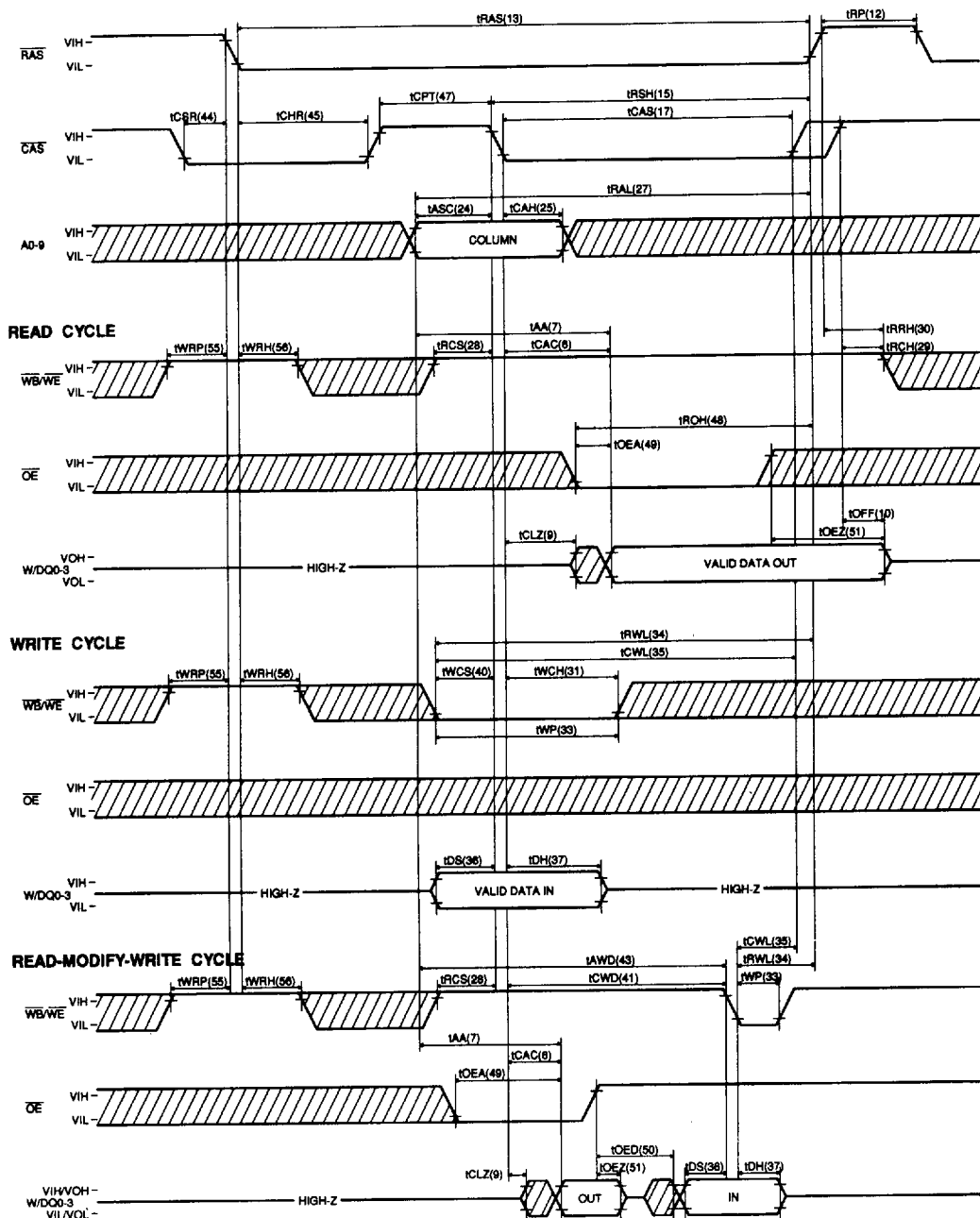


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-9, $\overline{WB/WE}$ and $\overline{OE}$ = "H" and "L"

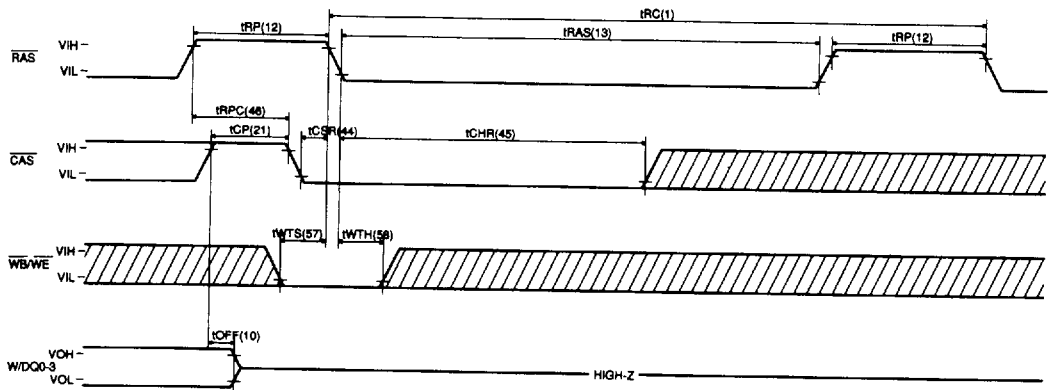
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



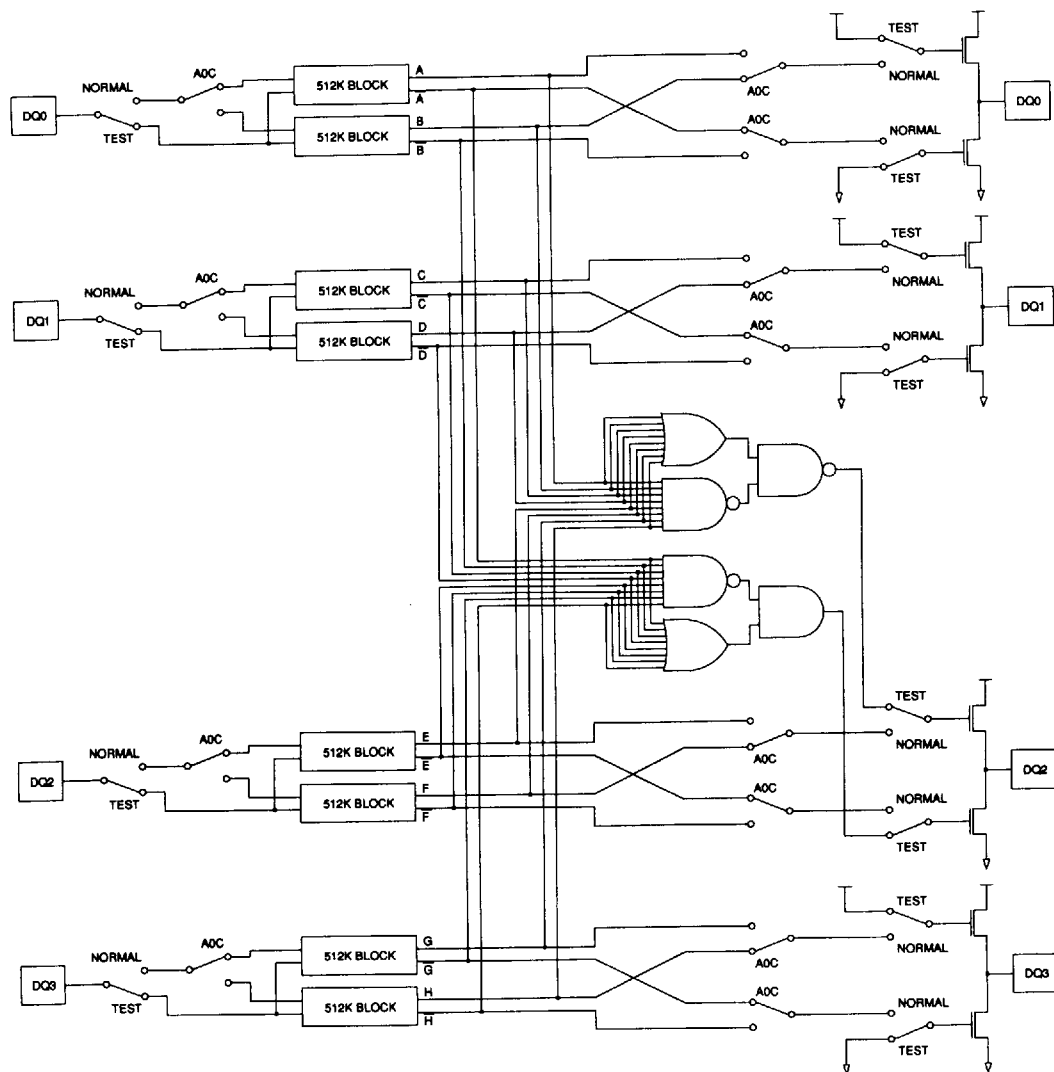
TEST MODE

The HY514410B is a DRAM organized 1,048,576 x 4-bit. It is internally organized 524,288 x 8-bit. In Test Mode, data are written into 8 sectors (Each is composed of 512K bits) in parallel and retrieved the same way. Column address A0 is not used. If, upon reading, all 8-bit data from 8 sectors are equal (all "1"s or "0"s), the DQ2 pin indicates a "1". If they are not equal, the DQ2 pin indicates a "0". The DQ0, DQ1 and DQ3 pins always indicate a "1" in Test Mode Read cycles. The diagram below shows the timing of the HY514410B to enter Test Mode. In Test Mode, the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. WE, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY514410B into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time.(1/2 in case of N test pattern)

TEST MODE IN CYCLE



BLOCK DIAGRAM IN TEST MODE



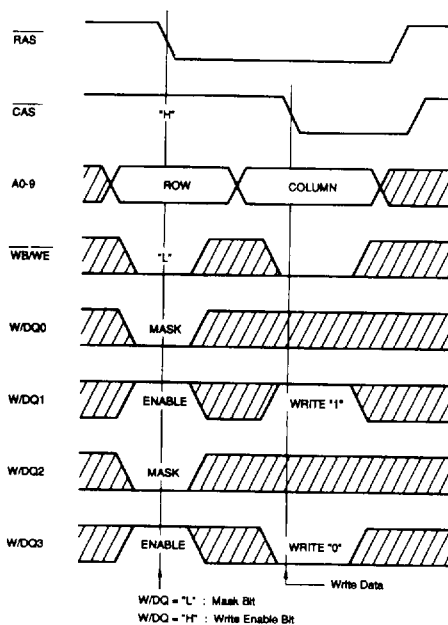
WRITE-PER-BIT FUNCTION

The Write-Per-Bit function selectively controls the internal write enable circuit of the HY514410B. When **WB/WE** is held "Low" at the falling edge of **RAS** during a random access operation, the write mask is enabled. At the same time, the mask data on the **W/DQ** pins is located onto the write mask register (WMR). When a "0" is sensed on any of the **W/DQ** pins, their corresponding write circuits are disabled and new data will not be written. When "1" is sensed on any of the **W/DQ** pins, their corresponding write circuit will remain enabled so that new data is written. The truth table of the Write-Per-Bit function and an example of the Write-Per-Bit function illustrating its application to displays are shown below.

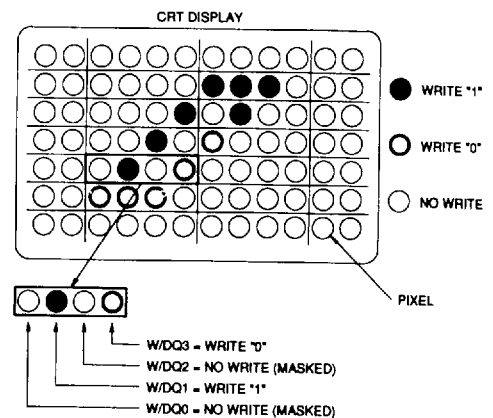
TRUTH TABLE FOR WRITE-PER-BIT FUNCTION

at the falling edge of RAS			Function
CAS	WB/WE	W/DQ0-3	
H	H	Don't Care	Write Enable
H	L	1	Write Enable
		0	Write Mask

WRITE-PER-BIT TIMING DIAGRAM

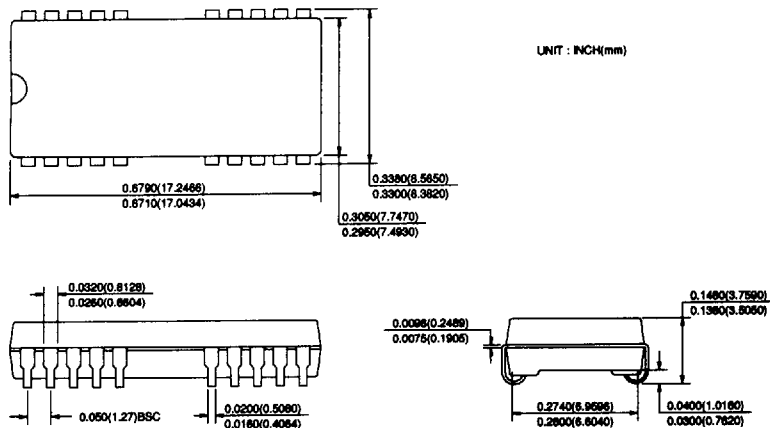


CORRESPONDING BIT MAP

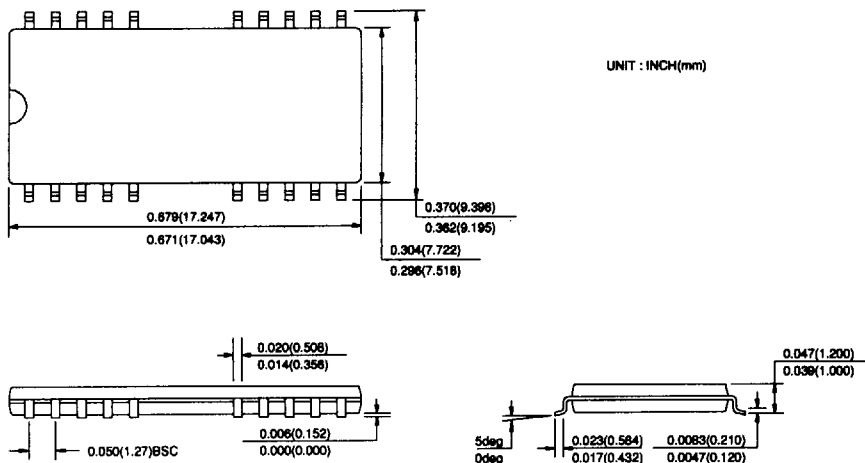


PACKAGE INFORMATION

300 mil 20/26 pin Small Outline J-form Package (J)



300 mil 20/26 pin Thin Small Outline Package (T) (R)

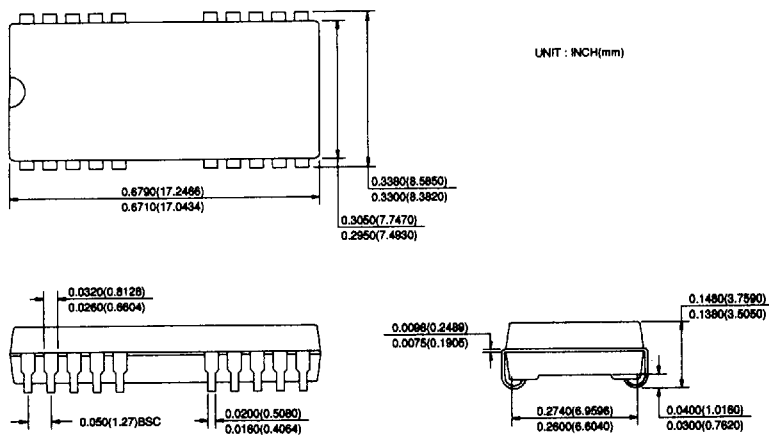


ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY514410BJ	50/60/70		SOJ
HY514410BLJ	50/60/70	L-part	SOJ
HY514410BSLJ	50/60/70	SL-part	SOJ
HY514410BT	50/60/70		TSOP-II
HY514410BLT	50/60/70	L-part	TSOP-II
HY514410BSLT	50/60/70	SL-part	TSOP-II
HY514410BR	50/60/70		TSOP-II(R)
HY514410BLR	50/60/70	L-part	TSOP-II(R)
HY514410BSLR	50/60/70	SL-part	TSOP-II(R)

PACKAGE INFORMATION

300 mil 20/26 pin Small Outline J-form Package (J)



300 mil 20/26 pin Thin Small Outline Package (T) (R)

