HYUNDAI SEMICONDUCTOR

HY51C256/L

256K × 1-Bit CMOS Dynamic RAM

OCTOBER 1986

DESCRIPTION

The HY51C256/L is a high speed 262,144×1-bit dynamic Random Access Memory. Fabricated with Hyundai's HYCMOS technology, the HY51C256/L offers features not provided by any NMOS dynamic RAM: Ripplemode* for high data bandwidth, fast usable speed and CMOS standby current. All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

Ripplemode* operation allows random or sequential access of up to 512 bits within a row, with cycle times as fast as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is no longer in the critical timing path. The flow-through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the HY51C256/L ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance micro-processor systems.

The HY51C256L offers a typical standby current as low as 10μA when $\overline{RAS} \geq V_{DD}-0.2V$. During standby (i.e. only refresh cycles) the refresh period can be extended to 32 ms to reduce the total power required for data retention to less than 425μW. The HY51C256L combines low power with high density for portable and battery back-up applications.

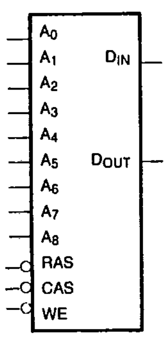
FEATURES

- ▲ **Ripplemode* Operation**
  - **—Continuous data rate up to 20MHz**
  - **—Random access within row**
  - **—Flow-through column latch for pipelining**
- ▲ **Low Input/Output Capacitance**
- ▲ **TTL Compatible**
- ▲ **Low Power Data Retention—HY51C256L**
  - **—Standby current, CMOS—100μA (max.)**
  - **—Refresh period, $\overline{RAS}$-Only-32 ms (max.)**
  - **—Data Retention Current—200μA (max.)**
- ▲ **Low Operating Current—40mA (max.)**
- ▲ **$\overline{RAS}$-Only Refresh, Hidden Refresh**
- ▲ **High Reliability Plastic 16 Pin DIP**

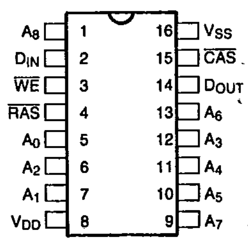
***Ripplemode is a registered trademark of Intel corporation**

	HY51C256/L-10	HY51C256/L-12	HY51C256/L-15	HY51C256/L-20
Maxmum Access Time (ns)	100	120	150	200
Maximum Access Time From $\overline{CAS}$ (ns)	15	20	25	30
Minimum Cycle Time (ns)	170	200	240	310
Ripplemode Cycle Time (ns)	50	60	70	90
Maximum CMOS Standby Current (mA)	2/0.1	2/0.1	2/0.1	2/0.1

LOGIC SYMBOL



PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A_0-A_8	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	Power (+5V)
V_{SS}	Ground

This documentation is a general product description and is subject to change without notice. Hyundai Semiconductor does not assume any responsibility for use of circuits described. No circuit patent licenses are implied.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	−10° to +80°C
Storage Temperature	Plastic −55°C to +125°C
Voltage on Any Pin except V_{DD} Relative to V_{SS}	−1.0V to 7.5V
Voltage on V_{DD} Relative to V_{SS}	−1.0V to 7.5V
Voltage on D_{OUT} Relative to V_{SS}	−2.0V to V_{DD} +1V
Data Out Current	50mA
Power Dissipation	1.0W

Stresses above those listed under "Absolute Maximum Ratings" might cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.

D.C. CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	SPEED	HY51C256/L Min.	Typ[2]	Max.	UNIT	TEST CONDITIONS	NOTE
I_{DD1}	V_{DD} Supply Current, Operating	−10		/48	70/65	mA	$t_{RC}=t_{RC}$ (min.)	3.4
		−12		/42	60/55			
		−15		/35	50/45			
		−20		/30	45/40			
I_{DD2}	V_{DD} Supply Current, TTL Standby			10.5	4/2	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, all other inputs ≥ −0.5V	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	−10			70/65	mA	$t_{RC}=t_{RC}$ (min.)	4
		−12			60/55			
		−15			50/45			
		−20			45/40			
I_{DD4}	V_{DD} Supply Current, Ripplemode	−10		/22	70/65	mA	$t_{PC}=t_{PC}$ (min.)	3,4
		−12		/21	60/55			
		−15		/20	50/45			
		−20		/19	45/40			
I_{DD5}	V_{DD} Supply Current, TTL Standby, Output Enabled			/1	6/4	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs ≥ −0.5V	3
I_{DD6}	V_{DD} Supply Current, CMOS Standby			/0.01	2/0.1	mA	$\overline{RAS}$ ≥ V_{DD}−0.2V and $\overline{CAS}$ at V_{IH} all other inputs ≥ −0.5V	
$\|I_{LI}\|$	Input Load Current (any pin)				10	μA	$V_{IN}=V_{SS}$ to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State				10	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, D_{OUT} $=V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)		−1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)		2.4		V_{DD}+1	V		5
V_{OL}	Output Low Voltage				0.4	V	I_{OL}=4.2 mA	6
V_{OH}	Output High Voltage		2.4			V	I_{OH}=−5 mA	6

NOTES:

1. All voltages referenced to V_{SS}.
2. Typical values are at T_A=25°C and V_{DD}= +5V.
3. I_{DD} is dependent on output loading when the device output is selected. I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Ripplemode*, etc.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH}(max) ≤ V_{DD}.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, D_{IN}	4	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	3	4	pF
C_{OUT}	D_{OUT}	4	6	pF

NOTES:
†Capacitance is sampled and not 100% tested.

A.C. CHARACTERIST CS[1,2,3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

#	JEDEC SYMBOL	SYMBOL	PARAMETER	HY51C256/L-10		HY51C256/L-12		HY51C256/L-15		HY51C256/L-20		UNIT	NOTES
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	150	75000	200	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	170		200		240		310		ns	
3	5_{RH2RL2}	5_{RP}	$\overline{RAS}$ Percharge Time	60		70		80		100		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	100		120		150		200		13	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	25	75000	25	75000	30	75000	35	75000	ns	
6	t_{WH2RL2}	t_{WRP}	Write to $\overline{RAS}$ Precharge Time	—		—		—		—		ns	4
7	t_{RL1WL2}	t_{RWH}	$\overline{RAS}$ to Write Hold Time	—		—		—		—		ns	4
8	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold time	15		15		20		25		ns	
10	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
11	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		−20		ns	
12	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	85	25	100	30	125	35	170	ns	5
13	t_{AVCL2}	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
14	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		20		20		25		ns	
15	t_{RL1AX}	t_{AR}	Column Address Hold Time From $\overline{RAS}$	55		60		70		80		ns	
	t_{RVRV}	t_{REF1}	Refresh Time		4		4		4		5	ms	6
	t_{RVRV}	t_{REF2}	Refresh Time ($\overline{RAS}$-Only)		32		32		32		32	ms	6
	t_T	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	3	25	ns	7
16	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0		0		0		0		ns	
17	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	5	20	5	25	5	25	5	30	ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as a $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).
3. A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, $V_{IL}(min) \geq V_{SS}$ and $V_{IH}(max) \leq V_{DD}$.
4. Timing parameters t_{WRP} and t_{RWH}, referenced to $\overline{RAS}$, are redundant on the HY51C256/L and not specified in the data sheets.
5. t_{RCD} (max) is for reference only.
6. The HY51C256L extends the refresh period to 32ms during $\overline{RAS}$-only refresh operation.
7. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. CHARACTERISTICS (CONT'D.)

READ CYCLE

#	JEDEC SYMBOL	SYMBOL	PARAMETER	HY51C256/L-10		HY51C256/L-12		HY51C256/L-15		HY51C256/L-20		UNIT	NOTES
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
18	t_{RLIQV}	t_{RAC}	Access Time From $\overline{RAS}$		100		120		150		200	ns	8
19	t_{CLIQV}	t_{CAC}	Access Time Frim $\overline{CAS}$		15		20		25		30	ns	9, 10
20	t_{AVQV}	t_{CAA}	Access Time From Column Address		40		50		60		80	ns	10
21	t_{CLIRHI}	$t_{RSH(R)}$	$\overline{RAS}$ Hold time (Read Cycle)	10		10		10		10		ns	
22	t_{WH2CL2}	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
23	t_{AVRHI}	t_{CAR}	Colum Address to $\overline{RAS}$ Set-up Time	45		50		60		80		ns	
24	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	11
25	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{CAS}$	10		10		10		10		ns	11

WRITE CYCLE

#	JEDEC SYMBOL	SYMBOL	PARAMETER	HY51C256/L-10		HY51C256/L-12		HY51C256/L-15		HY51C256/L-20		UNIT	NOTES
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
26	$t_{CLIRHI(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	25		30		35		40		ns	
27	t_{WLIRHI}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		35		40		ns	
28	t_{WLICHI}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		35		40		ns	
29	t_{WLIWHI}	t_{WP}	Write Command Pulse Width	20		20		25		30		ns	
30	t_{WLICL2}	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	12
31	t_{CLIWHI}	t_{WCH}	Write Command Hold Time	20		25		30		35		ns	
32	t_{DVCL2}	t_{DS}	Data-In Set-up Time	0		0		0		0		ns	
33	t_{CLIDX}	t_{DH}	Data-In Hold Time	20		25		25		30		ns	

NOTES:

8. Assumes that $t_{RCD} \leq t_{RCD}$(max). If $t_{RCD} > t_{RCD}$ (max), then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
9. Assumes $t_{RCD} \geq t_{RCD}$(max).
10. If $t_{ASC} < (t_{CAA}(max) - t_{CAC}(max) - t_T)$, then access time is defined by t_{CAA} rather than by t_{CAC}.
11. Either t_{RCH} or t_{RRH} must be satisfied.
12. t_{WCS}, t_{RWD}, t_{CWS} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the D_{OUT} pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-modify-write cycle and the data out will present the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (CONT'D.)

READ/MODIFY/WRITE CYCLE[12]

#	JEDEC SYMBOL	SYMBOL	PARAMETER	HY51C256/L-10		HY51C256/L-12		HY51C256/L-15		HY51C256/L-20		UNIT	NOTES
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
34	$t_{RL2RL2(RMW)}$	t_{RWC}	Read/Modify/Write (RMW) Cycle Time	200		235		280		355		ns	
35	$t_{RL1RH1\ (RMW)}$	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	130	75000	155	75000	185	75000	240	75000	ns	
36	$t_{CL1CH1\ (RMW)}$	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	55		60		65		75		ns	
37	t_{RL1WLw}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		150		200		ns	12
38	t_{CL1SL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20		30		30		35		ns	12
39	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	50		60		70		90		ns	12

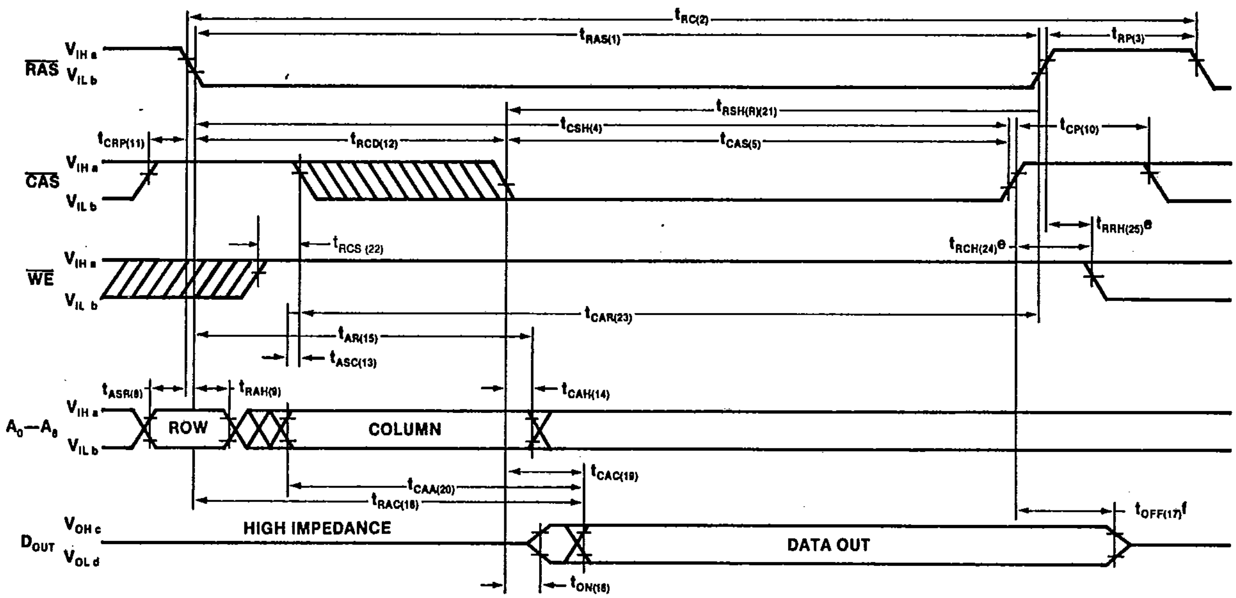
RIPPLEMODE* CYCLE[14]

#	JEDEC SYMBOL	SYMBOL	PARAMETER	HY51C256/L-10		HY51C256/L-12		HY51C256/L-15		HY51C256/L-20		UNIT	NOTES
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{CH2QV}	t_{CAP}	Access Time From Column Precharge		45		55		65		85	ns	13
41	$t_{CL2CL2(R)}$	t_{PC}	Ripplemode Read or Write Cycle	50		60		70		90		ns	13
42	$t_{CL2CL2(RRMW)}$	t_{PCM}	Ripplemode RMW Cycle Time	80		90		105		135		ns	

NOTES:

13. Access time is determined by the longer of t_{CAA} or t_{CAC} or t_{CAP}.

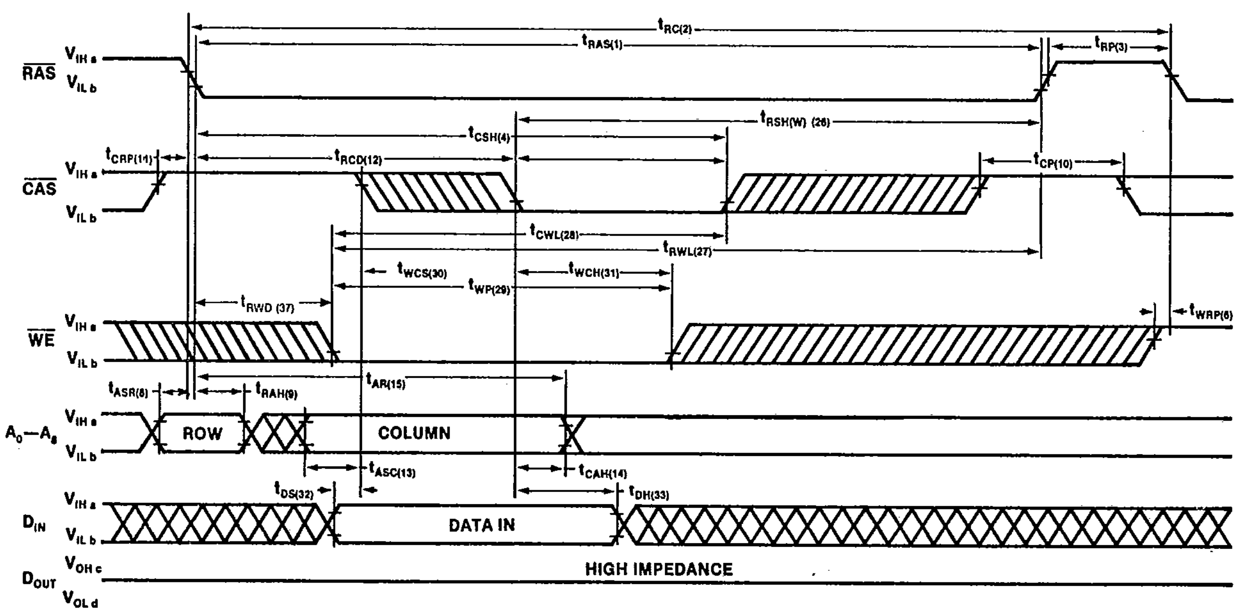
READ CYCLE



NOTES:

a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. Either t_{RCH} or t_{RRH} must be satisfied.
f. t_{OFF} is measured to $I_{OUT} \leq I_{LO}$.

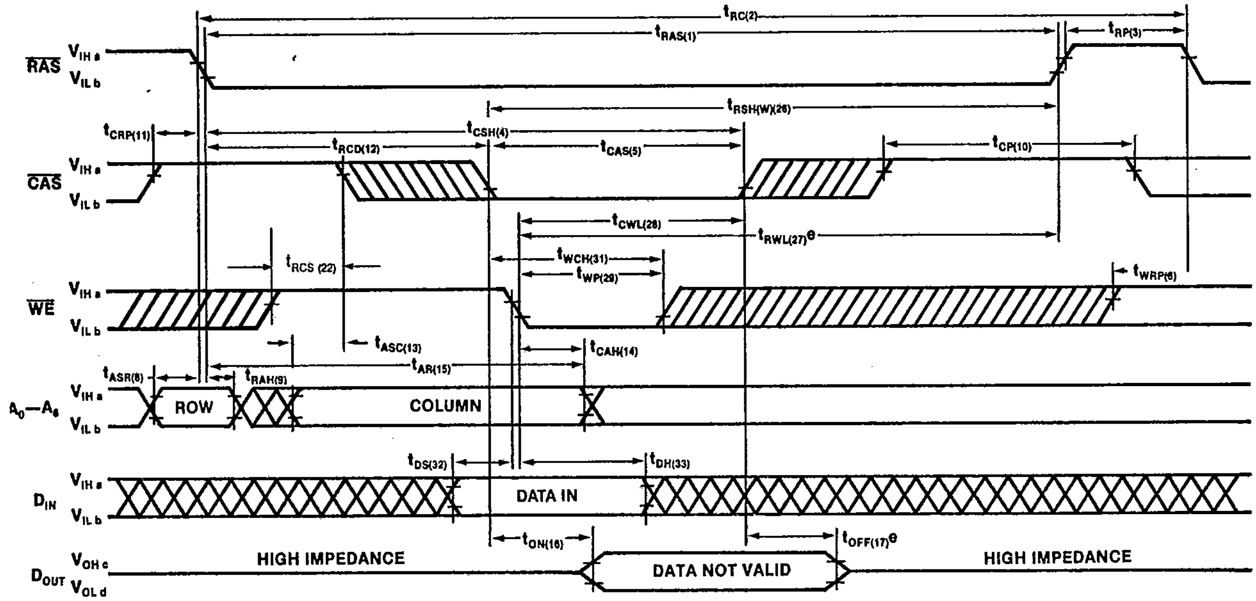
WRITE CYCLE (CAS CONTROLLED)[e]



NOTES:

a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. WE is low prior to or simultaneously with CAS low transition. CAS latches column addresses and D_{IN}

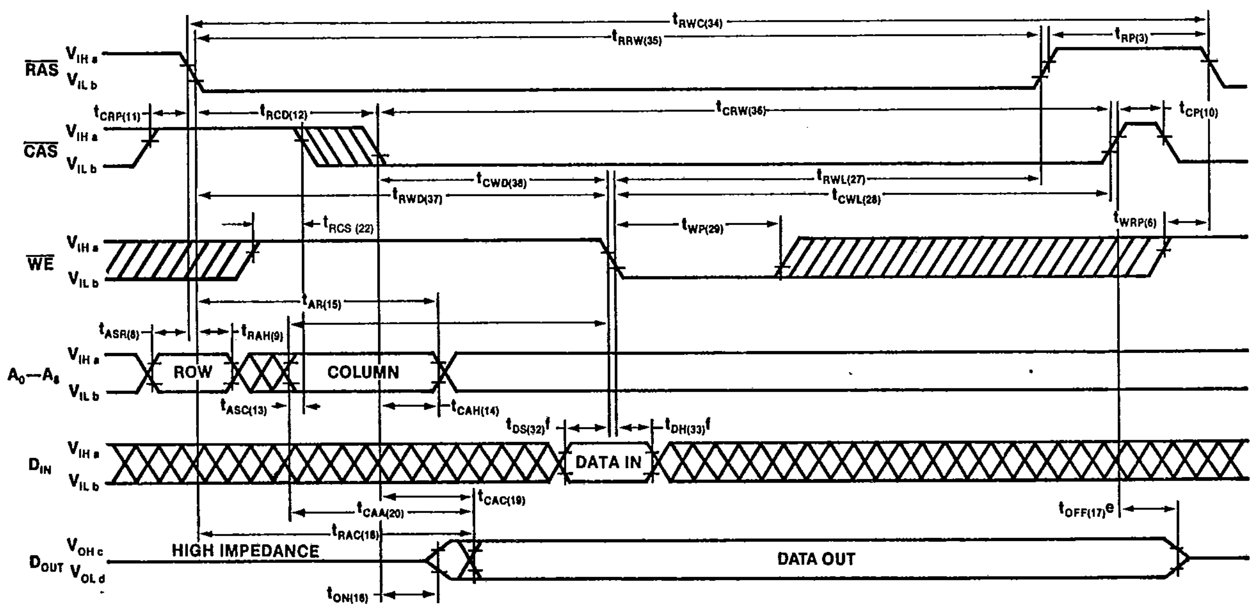
WRITE CYCLE ($\overline{WE}$ CONTROLLED)[f]



NOTES:

a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to $\overline{WE}$ low transition. $\overline{CAS}$ latches the column addresses while $\overline{WE}$ latches the D_{IN}

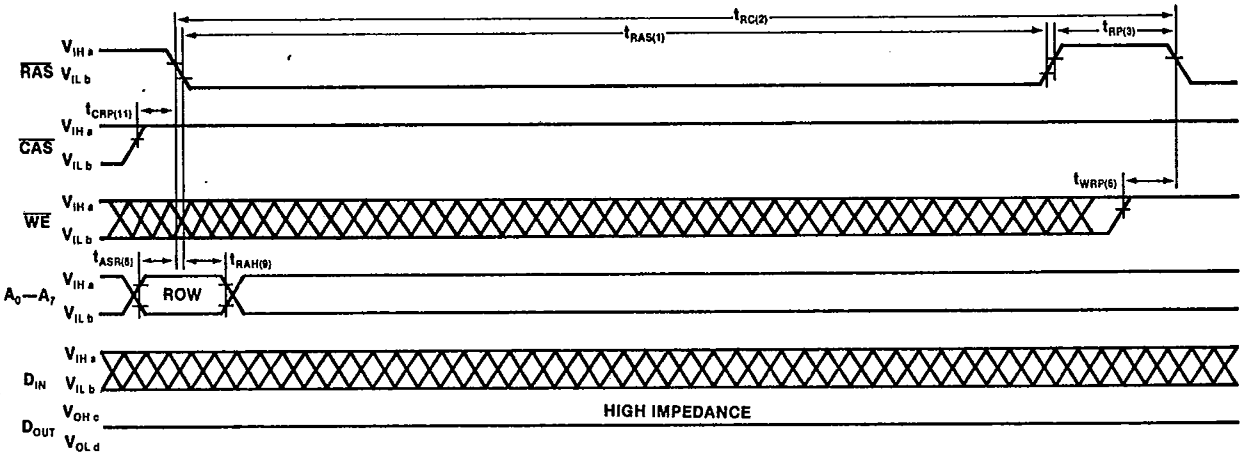
READ/MODIFY/WRITE CYCLE



NOTES:

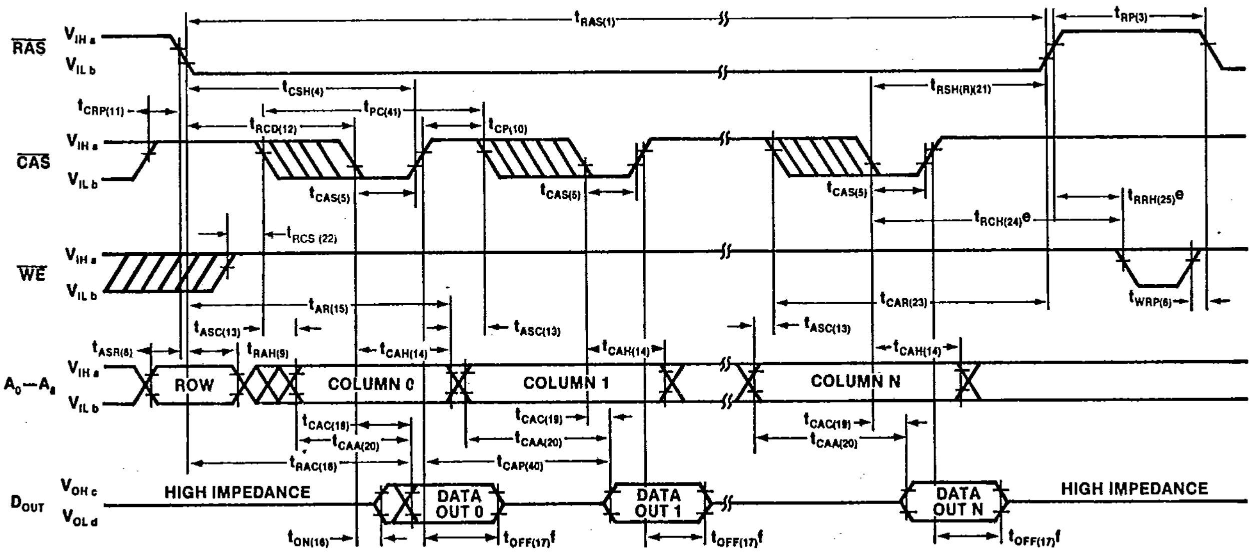
a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

$\overline{RAS}$-ONLY REFRESH CYCLE



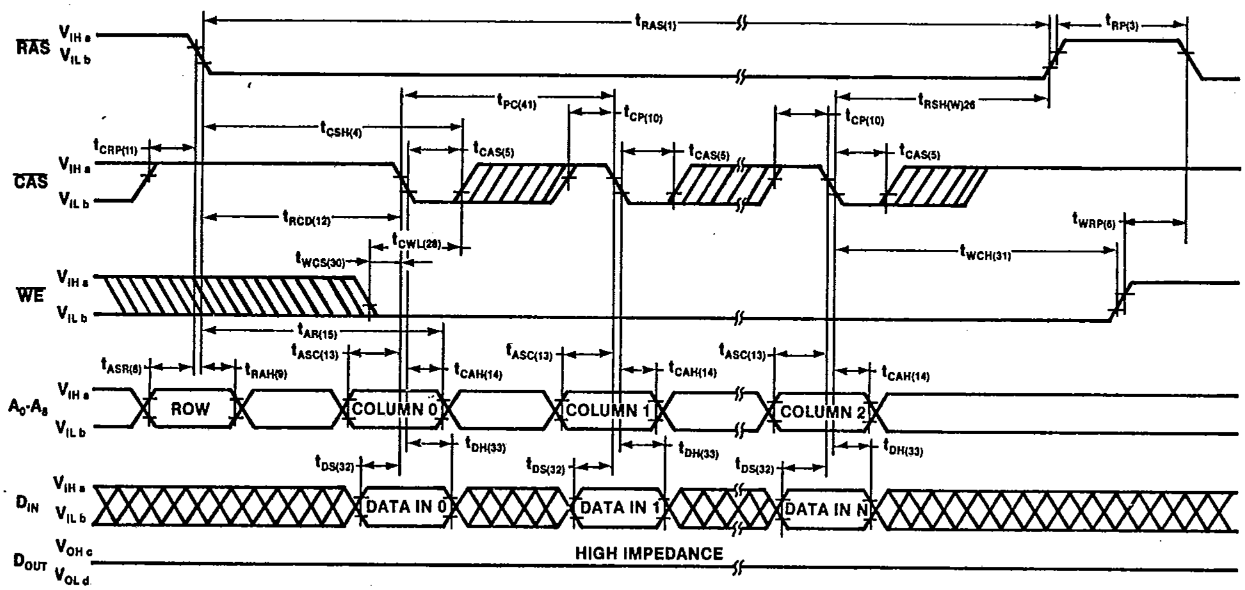
NOTES:
a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

RIPPLEMODE* READ CYCLE



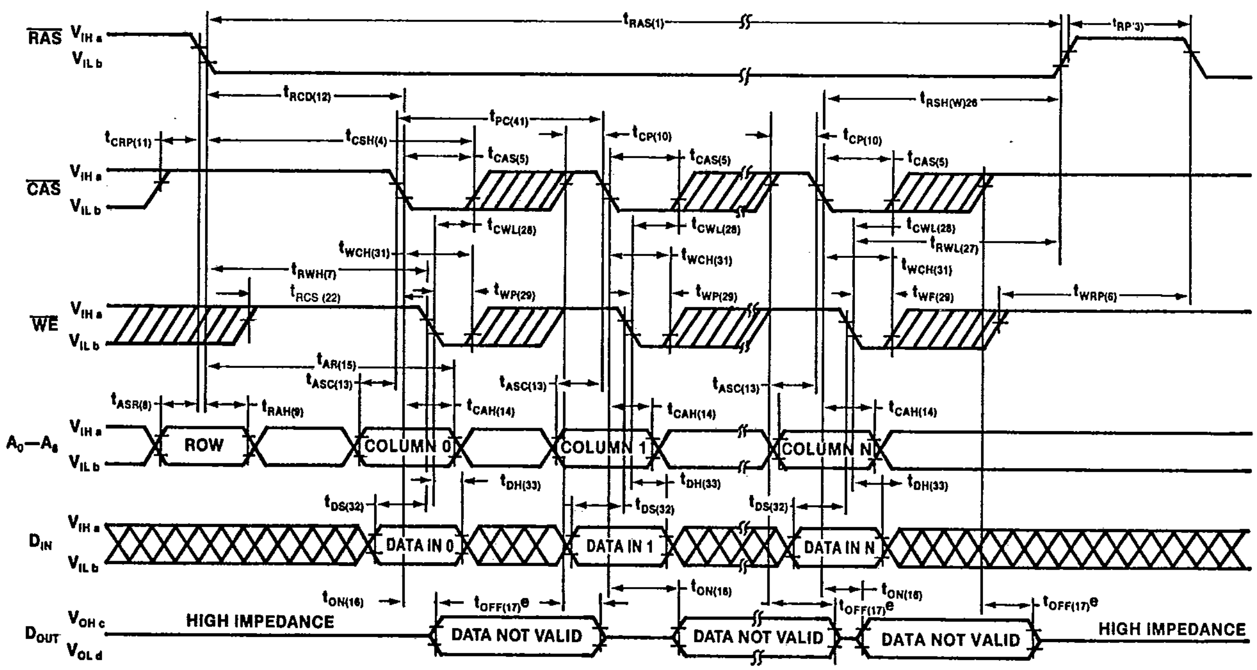
NOTES:
a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. Either t_{RCH} or t_{RRH} must be satisfied.
f. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

RIPPLEMODE* WRITE CYCLE ($\overline{CAS}$ CONTROLLED)[e]



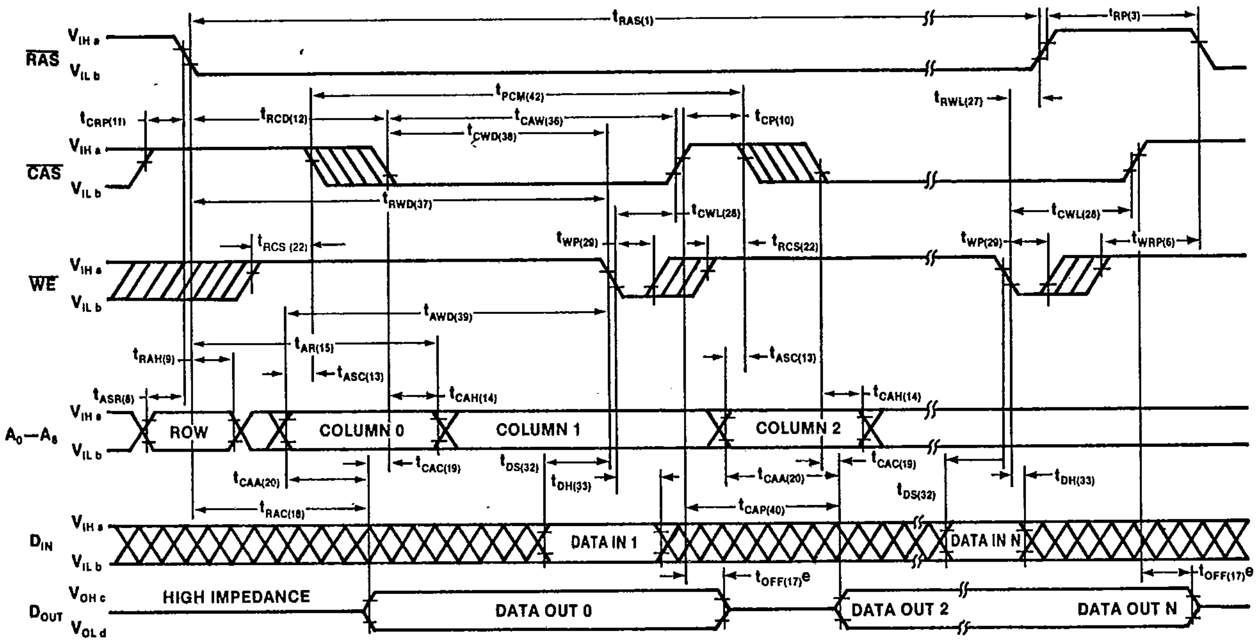
NOTES:
a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column address and D_{IN}

RIPPLEMODE* WRITE CYCLE ($\overline{WE}$ CONTROLLED)[f]



NOTES:
a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the D_{IN}

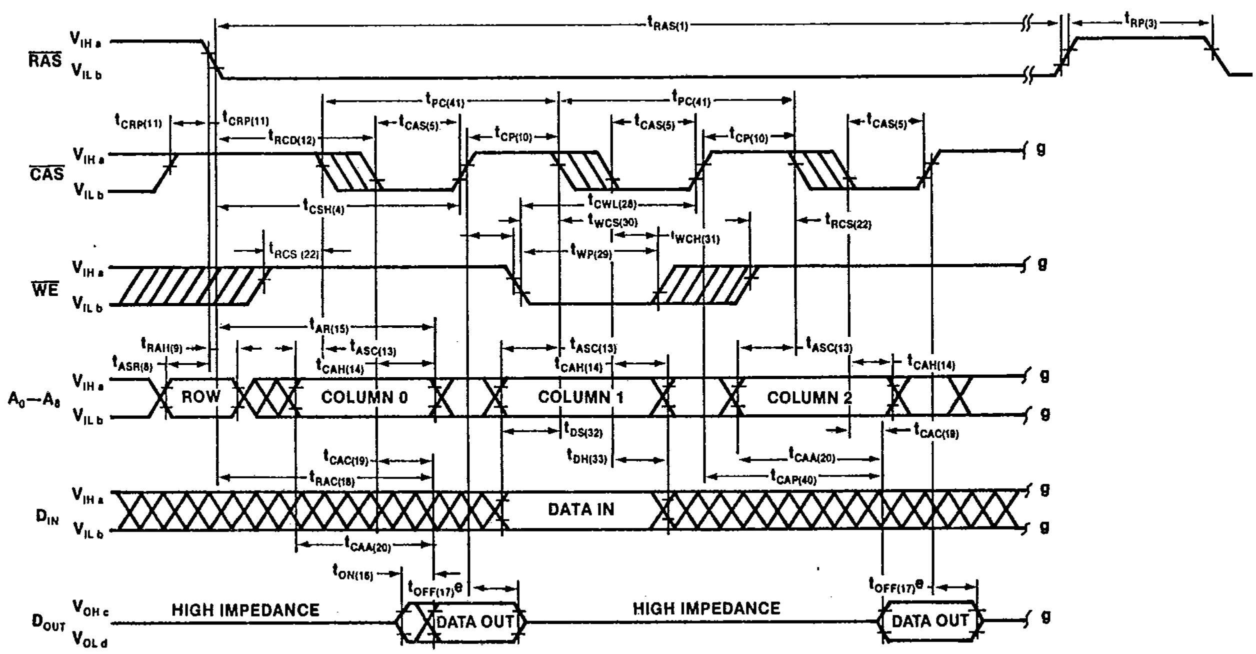
RIPPLEMODE* READ/MODIFY/WRITE CYCLE[f]



NOTES:

a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the D_{IN}

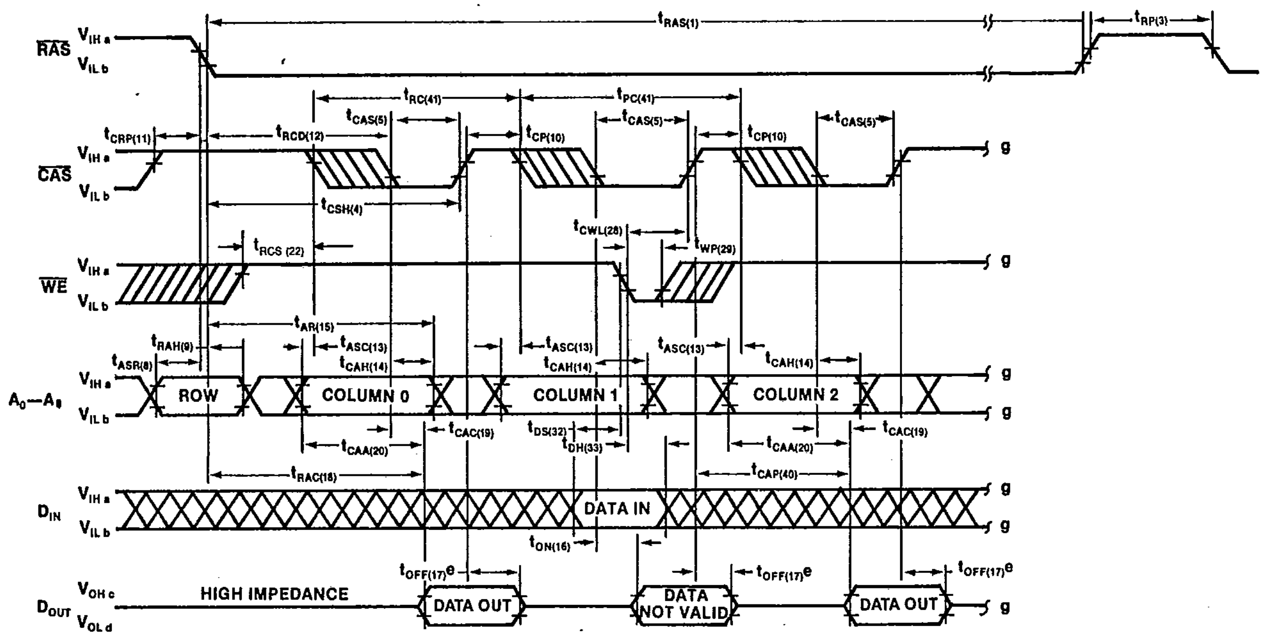
RIPPLEMODE* READ/WRITE/READ/...CYCLE ($\overline{CAS}$ CONTROLLED)[f]



NOTES:

a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column addresses and D_{IN}
g. The cycle can be terminated either by a read or a write operation followed by a $\overline{RAS}$ high transition. See page 8 or 9 for timing.

RIPPLEMODE* READ/WRITE/READ/...CYCLE ($\overline{WE}$ CONTROLLED)[f]



NOTES:

a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to $\overline{WE}$ low transition. $\overline{CAS}$ latches the column addresses while $\overline{WE}$ latches D_{IN}
g. The cycle can be terminated either by a read or write operation followed by a $\overline{RAS}$ high transition. See page 8 or 9 for timing.

FUNCTIONAL DESCRIPTION

The HY51C256/L is a CMOS dynamic RAM optimized for both high data bandwidth and low power applications. It is functionally similar to a traditional dynamic RAM. The HY51C256/L reads and writes data by multiplexing an 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is intiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among the t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the later of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state; terminating with $\overline{WE}$ allows the output to go active.

The HY51C256/L incorporates a self-timed write feature which simplifies the system interface. The write function is internally timed on a write command which allows for a fast write pulse width and a fast write precharge time, thus eliminating the need for critical placement of transitions during the write cycle.

REFRESH CYCLE

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will refresh the addressed row.

EXTENDED REFRESH CYCLE

The HY51C256L extends the refresh cycle period to 32 milliseonds for $\overline{RAS}$-Only refresh cycles. This feature reduces the total current consumption to a maximum of 200 μA and typically 85 μA, for data retention ($\overline{RAS}$-Only refresh operation for the HY51C256L-20 at $\overline{RAS} \geq V_{DD} - 0.2V$). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC}\, I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{t_{RI}}$$

where t_{RC}=refresh cycle time, and t_{RI}=refresh interval time or $t_{REF}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

RIPPLEMODE* OPERATION

Ripplemode* operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the addresses into the column address buffer and acts as an output enable.

During this operation read, write, read-modify write, or read-write-read cycles are possible at random or sequential addresses within a row. Following the entry cycle into Ripplemode*, access time is t_{CAA} or t_{CAP} dependent. If the column address is valid prior to or coincident with the rising edge of $\overline{CAS}$, then the access time is determined by the rising edge of $\overline{CAS}$ specified by t_{CAP} as shown in Figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Ripplemode* provides a sustained data rate over 12 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511\ t_{PC}}$$

DATA OUT OPERATION

The HY51C256/L Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

POWER ON

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).

The V_{DD} current (I_{DD}) requirement of the HY51C256/L during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ = V_{SS} during power on, the device will go into an active cycle and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

TABLE 1. HY51C256/L DATA OUTPUT OPERATION FOR VARIOUS TYPES OF CYCLES

CYCLE	DATA OUT STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{CAS}$ Controlled)	Data from Addressed Memory Cell
Read-Write-Read Cycle ($\overline{WE}$ Controlled)	Data from Addressed Memory Cell and Active, Not Valid
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Only Cycle	High Impedance

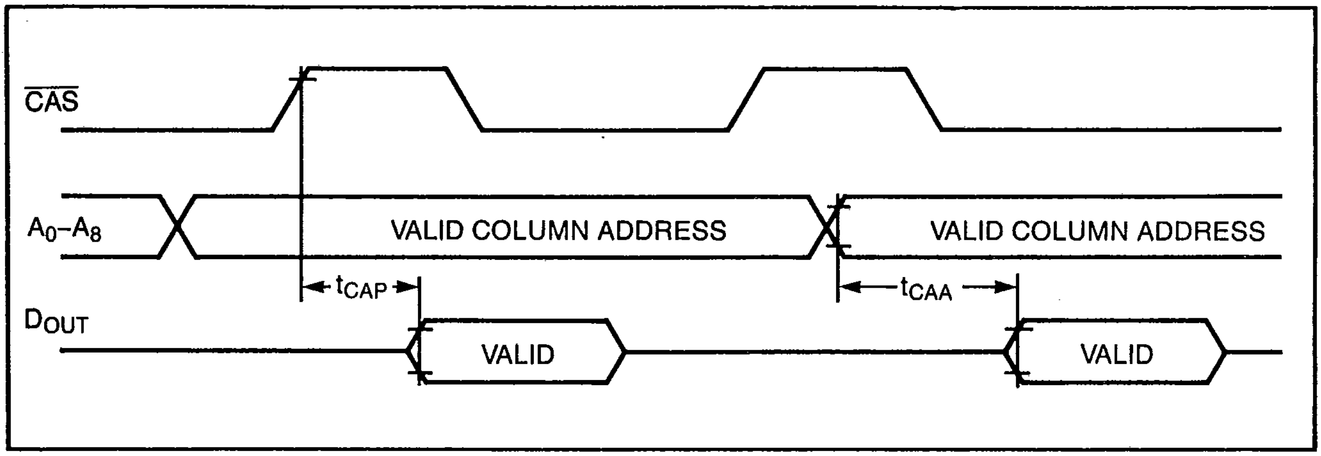


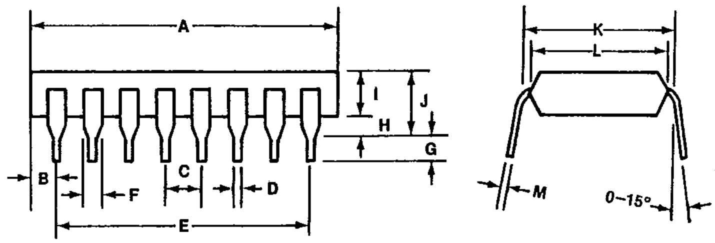
FIGURE 1. RIPPLEMODE* ACCESS TIME DETERMINATION

*Registered trademark of Intel Corporation.

PACKAGE OUTLINE

16 PIN PLASTIC

ITEM	MILLIMETERS	INCHES
A	19.05	0.750
B	0.635	0.025
C	2.54	0.100
D	0.457	0.018
E	17.78	0.700
F	1.524	0.060
G	3.302	0.130
H	0.508	0.020
I	3.302	0.130
J	3.81	0.150
K	7.62	0.300
L	6.35	0.250
M	0.254	0.010



ORDERING INFORMATION

HY51C256X XXX

- 10=100ns
  12=120ns
  15=150ns
  20=200ns
- S=PLASTIC DIP 300MIL
- NO MARK=Standard
  L=Low Power